



# SP0264

## NARRATOR® SPEECH PROCESSOR

### FEATURES

- Natural speech
- On-chip 64K bit ROM
- Stand alone operation with inexpensive support components
- Wide operating voltage
- Word, phrase or sentence library, ROM expandable
- Directly expandable to a total of 480K ROM
- Simple interface to most microcomputers or microprocessors
- Supports L.P.C. synthesis; formant synthesis; and allophone synthesis
- Pin compatible with the SP0256B speech synthesizer
- Available in -40° C to 85° C version

### APPLICATIONS

- Telecommunications
- Appliances
- Computer peripherals
- Automotive
- Personal computers
- Toys/games
- Educational aids
- Warning systems
- Security systems
- Electronic musical instruments
- Aids to the blind
- Narrow bandwidth communication systems

### DESCRIPTION

The SP0264 Speech Processor (SP) is a single chip N-Channel silicon gate MOS LSI device that is able, using its stored program, to synthesize speech or complex sounds.

The achievable output is equivalent to a flat frequency response ranging from 0 to 5kHz, a dynamic range of 42 dB, and a signal to noise ratio of approximately 35dB.

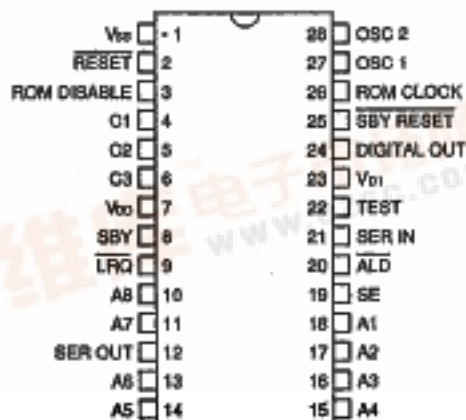
The SP0264 incorporates four basic functions:

- A software programmable digital filter that can be made to model a vocal tract.
- A 64K ROM which stores both data and instructions.
- A Microcontroller which controls the data flow from the ROM to the digital filter.
- A pulsewidth modulator that creates a digital output which is converted to an analog signal when filtered by an external low pass filter.

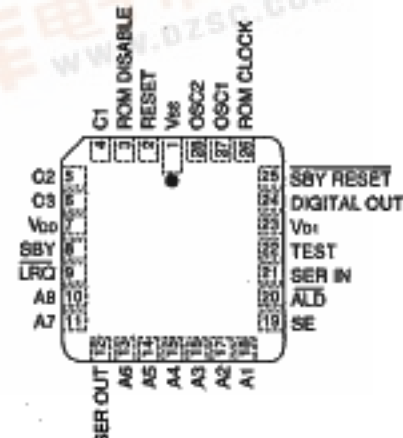
### PIN CONFIGURATION

Top View

#### 28 LEAD DUAL INLINE



#### 28 LEAD PLCC



● Pin 1 indicator on PLCC on top of package

## SP0264

### OPERATION

The addressing of the SP0264 is controlled by the address pins (A1-A8), Address Load ( $\overline{\text{ALD}}$ ), and Strobe Enable (SE). Speech data for the SP0264 may be stored within the internal 64K ROM and/or an external serial speech ROM.

There are two modes available for loading an address into the chip. Strobe Enable (SE) controls which mode will be used.

**Mode 0 (SE=0).** The speech processor will latch an address when any one (or more) address pin makes a low to high transition. All address lines must be returned to the low state prior to entering a new address. (Note: Address zero (0000 0000) is not a valid address in this mode of operation.) In order to best utilize this mode of operation, a vocabulary should consist of no more than eight individual words or phrases such that single address line transitions can be made. These words or phrases must be stored using the following entry point address: 1, 2, 4, 8, 16, 32, 64 and 128.

**NOTE:** There is a 2 byte overhead penalty paid for each dummy entry point between the entry points actually used.

**Mode 1 (SE=1).** The SP0264 will latch an address using the  $\overline{\text{ALD}}$  pin. The desired address is set up on the address bus (A1-A8) and then  $\overline{\text{ALD}}$  is pulsed low. Any address can be loaded using this mode, but certain set up and hold times are required (refer to the timing diagrams for the specific times).

Two microprocessor interface pins are available for loading of addresses using mode 1. They are  $\overline{\text{LRQ}}$  and SBY. Load Request ( $\overline{\text{LRQ}}$ ) tells the processor when the address input buffer is full. Standby (SBY) tells the processor that the chip has stopped talking and no new address has been loaded. When  $\overline{\text{LRQ}}$  is low, a new address may be loaded onto the address bus. Strobing  $\overline{\text{ALD}}$  will cause the new address to be loaded and  $\overline{\text{LRQ}}$  to go high.  $\overline{\text{LRQ}}$  will return low when the address buffer is available to accept a new address. The SP0264 is capable of latching one new address while speaking the last utterance (word or phrase). The time between address load requests is variable, depending on the length of the utterance currently being spoken.

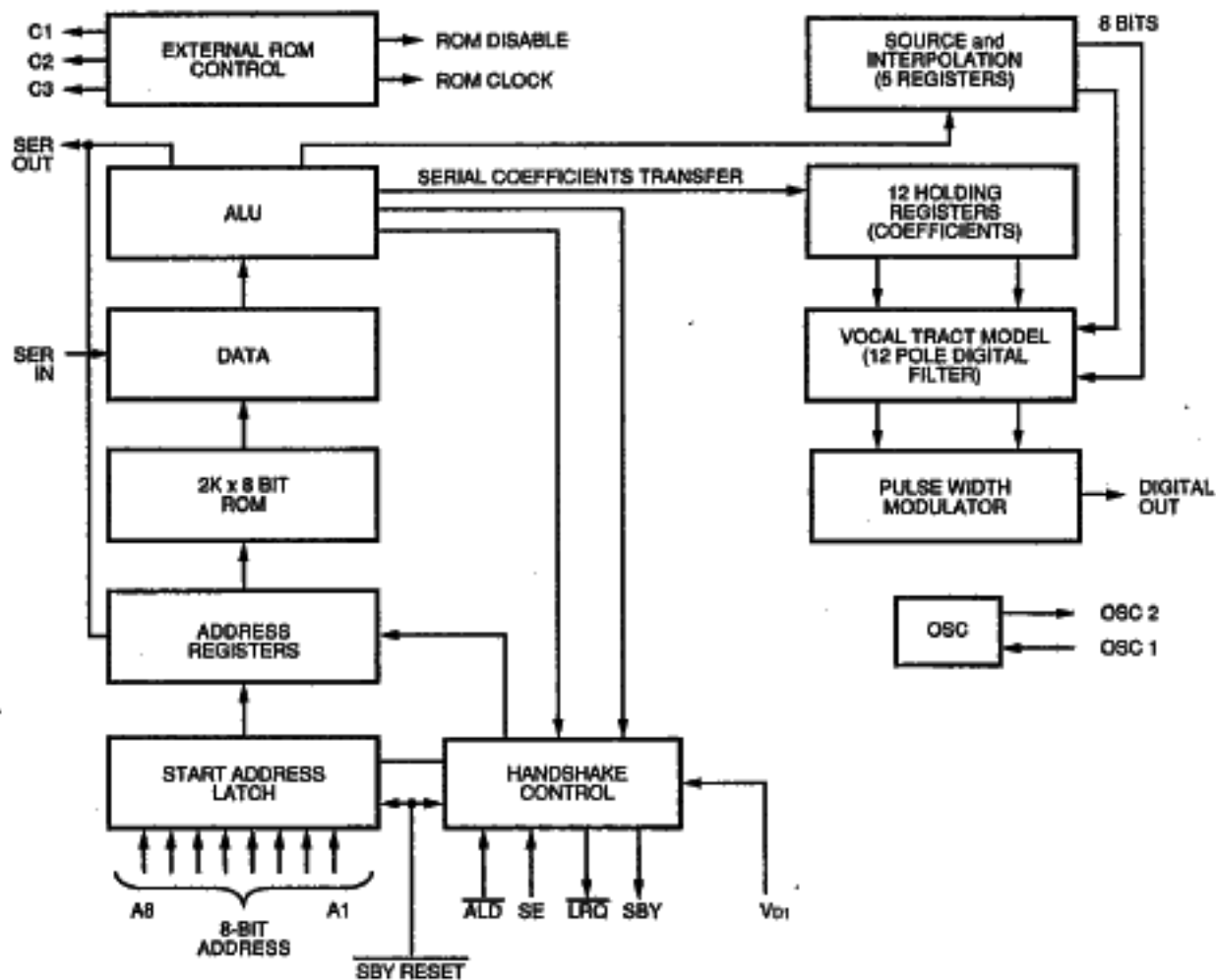
Standby (SBY) goes low when an address is loaded and will stay low until all internal instructions have been completed (i.e. the speech chip stops talking). If a second address has been loaded before the chip stops speaking the first utterance, SBY will stay low through the completion of the second utterance (ad infinitum).

The SP0264 may be partially powered down when SBY is high to conserve battery life, provided  $\text{V}_{\text{D1}}$  remains powered. During power down and power up, reset should be held low to ensure the proper reset condition. While the speech processor is in the partial power down state, the handshake control signals ( $\overline{\text{ALD}}$ , SE,  $\overline{\text{LRQ}}$ , and SBY) and the address bus are active. However, the SP0264 will not output the addressed speech data until after  $\text{V}_{\text{DD}}$  is reapplied.

### INTERNAL ROM DISABLE

This mode may be entered by wiring TEST to a permanent high. This causes the SP0264 to ignore its internal ROM to fetch data from external speech ROMs encoded by the DEVICE SELECT mask.

## SP0264 BLOCK DIAGRAM



## PIN FUNCTIONS

Pin Number	Name	Function
1	Vss	Ground
2 (input)	$\overline{\text{RESET}}$	A logic 0 resets that portion of the SP powered by VDD. Must be returned to logic 1 for normal operation. Upon reset C1, C2, C3, and SBY = 1.
3 (output)	ROM DISABLE	For use with an external serial speech ROM, a logic 1 disables the external ROM.
4, 5, 6 (outputs)	C1, C2, C3	Output control lines for use with an external serial speech ROM. Refer to the SPR128 data sheet for details.
7	VDD	Power supply for all portions of the SP except the microprocessor interface logic.
8 (output)	SBY	STANDBY. A logic 1 output indicates that the SP is inactive and VDD can be powered down externally to conserve power. When the SP is reactivated by an address being loaded, SBY will go to a logic 0.
9 (output)	$\overline{\text{LRQ}}$	LOAD REQUEST. $\overline{\text{LRQ}}$ is a logic 1 output whenever the input buffer is full. When $\overline{\text{LRQ}}$ goes to a logic 0, the input port may be loaded by placing the 8 address bits on A1-A8 and pulsing the $\overline{\text{ALD}}$ input.
10, 11, 13, 14, 15, 16, 17, 18	A8, A7, A6, A5 A4, A3, A2, A1	8 bit address which defines any one of 256 speech entry points.
12 (output)	SER OUT	SERIAL ADDRESS OUT. This output transfers a 16-bit address serially to an external speech ROM. When $\overline{\text{RESET}}$ and SBY RESET go to 0, SER OUT goes to 1.
19 (input)	SE	STROBE ENABLE. Normally held in a logic 1 state. When tied to ground, $\overline{\text{ALD}}$ is disabled and the SP will automatically latch in the address on the input bus approximately 1us after detecting a logic 1 on any address line.
20 (input)	$\overline{\text{ALD}}$	ADDRESS LOAD. A negative pulse on this input loads the 8 address bits into the input port. The negative edge of this pulse causes $\overline{\text{LRQ}}$ to go high.
21 (input)	SER IN	SERIAL IN. This is an 8-bit serial data input from an external speech ROM.
22 (input)	TEST	This pin should be grounded for normal operation. A logic 1 places the SP0264 in its test mode.

## PIN FUNCTIONS

Pin Number	Name	Function
23	V <sub>D1</sub>	Power supply for the microprocessor interface logic and controller. When not tied to V <sub>DD</sub> , V <sub>D1</sub> must remain high.
24 (output)	DIGITAL OUT	Pulse width modulated digital speech output which, when filtered by a 5kHz low pass filter and amplifier, will drive a loudspeaker.
25 (input)	<del>SBY RESET</del>	<del>STANDBY RESET</del> . A logic 0 resets the microprocessor interface logic and the address latches. Must be returned to logic 1 for normal operation. <del>SBY RESET</del> must be tied to RESET (pin 2).
26 (output)	ROM CLOCK	This is a 1.56MHz clock output used to drive an external serial speech ROM.
27 (input)	OSC1	XTAL IN. Input connection for a 3.12MHz crystal.
28 (output)	OSC2	XTAL OUT. Output connection for a 3.12MHz crystal.

**ELECTRICAL CHARACTERISTICS**

**Absolute maximum ratings over specified temperature range (unless otherwise noted)\***

All pins with respect to Vss ..... -0.3V to 8.0V

Storage Temperature ..... -25° C to 125° C

**Standard Conditions**

Clock - Crystal Frequency ..... 3.120MHz

Operating Temp (Commercial) ..... TA = 0° C to +70° C

Operating Temp (Industrial) ..... TA = -40° C to +85° C

\*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

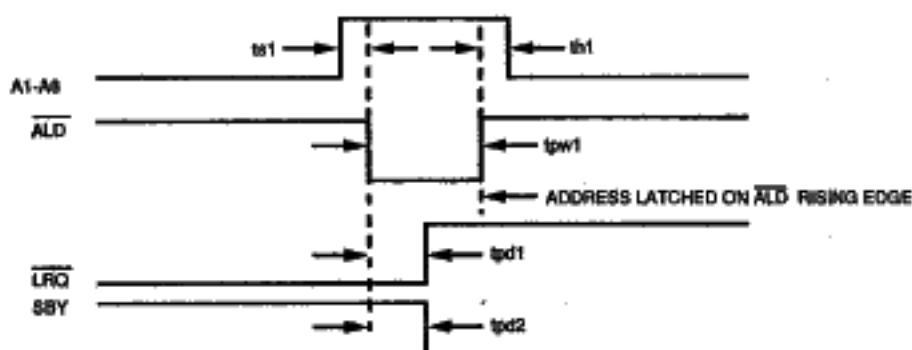
Data labeled "typical" is presented for design guidance only and is not guaranteed.

**DC CHARACTERISTICS**

Parameter	Sym	Min	Typ	Max	Units	Conditions
Primary Supply Voltage	VDD	4.5	-	6.5	V	
Standby Supply Voltage	V <sub>D1</sub>	4.5	-	6.5	V	
Primary Supply Current	I <sub>DD</sub>	-	35	65	mA	Reset and SBY Reset high. OSC1 = 3.12MHz. All other inputs floating.
Standby Supply Current	I <sub>D1</sub>	-	15	25	mA	Same as above.
<b>INPUTS</b>						
A1-A8, ALD, SERIN, TEST, SE						
LOGIC 0	V <sub>IL</sub>	0.0	-	0.6	V	
LOGIC 1	V <sub>IH</sub>	2.4	-	V <sub>D1</sub>	V	
CAPACITANCE	C <sub>IN</sub>	-	-	10	pf	0 volts bias, f = 3.12 MHz
LEAKAGE	I <sub>L</sub>	-	-	+10	μA	V <sub>FIN</sub> = 7.0V Other Pins = 0.0V
<b>RESET, SBY RESET</b>						
LOGIC 0	V <sub>RSIL</sub>	0.0	-	0.6	V	
LOGIC 1	V <sub>RSIH</sub>	4.0	-	V <sub>D1</sub>	V	V <sub>D1</sub> = 4.5V
		4.6	-	V <sub>D1</sub>	V	V <sub>D1</sub> = 6.5V
<b>OUTPUTS</b>						
SBY, Digital Out, C1, C2, C3, LRO, ROM DIS, ROM CLK, SEROUT						
LOGIC 0	V <sub>OL</sub>	0.0	-	0.6	V	I <sub>OL</sub> = 0.72mA (2LS TTL Loads)
LOGIC 1	V <sub>OH</sub>	2.5	-	V <sub>D1</sub>	V	I <sub>OH</sub> = -50μA (2LS TTL Loads)
<b>OSCILLATOR</b>						
OSC2 (Output)						
LOGIC 0	V <sub>OL</sub>	0.0	-	1.0	V	When driven from ext. input OSC1 (input) = 4.00V MIN at V <sub>D1</sub> = 4.50V
LOGIC 1	V <sub>OH</sub>	2.5	-	V <sub>D1</sub>	V	OSC1 (input) = 0.60V MAX
Short Circuit Current on OSC2	I <sub>SC</sub>	-7.5	-	-0.4	mA	OSC1 (input) = 0.60V OSC2 (output) = 0.00V
OSC1 Input Current	I <sub>IN</sub>	-4.9	-	-0.4	μA	OSC1 (input) = 0.00V

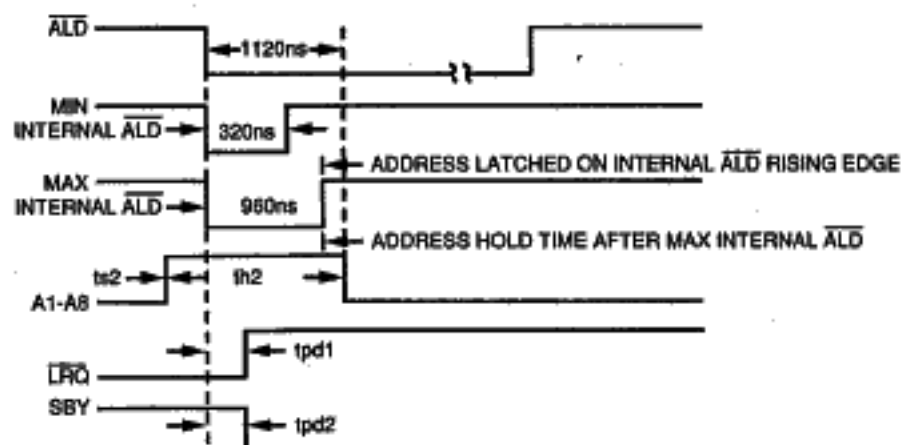
## AC CHARACTERISTICS - ALD HANDSHAKE CONTROL

Parameter	Sym	Min	Typ	Max	Units	Conditions
$\overline{\text{ALD}}$	tpw1	200	-	960	ns	$200 \leq \overline{\text{ALD}} \leq 960\text{ns}$
A1 - A8 Set Up	ts1	160	-	-	ns	
Hold	th1	160	-	-	ns	
$\overline{\text{LRQ}}$	tpd1	-	-	300	ns	
SBY	tpd2	-	-	300	ns	



## AC CHARACTERISTICS - LRQ HANDSHAKE CONTROL (BUFFERS FULL)

Parameter	Sym	Min	Typ	Max	Units	Conditions
A1 - A8 Set Up	$t_{s2}$	0	-	-	ns	$\overline{\text{ALD}} > 960\text{ns}$
Hold	$t_{h2}$	1120	-	-	ns	
$\overline{\text{LRQ}}$	$t_{pd1}$	-	-	300	ns	
SBY	$t_{pd2}$	-	-	300	ns	

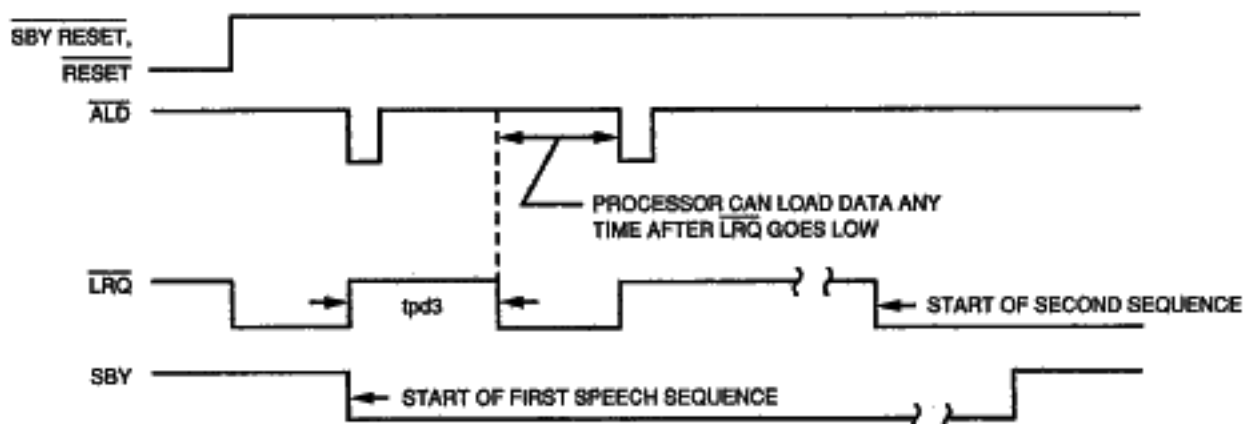


# SP0264

## AC CHARACTERISTICS - LRQ HANDSHAKE CONTROL (BUFFERS EMPTY)

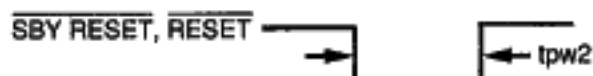
Parameter	Sym	Min	Typ	Max	Units	Conditions
LRQ	tpd3	16.67	-	33.3	μs	Address Buffer ready for next load.

## TYPICAL TIMING SEQUENCE



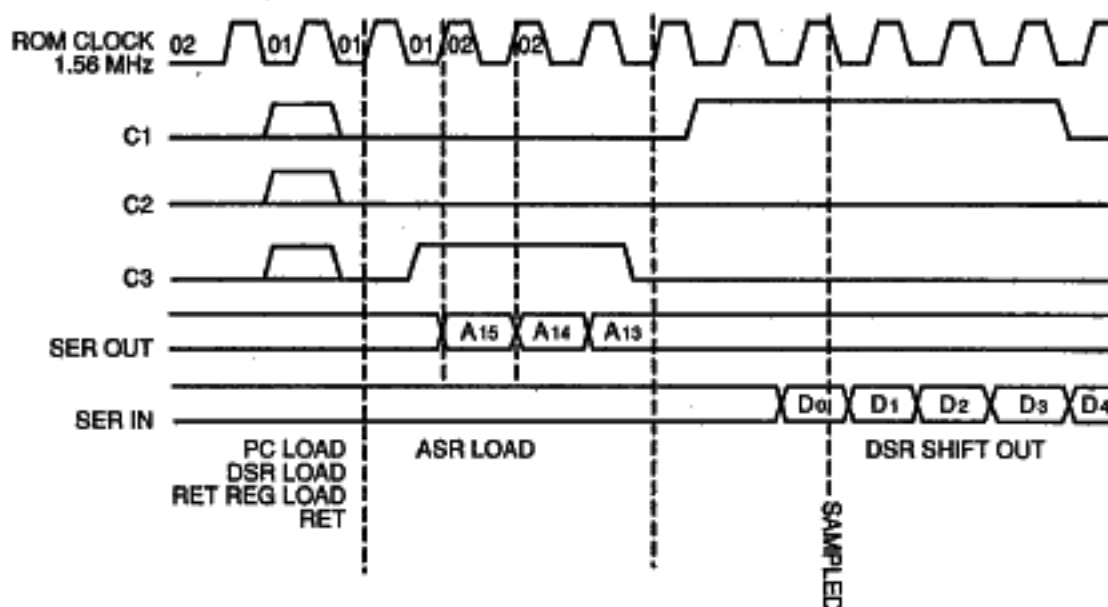
## AC CHARACTERISTICS - RESET TIMING

Parameter	Sym	Min	Typ	Max	Units	Conditions
Clock	F	3.11	3.120	3.13	MHz	Crystal oscillator driven from external.
Clock Duty Cycle	-	48	-	52	%	
Reset, SBY Reset	tpw2	25	-	-	μs	





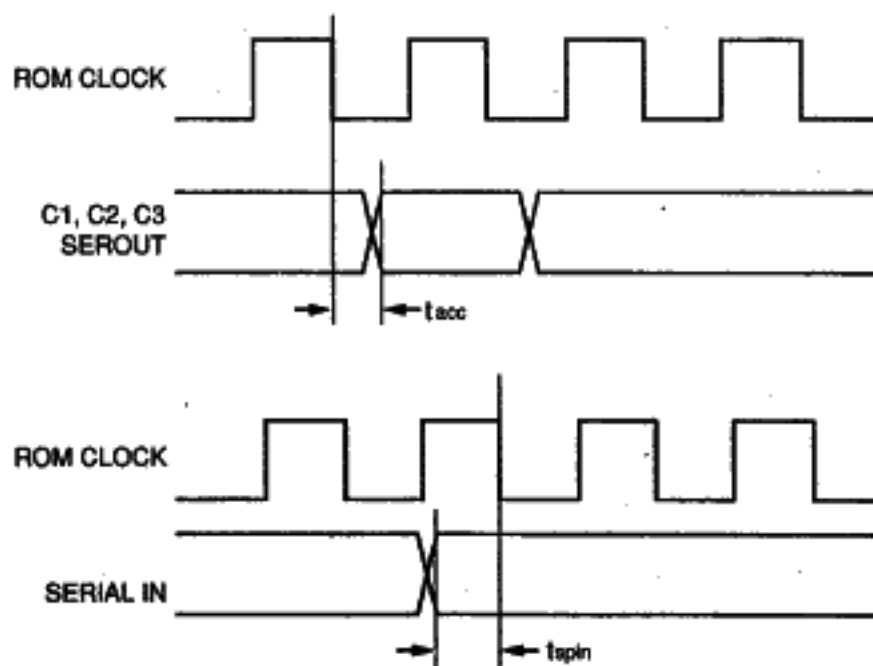
## EXTERNAL ROM INTERFACE TIMING



## AC CHARACTERISTICS - EXTERNAL ROM INTERFACE

Parameter	Sym	Min	Typ	Max	Units	Conditions
Access Time	$t_{acc}$		-	275	ns	
Serial Setup Time	$t_{pin}$	200	-	-	ns	

## EXTERNAL ROM INTERFACE TIMING



# SP0264

## SP0264 EXTERNAL AND INTERNAL CONTROL LINES\*

(All synchronous to the ROM clock)

### C1 C2 C3

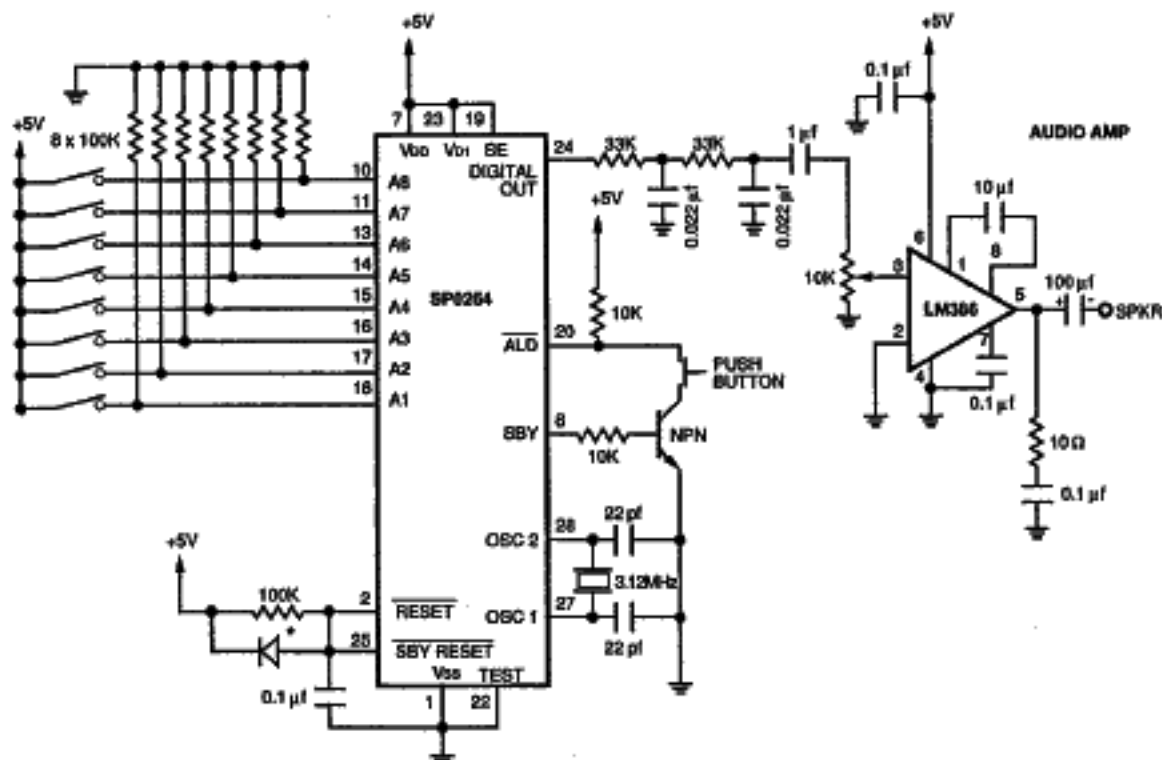
- 0 0 0 NOP - No Action Taken
- 0 0 1 ASRLD - (Address Shift Register Load) Serially shifts data (MSB first) from the serial address out pin (also occurs internally in the SP0264 into the ASR reg in preparation for loading into the PC). The ASRLD loads 16 bits of the ASR with two 8 bit load sequences followed shortly by a PCLD.
- 0 1 0 PCLD - Loads the contents of the ASR register into the PC. Occurs only after 16 ASRLDS have occurred.
- 0 1 1 DSRLD - (Data Shift Register Load) Loads the 8 bit data shift register with the contents of the ROM pointed to by the current address in the

### C1 C2 C3

- 1 0 0 DSRSH - (Data Shift Register Shift) Shifts data out of DSR reg starting with the second LSB (the first LSB is shifted out with the occurrence of a DSRLD). There are seven (7) DSRSH's after every DSRLD (not necessarily consecutive).
- 1 0 1 STACKLD - Loads the STACK with the current value of the PC.
- 1 1 0 RETURN - Loads the PC with the contents of the STACK.
- 1 1 1 Will occur in SP0264 when  $\overline{\text{SBY RESET}}$  and  $\overline{\text{RESET}} = "0"$ .

\*All ROMs including the SP0264 internal ROM will be activated by the above control lines. However, only the ROM with the current chip select will be enabled to send speech data to the SP0264.

### Typical Application: Stand Alone Configuration



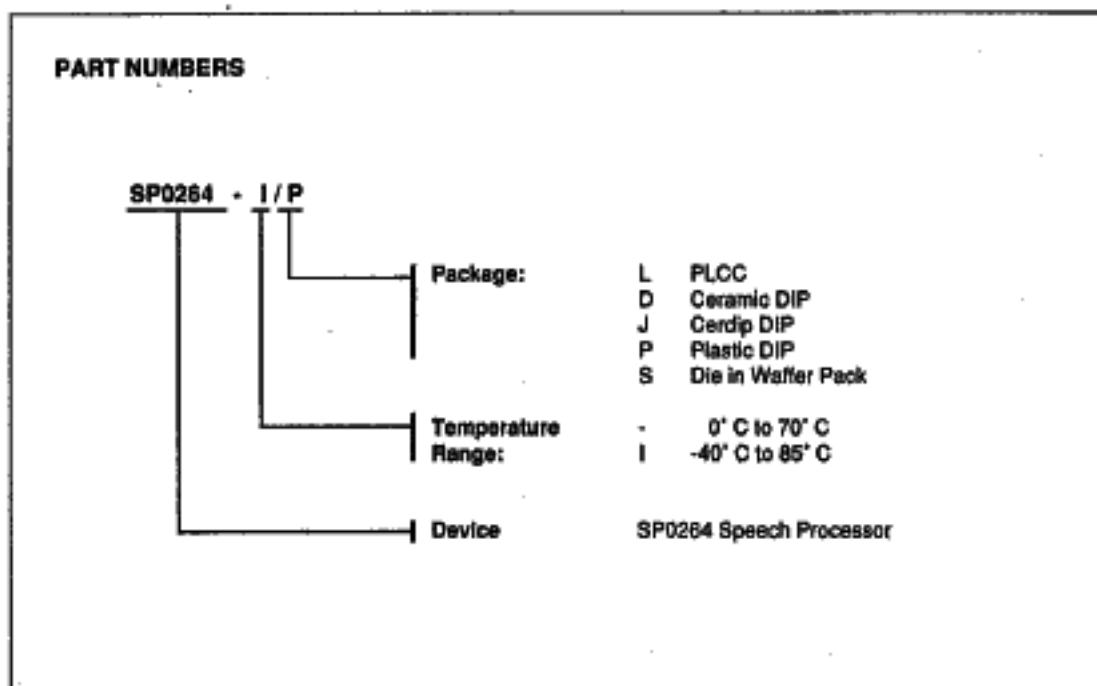
\* Diode possibly necessary if power is turned off then on in less than 50 ms.

[illegible]

## SP0264

### SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Microchip Technology Incorporated

Printed in USA © 8904

#### United States

##### Factory:

Microchip Technology Inc.  
2355 W Chandler Blvd.  
Chandler, AZ 85224-6199  
(602) 963-7373

##### Sales Offices:

Mid-West: (312) 505-0022  
New England: (617) 272-8030  
South-East: (404) 642-6933  
South-Central: (214) 733-0391  
North-West: (408) 436-7950  
South-West: (213) 323-1888

#### France

General Instrument Microelectronics  
Immeuble "Expansion"  
9/11, Rue Georges Enesco  
F-94008 Cretell Cedex  
(1) 43.99.12.63

#### West Germany

General Instrument Microelectronics  
Frelscheuetzstr. 96  
Postfach 810329  
D-8000 Muenchen 81  
(089) 95997-35

#### United Kingdom

General Instrument Microelectronics  
Times House, Ruislip  
Middlesex, HA4 8LE  
(0895) 636141

#### Hong Kong

Arizona Microchip Technology Ltd.  
Room 1103, Tower 1,  
South Seas Centre  
75, Mody Road  
Tsimshatsui East, Kowloon  
3/3116103

#### Japan

Microchip Technology Inc.  
4F Madre Matsuda Building  
4-13, Kioi Cho  
Chiyoda-Ku, Tokyo 102  
3/2348774

#### Singapore

Quadrep Marketing (S) PTE Ltd.  
1 Selegie Road, #09-06 Paradiz Centre  
Singapore 0718  
3394630

#### Taiwan

Microchip Technology Taiwan  
c/o General Instrument  
233 Pao Chiao Road, Hsin Tien  
Taipei Hsien  
2/9146234

#### Korea

Microchip Technology Ltd.,  
c/o Dae Ho Corporation  
1004, Keo Yang Bldg.  
51-8 Soosong Dong, Chongro-Ku  
Seoul  
2/7398543

