Enhanced Low Power Half-Duplex RS-485 Transceivers

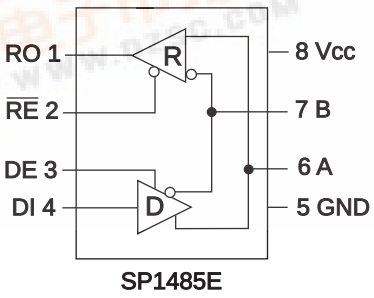
- +5V supply
- Low Power BiCMOS
- Driver/Receiver Enable for Multi-Drop configurations
- Available in 8 Pin NSOIC or PDIP packages
- Enhanced ESD Specifications:

  ±15KV Human Body Model
  ±15KV IEC1000-4-2 Air Discharge
  ±8KV IEC1000-4-2 Contact Discharge

DESCRIPTION

The **SP1485E** is a half-duplex transceiver that meets the specifications of RS-485 and RS-422 serial protocols with enhanced ESD performance. The ESD tolerance has been improved on this device to over ±15KV for both Human Body Model and IEC1000-4-2 Air Discharge Method. This device is pin-to-pin compatible with Sipex's SP485 devices as well as popular industry standards. As with the original version, the **SP1485E** features Sipex's BiCMOS design allowing low power operation without sacrificing performance. The **SP1485E** meets the requirements of the RS-485 and RS-422 protocols up to 20Mbps under load.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC}.....+7V

Input Voltages

Logic.....-0.3V to (V_{CC}+0.5V)

Drivers.....-0.3V to (V_{CC}+0.5V)

Receivers..... ±15V

Output Voltages

Logic.....-0.3V to (V_{CC}+0.5V)

Drivers..... ±15V

Receivers.....-0.3V to (V_{CC}+0.5V)

Storage Temperature.....-65˚C to +150˚C

Power Dissipation per Package

8-pin NSOIC (derate 6.60mW/ºC above +70ºC).....550mW

8-pin PDIP (derate 11.8mW/ºC above +70ºC).....1000mW

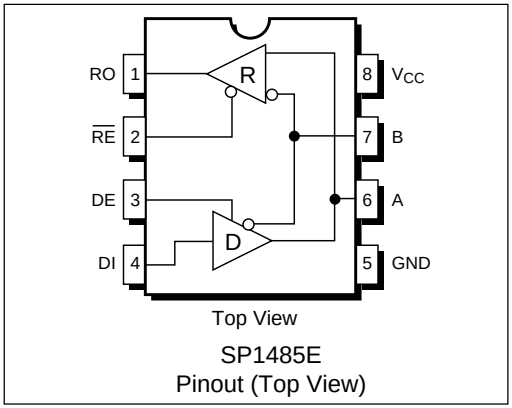
ELECTRICAL CHARACTERISTICS

T_{MIN} to T_{MAX} and V_{CC} = 5V ± 5% unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SP1485E DRIVER					
DC Characteristics					
Differential Output Voltage	3.5		V_{CC}	Volts	Unloaded; R = ∞ ; *see Figure 1*
Differential Output Voltage	2		V_{CC}	Volts	with load; R = 50Ω; (RS-422); *see Figure 1*
Differential Output Voltage	1.5		V_{CC}	Volts	with load; R = 27Ω; (RS-485);*see Figure 1*
Change in Magnitude of Driver Differential Output Voltage for Complimentary States			0.2	Volts	R = 27Ω or R = 50Ω; *see Figure 1*
Driver Common-Mode Output Voltage			3	Volts	R = 27Ω or R = 50Ω; *see Figure 1*
Input High Voltage	2.0			Volts	Applies to DE, DI, $\overline{RE}$
Input Low Voltage			0.8	Volts	Applies to DE, DI, $\overline{RE}$
Input Current			±10	µA	Applies to DE, DI, $\overline{RE}$
Driver Short-Circuit Current					
V_{OUT} = HIGH			±250	mA	-7V ≤ V_O ≤ +12V
V_{OUT} = LOW			±250	mA	-7V ≤ V_O ≤ +12V
SP1485E DRIVER					
AC Characteristics					
Maximum Data Rate	20			Mbps	$\overline{RE}$ = 5V, DE = 5V; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF
Driver Input to Output	10	30	40	ns	t_{PLH}; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *see Figures 3 and 5*
	10			ns	t_{PHL}; R_{DIFF} = 54Ω, C_{LI} = C_{L2} = 100pF;
Driver Skew		3		ns	*see Figures 3 and 5,* t_{SKEW} = | t_{DPLH} - t_{DPHL} |
Driver Rise or Fall Time		8	20	ns	From 10% to 90%; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *see Figures 3 & 6*
Driver Enable to Output High		40	70	ns	C_L = 100pF; *see Figures 4 & 6;* S_2 closed
Driver Enable to Output Low		40	70	ns	C_L = 100pF; *see Figures 4 & 6;* S_1 closed
Driver Disable Time from Low		40	70	ns	C_L = 100pF; *see Figures 4 & 6;* S_1 closed
Driver Disable Time from High		40	70	ns	C_L = 100pF; *see Figures 4 & 6;* S_2 closed

T_{MIN} to T_{MAX} and V_{CC} = 5V ± 5% unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SP1485E RECEIVER					
DC Characteristics					
Differential Input Threshold	-0.2		+0.2	Volts	$-7V \le V_{CM} \le +12V$
Differential Input Threshold (SP1485EMN ONLY)	-0.4		+0.4	Volts	$-7V \le V_{CM} \le +12V$
Input Hysteresis		20		mV	V_{CM} = 0V
Output Voltage High	3.5			Volts	I_O = -4mA, V_{ID} = +200mV
Output Voltage Low			0.4	Volts	I_O = +4mA, V_{ID} = -200mV
Three-State (High Impedance) Output Current			±1	µA	$0.4V \le V_O \le 2.4V$; RE = 5V
Input Resistance	12	15		kΩ	$-7V \le V_{CM} \le +12V$
Input Current (A, B); V_{IN} = 12V			+1.0	mA	DE = 0V, V_{CC} = 0V or 5.25V, V_{IN} = 12V
Input Current (A, B); V_{IN} = -7V			-0.8	mA	DE = 0V, V_{CC} = 0V or 5.25V, V_{IN} = -7V
Short-Circuit Current	7		95	mA	$0V \le V_O \le V_{CC}$
SP1485E RECEIVER					
AC Characteristics					
Maximum Data Rate	20			Mbps	RE = 0V, DE = 0V
Receiver Input to Output	15	40	50	ns	t_{PLH}; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; *Figures 3 & 7*
	15			ns	t_{PHL}; R_{DIFF} = 54Ω, C_{LI} = C_{L2} = 100pF
Diff. Receiver Skew $\lvert t_{PLH} - t_{PHL} \rvert$		5	10	ns	R_{DIFF} = 54Ω; C_{L1} = C_{L2} = 100pF; *Figures 3 & 7*
Receiver Enable to Output Low		45	70	ns	C_{RL} = 15pF; *Figures 2 & 8;* S_1 closed
Receiver Enable to Output High		45	70	ns	C_{RL} = 15pF; *Figures 2 & 8;* S_2 closed
Receiver Disable from Low		45	70	ns	C_{RL} = 15pF; *Figures 2 & 8;* S_1 closed
Receiver Disable from High		45	70	ns	C_{RL} = 15pF; *Figures 2 & 8;* S_2 closed
POWER REQUIREMENTS					
Supply Voltage	+4.75		+5.25	Volts	
Supply Current					
SP1485E					
No Load		900		µA	RE, DI = 0V or V_{CC}; DE = V_{CC}
		600		µA	RE = 0V, DI = 0V or 5V; DE = 0V
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
Commercial (_C_)	0		+70	°C	
Industrial (_E_)	-40		+85	°C	
(_M_)	-40		+125	°C	
Storage Temperature	-65		+150	°C	
Package					
Plastic DIP (_P)					
NSOIC (_N)					



PIN FUNCTION

Pin 1 – RO – Receiver Output.

Pin 2 – $\overline{RE}$ – Receiver Output Enable Active LOW.

Pin 3 – DE – Driver Output Enable Active HIGH.

Pin 4 – DI – Driver Input.

Pin 5 – GND – Ground Connection.

Pin 6 – A – Driver Output/Receiver Input Non-inverting.

Pin 7 – B – Driver Output/Receiver Input Inverting.

Pin 8 – Vcc – Positive Supply 4.75V<Vcc< 5.25V.

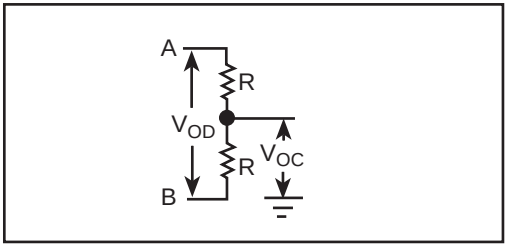


Figure 1. RS-485 Driver DC Test Load Circuit

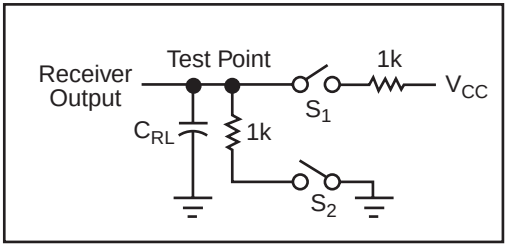


Figure 2. Receiver Timing Test Load Circuit

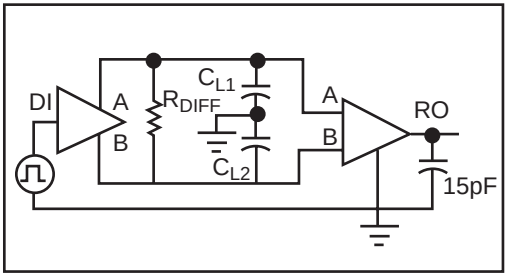


Figure 3. RS-485 Driver/Receiver Timing Test Circuit

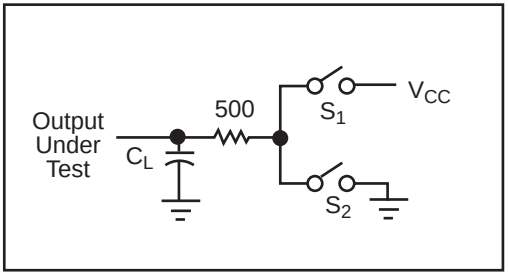


Figure 4. RS-485 Driver Timing Test Load #2 Circuit

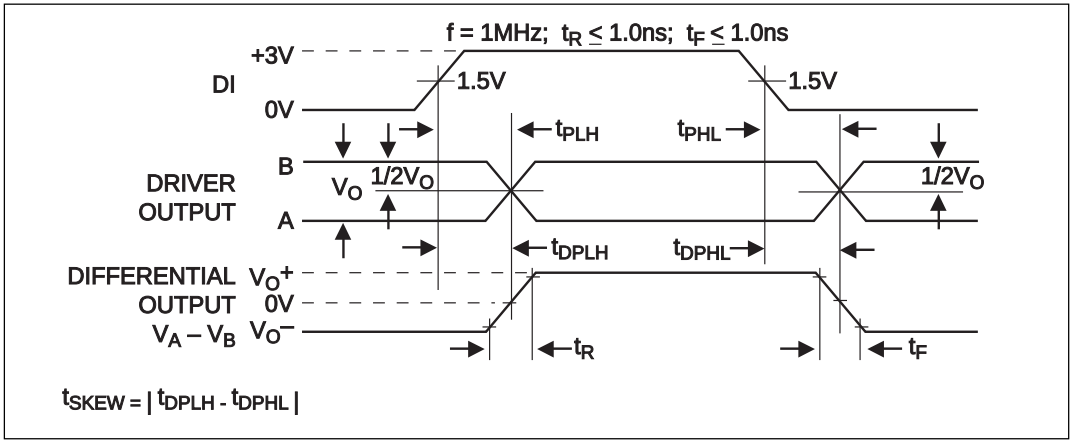


Figure 5. Driver Propagation Delays

INPUTS				OUTPUTS	
$\overline{RE}$	DE	DI	LINE CONDITION	B	A
X	1	1	No Fault	0	1
X	1	0	No Fault	1	0
X	0	X	X	Z	Z
X	1	X	Fault	Z	Z

Table 1. Transmit Function Truth Table

INPUTS			OUTPUTS
$\overline{RE}$	DE	A - B	R
0	0	+0.2V	1
0	0	-0.2V	0
0	0	Inputs Open	1
1	0	X	Z

Table 2. Receive Function Truth Table

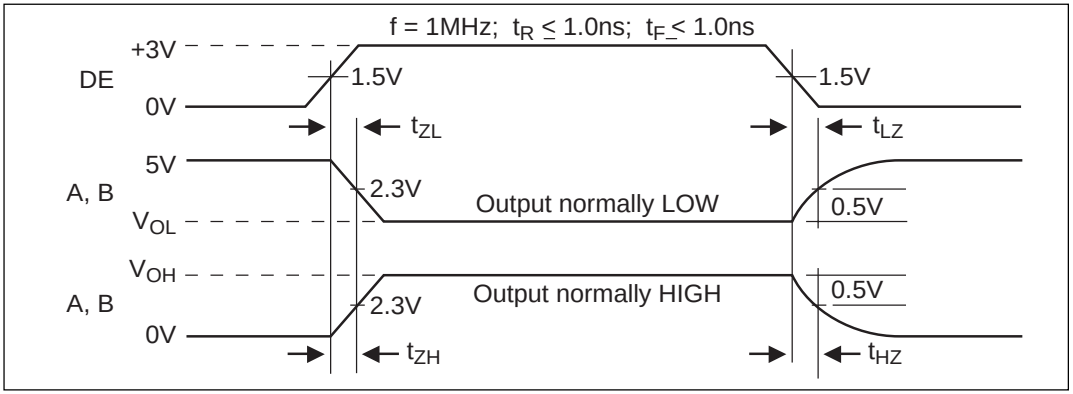


Figure 6. Driver Enable and Disable Times

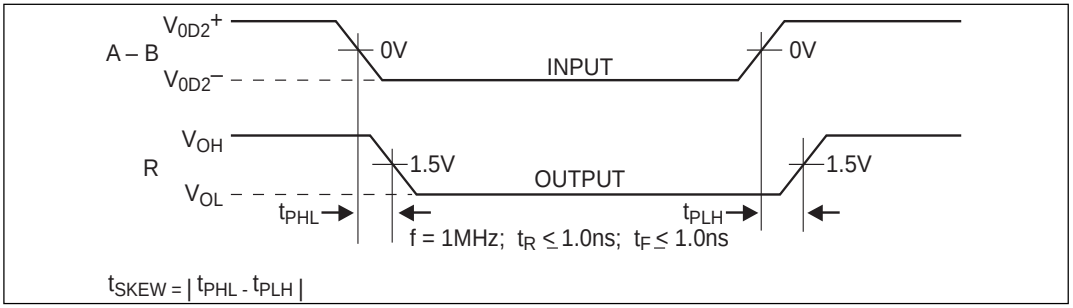


Figure 7. Receiver Propagation Delays

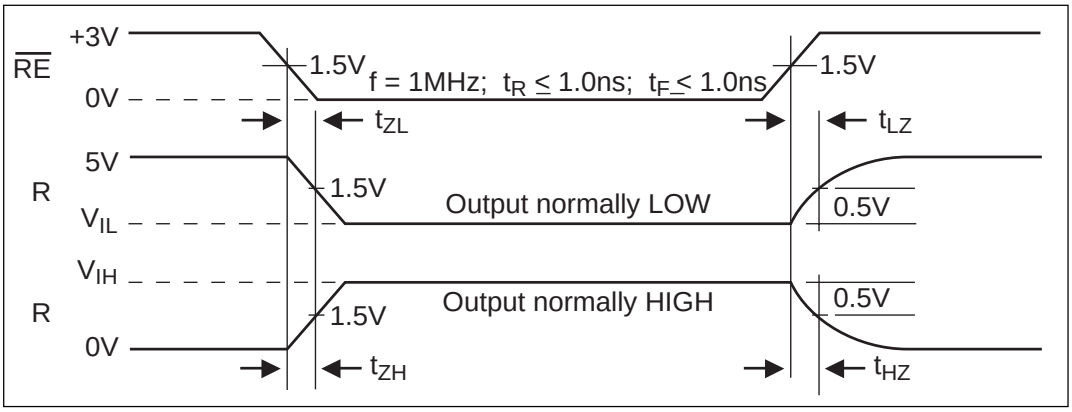


Figure 8. Receiver Enable and Disable Times

DESCRIPTION

The **SP1485E** is half-duplex differential transceivers that meet the requirements of RS-485 and RS-422. Fabricated with a Sipex proprietary BiCMOS process, this product requires a fraction of the power of older bipolar designs.

The RS-485 standard is ideal for multi-drop applications and for long-distance interfaces. RS-485 allows up to 32 drivers and 32 receivers to be connected to a data bus, making it an ideal choice for multi-drop applications. Since the cabling can be as long as 4,000 feet, RS-485 transceivers are equipped with a wide (-7V to +12V) common mode range to accommodate ground potential differences. Because RS-485 is a differential interface, data is virtually immune to noise in the transmission line.

Drivers

The driver outputs of the **SP1485E** are differential outputs meeting the RS-485 and RS-422 standards. The typical voltage output swing with no load will be 0 Volts to +5 Volts. With worst case loading of 54Ω across the differential outputs, the drivers can maintain greater than 1.5V voltage levels. The drivers of the **SP1485E** have an enable control line which is active HIGH. A logic HIGH on DE (pin 3) will enable the differential driver outputs. A logic LOW on DE (pin 3) will tri-state the driver outputs.

The transmitters of the **SP1485E** will operate up to at least 20Mbps.

Receivers

The **SP1485E** receivers have differential inputs with an input sensitivity as low as ±200mV. Input impedance of the receivers is typically 15kΩ (12kΩ minimum). A wide common mode range of -7V to +12V allows for large ground potential differences between systems. The receivers of the **SP1485E** have a tri-state enable control pin. A logic LOW on RE (pin 2) will enable the receiver, a logic HIGH on RE (pin 2) will disable the receiver.

The receiver for the **SP1485E** will operate up to at least 20Mbps. The receiver for each of the two devices is equipped with the fail-safe feature. Fail-safe guarantees that the receiver output will be in a HIGH state when the input is left unconnected.

ESD TOLERANCE

The **SP1485E** incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least ±15kV without damage or latch-up.

There are different methods of ESD testing applied:

a) MIL-STD-883, Method 3015.7
b) IEC1000-4-2 Air-Discharge
c) IEC1000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in *Figure 7*. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-1000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC1000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for

IEC1000-4-2 is shown on *Figure 8*. There are two methods within IEC1000-4-2, the Air Discharge method and the Contact Discharge method.

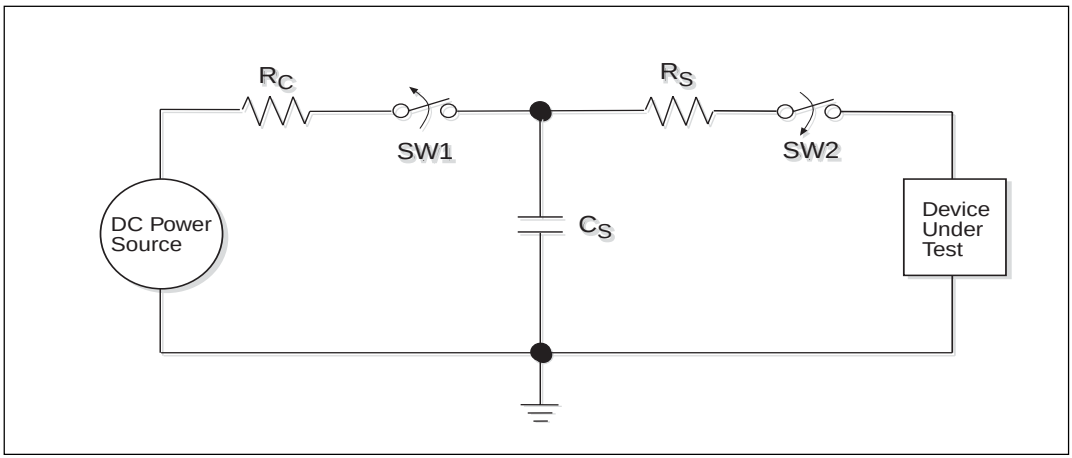


Figure 7. ESD Test Circuit for Human Body Model

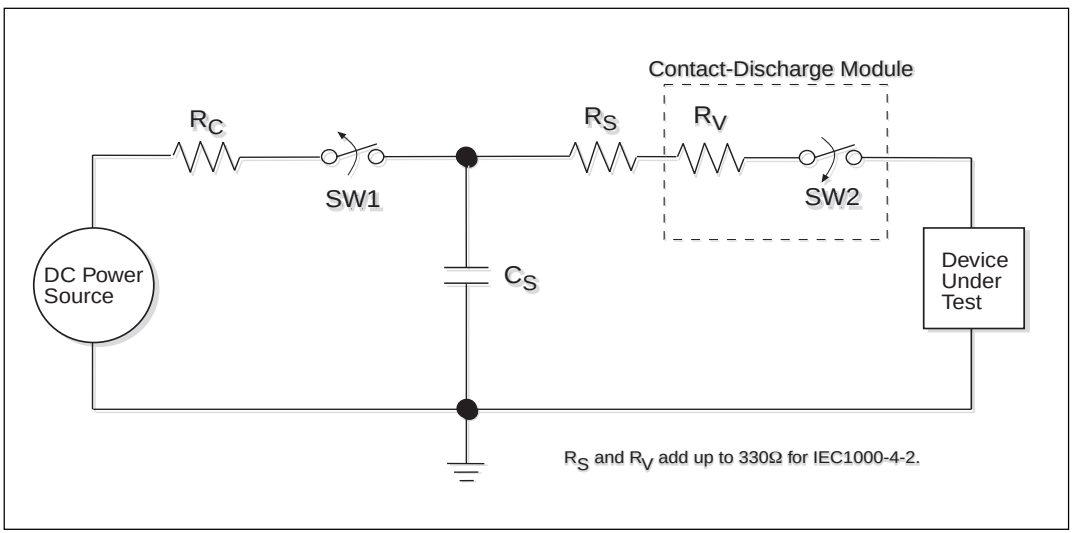


Figure 8. ESD Test Circuit for IEC1000-4-2

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

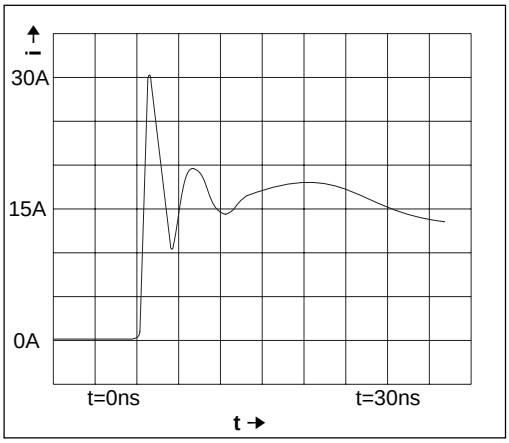


Figure 9. ESD Test Waveform for IEC1000-4-2

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

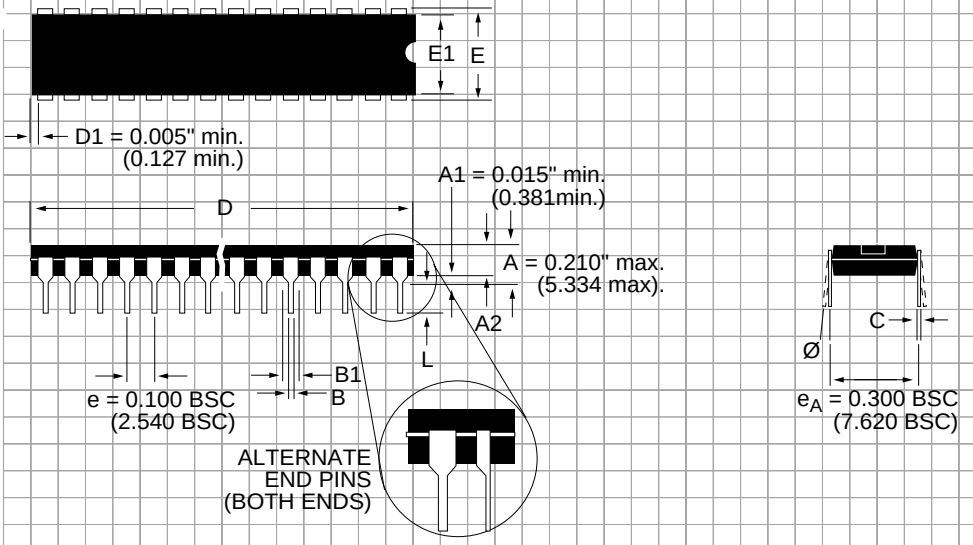
The circuit model in *Figures 7* and *8* represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S, the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ an 100pF, respectively. For IEC-1000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330Ω an 150pF, respectively.

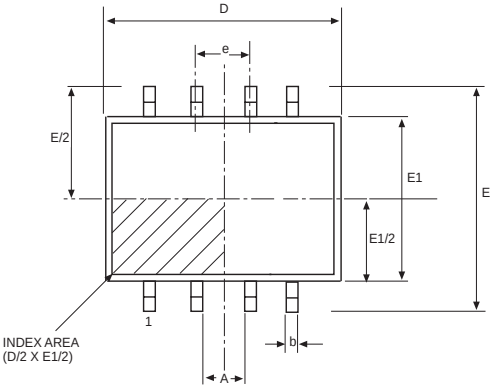
The higher C_S value and lower R_S value in the IEC1000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

SP1481E, SP1485E FAMILY	HUMAN BODY MODEL	IEC1000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	±15kV	±15kV	±8kV	4
Receiver Inputs	±15kV	±15kV	±8kV	4

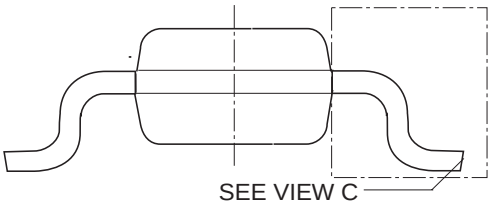
PACKAGE: PLASTIC DUAL–IN–LINE (NARROW)

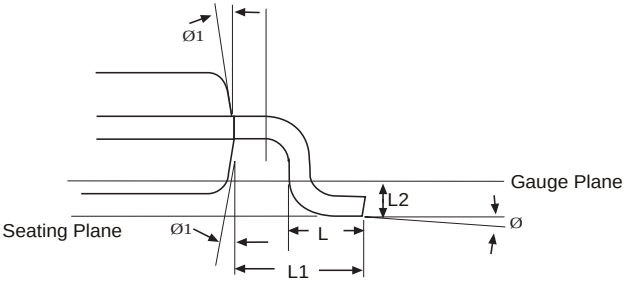


DIMENSIONS (Inches) Minimum/Maximum (mm)	8–PIN
A2	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)
D	0.355/0.400 (9.017/10.160)
E	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)
Ø	0°/ 15° (0°/15°)

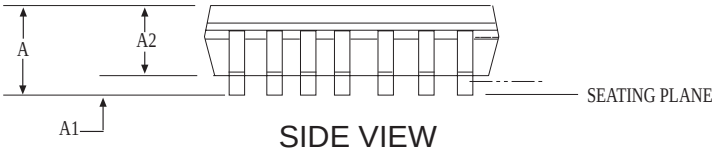


TOP VIEW



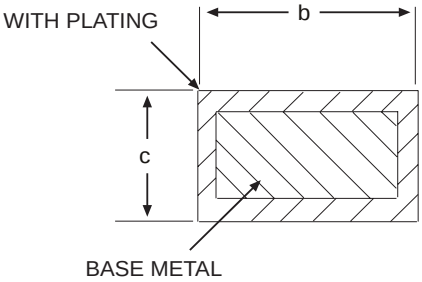


VIEW C



SIDE VIEW

DIMENSIONS Minimum/Maximum (mm)	8 Pin NSOIC (JEDEC MS-012, AA - VARIATION)		
COMMON HEIGHT DIMENSION			
SYMBOL	MIN	NOM	MAX
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
c	0.17	-	0.25
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.04 REF		
L2	0.25 BSC		
Ø	0º	-	8º
Ø1	5º	-	15º



CONTACT AREA

ORDERING INFORMATION

Model	Temperature Range	Package
SP1485ECN	0˚C to +70˚C	8-pin Narrow SOIC
SP1485ECP	0˚C to +70˚C	8-pin Plastic DIP
SP1485EEN	-40˚C to +85˚C	8-pin Narrow SOIC
SP1485EEP	-40˚C to +85˚C	8-pin Plastic DIP
SP1485EMN	-40˚C to +125˚C	8-pin Narrow SOIC

Please consult the factory for pricing and availability on a Tape-On-Reel option.

REVISION HISTORY

DATE	REVISION	DESCRIPTION
11/11/03	A	Implemented tracking revision.
12/18/03	B	Added Driver and Receiver TPLH/TPHL AC Characteristics.
02/26/04	C	Changed Driver Input to Output values from 20ns (typ), 30ns (max) to 30ns (typ), 40ns (max). Changed Receiver Input to Output values from 25ns (typ), 70ns (max) to 40ns (typ), 50ns (max) .

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