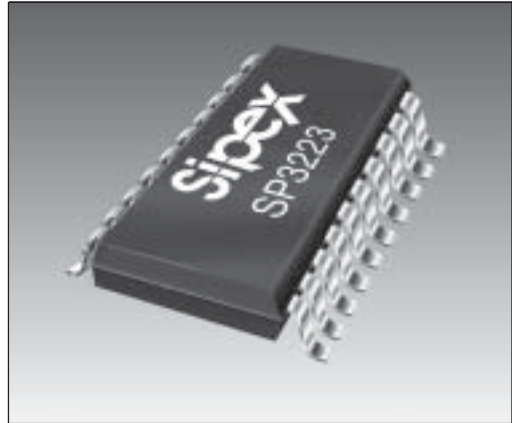


## Intelligent +3.0V to +5.5V RS-232 Transceivers

- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- Interoperable with EIA/TIA-232 and adheres to EIA/TIA-562 down to a +2.7V power source
- AUTO ON-LINE® circuitry automatically wakes up from a 1 $\mu$ A shutdown
- Minimum 120Kbps data rate under load
- Regulated Charge Pump Yields Stable RS-232 Outputs Regardless of V<sub>CC</sub> Variations
- ESD Specifications:
  - +2kV Human Body Model



### DESCRIPTION

The **SP3223** and **SP3243** products are RS-232 transceiver solutions intended for portable or hand-held applications such as notebook and palmtop computers. The **SP3223** and **SP3243** use an internal high-efficiency, charge-pump power supply that requires only 0.1 $\mu$ F capacitors in 3.3V operation. This charge pump and **Sipex's** driver architecture allow the **SP3223/SP3243** series to deliver compliant RS-232 performance from a single power supply ranging from +3.3V to +5.0V. The **SP3223** is a 2-driver/2-receiver device, and the **SP3243** is a 3-driver/5-receiver device ideal for laptop/notebook computer and PDA applications. The **SP3243** includes one complementary receiver that remains alert to monitor an external device's Ring Indicate signal while the device is shutdown.

The AUTO ON-LINE® feature allows the device to automatically "wake-up" during a shutdown state when an RS-232 cable is connected and a connected peripheral is turned on. Otherwise, the device automatically shuts itself down drawing less than 1 $\mu$ A.

### SELECTION TABLE

Device	Power Supplies	RS-232 Drivers	RS-232 Receivers	External Components	AUTO ON-LINE® Circuitry	TTL 3-State	No. of Pins
SP3223	+3.0V to +5.5V	2	2	4 capacitors	YES	YES	20
SP3243	+3.0V to +5.5V	3	5	4 capacitors	YES	YES	28

**Applicable U.S. Patents - 5,306,954; and other patents pending.**

## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

$V_{CC}$ .....	-0.3V to +6.0V
$V+$ (NOTE 1).....	-0.3V to +7.0V
$V-$ (NOTE 1).....	+0.3V to -7.0V
$V+ +  V- $ (NOTE 1).....	+13V
$I_{CC}$ (DC $V_{CC}$ or GND current).....	$\pm 100$ mA

### Input Voltages

$TxIN$ , <u>ONLINE</u> , SHUTDOWN, <u>EN (SP3223)</u> .....	-0.3V to +6.0V
$RxIN$ .....	$\pm 15$ V

### Output Voltages

$TxOUT$ .....	$\pm 15$ V
$RxOUT$ , <u>STATUS</u> .....	-0.3V to ( $V_{CC} + 0.3$ V)

### Short-Circuit Duration

$TxOUT$ .....	Continuous
Storage Temperature.....	-65°C to +150°C

## Power Dissipation per package

28-pin PDIP (derate 16.0mW/°C above+70°C)....1300mW  
 20-pin SSOP (derate 9.25mW/°C above +70°C)....750mW  
 20-pin TSSOP (derate 11.1mW/°C above +70°C)..900mW  
 28-pin SOIC (derate 12.7mW/°C above +70°C)...1000mW  
 28-pin SSOP (derate 11.2mW/°C above +70°C)....900mW

**NOTE 1:**  $V+$  and  $V-$  can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

## SPECIFICATIONS

Unless otherwise noted, the following specifications apply for  $V_{CC} = +3.0$ V to +5.5V with  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ .  
 Typical values apply at  $V_{CC} = +3.3$ V or +5.0V and  $T_{AMB} = 25^\circ$ C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>DC CHARACTERISTICS</b>					
Supply Current, AUTO ON-LINE®		1.0	10	$\mu$ A	All $RxIN$ open, <u>ONLINE</u> = GND, SHUTDOWN = $V_{CC}$ , $TxIN = V_{CC}$ or GND, $V_{CC} = +3.3$ V, $T_{AMB} = +25^\circ$ C
Supply Current, Shutdown		1.0	10	$\mu$ A	SHUTDOWN = GND, $TxIN = V_{CC}$ or GND, $V_{CC} = +3.3$ V, $T_{AMB} = +25^\circ$ C
Supply Current, AUTO ON-LINE® Disabled		0.3	1.0	mA	<u>ONLINE</u> = SHUTDOWN = $V_{CC}$ , no load, $V_{CC} = +3.3$ V, $T_{AMB} = +25^\circ$ C
<b>LOGIC INPUTS AND RECEIVER OUTPUTS</b>					
Input Logic Threshold LOW HIGH	2.0		0.8	V	$V_{CC} = +3.3$ V or +5.0V, $TxIN$ , <u>EN (SP3223)</u> , <u>ONLINE</u> , SHUTDOWN
Input Leakage Current		$\pm 0.01$	$\pm 1.0$	$\mu$ A	$TxIN$ , <u>EN</u> , <u>ONLINE</u> , SHUTDOWN, $T_{AMB} = +25^\circ$ C
Output Leakage Current		$\pm 0.05$	$\pm 10$	$\mu$ A	Receivers disabled
Output Voltage LOW			0.4	V	$I_{OUT} = 1.6$ mA
Output Voltage HIGH	$V_{CC} - 0.6$	$V_{CC} - 0.1$		V	$I_{OUT} = -1.0$ mA

## SPECIFICATIONS (continued)

Unless otherwise noted, the following specifications apply for  $V_{CC} = +3.0V$  to  $+5.5V$  with  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ . Typical values apply at  $V_{CC} = +3.3V$  or  $+5.0V$  and  $T_{AMB} = 25^{\circ}C$ .

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>DRIVER OUTPUTS</b>					
Output Voltage Swing	±5.0	±5.4		V	All driver outputs loaded with 3KΩ to GND, $T_{AMB} = +25^{\circ}C$
Output Resistance	300			Ω	$V_{CC} = V_{+} = V_{-} = 0V$ , $V_{OUT} = \pm 2V$
Output Short-Circuit Current		±35 ±70	±60 ±100	mA	$V_{OUT} = 0V$ $V_{OUT} = \pm 15V$
Output Leakage Current			±25	μA	$V_{CC} = 0V$ or $3.0V$ to $5.5V$ , $V_{OUT} = \pm 12V$ , Drivers disabled
<b>RECEIVER INPUTS</b>					
Input Voltage Range	-15		15	V	
Input Threshold LOW	0.6	1.2		V	$V_{CC} = 3.3V$
Input Threshold LOW	0.8	1.5		V	$V_{CC} = 5.0V$
Input Threshold HIGH		1.5	2.4	V	$V_{CC} = 3.3V$
Input Threshold HIGH		1.8	2.4	V	$V_{CC} = 5.0V$
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	kΩ	
<b>AUTO ON-LINE<sup>®</sup> CIRCUITRY CHARACTERISTICS (ONLINE = GND, SHUTDOWN = <math>V_{CC}</math>)</b>					
STATUS Output Voltage LOW			0.4	V	$I_{OUT} = 1.6mA$
STATUS Output Voltage HIGH	$V_{CC} - 0.6$			V	$I_{OUT} = -1.0mA$
Receiver Threshold to Drivers Enabled ( $t_{ONLINE}$ )		200		μS	Figure 15
Receiver Positive or Negative Threshold to STATUS HIGH ( $t_{STSH}$ )		0.5		μS	Figure 15
Receiver Positive or Negative Threshold to STATUS LOW ( $t_{STSL}$ )		20		μS	Figure 15

## SPECIFICATIONS (continued)

Unless otherwise noted, the following specifications apply for  $V_{CC} = +3.0V$  to  $+5.5V$  with  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ . Typical values apply at  $V_{CC} = +3.3V$  or  $+5.0V$  and  $T_{AMB} = 25^{\circ}C$ .

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>TIMING CHARACTERISTICS</b>					
Maximum Data Rate	120	235		kbps	$R_L = 3K\Omega$ , $C_L = 1000pF$ , one driver active
Receiver Propagation Delay $t_{PHL}$ $t_{PLH}$		0.3 0.3		$\mu s$	Receiver input to Receiver output, $C_L = 150pF$
Receiver Output Enable Time		200		ns	Normal operation
Receiver Output Disable Time		200		ns	Normal operation
Driver Skew		100	500	ns	$ t_{PHL} - t_{PLH} $ , $T_{AMB} = 25^{\circ}C$
Receiver Skew		200	1000	ns	$ t_{PHL} - t_{PLH} $
Transition-Region Slew Rate			30	$V/\mu s$	$V_{CC} = 3.3V$ , $R_L = 3K\Omega$ , $T_{AMB} = 25^{\circ}C$ , measurements taken from $-3.0V$ to $+3.0V$ or $+3.0V$ to $-3.0V$

## TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for  $V_{CC} = +3.3V$ , 120Kbps data rate, all drivers loaded with  $3K\Omega$ ,  $0.1\mu F$  charge pump capacitors, and  $T_{AMB} = +25^{\circ}C$ .

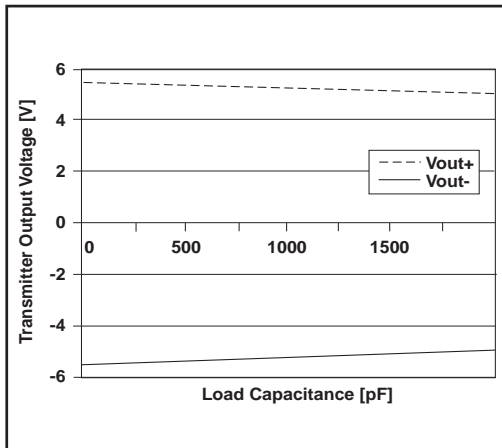


Figure 1. Transmitter Output Voltage VS. Load Capacitance for the SP3223

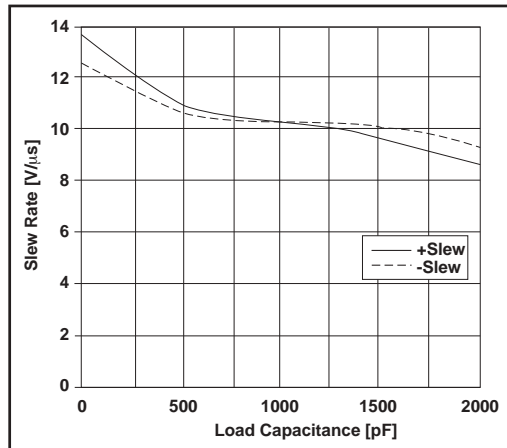


Figure 2. Slew Rate VS. Load Capacitance for the SP3223

# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise noted, the following performance characteristics apply for  $V_{CC} = +3.3V$ , 120Kbps data rate, all drivers loaded with  $3K\Omega$ ,  $0.1\mu F$  charge pump capacitors, and  $T_{AMB} = +25^{\circ}C$ .

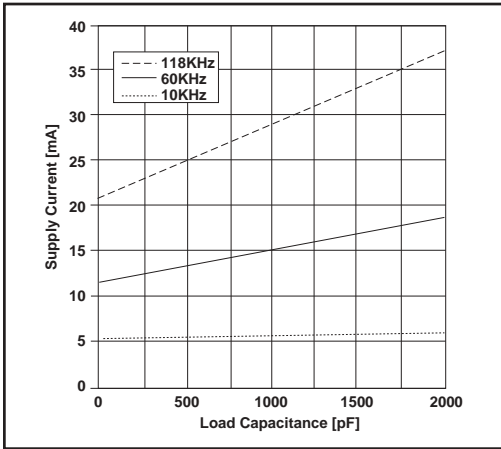


Figure 3. Supply Current VS. Load Capacitance when Transmitting Data for the SP3223

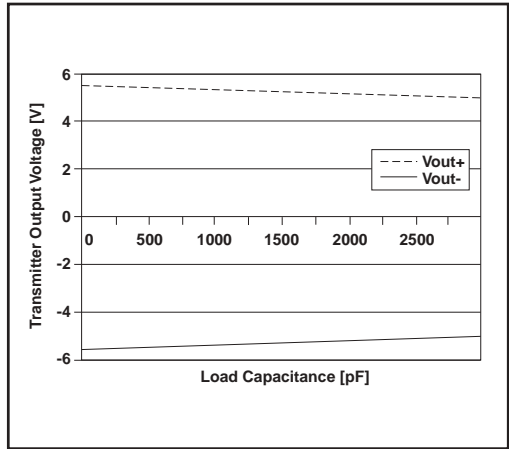


Figure 4. Transmitter Output Voltage VS. Load Capacitance for the SP3243

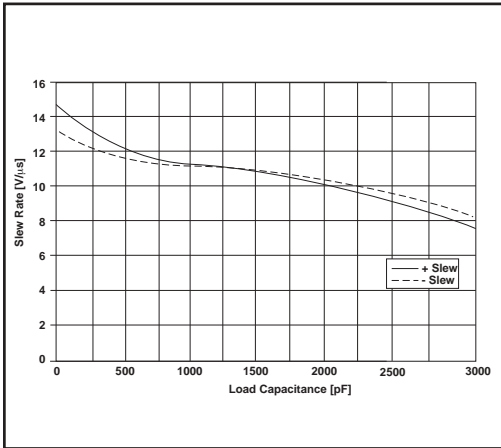


Figure 5. Slew Rate VS. Load Capacitance for the SP3243

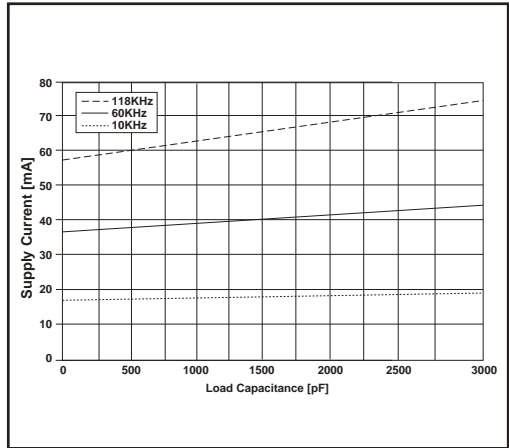


Figure 6. Supply Current VS. Load Capacitance when Transmitting Data for the SP3243

NAME	FUNCTION	PIN NUMBER	
		SP3223	SP3243
$\overline{\text{EN}}$	Receiver Enable. Apply logic LOW for normal operation. Apply logic HIGH to disable the receiver outputs (high-Z state).	1	-
C1+	Positive terminal of the voltage doubler charge-pump capacitor.	2	28
V+	Regulated +5.5V output generated by the charge pump.	3	27
C1-	Negative terminal of the voltage doubler charge-pump capacitor.	4	24
C2+	Positive terminal of the inverting charge-pump capacitor.	5	1
C2-	Negative terminal of the inverting charge-pump capacitor.	6	2
V-	Regulated -5.5V output generated by the charge pump.	7	3
R <sub>1</sub> IN	RS-232 receiver input.	16	4
R <sub>2</sub> IN	RS-232 receiver input.	9	5
R <sub>3</sub> IN	RS-232 receiver input.	-	6
R <sub>4</sub> IN	RS-232 receiver input.	-	7
R <sub>5</sub> IN	RS-232 receiver input.	-	8
R <sub>1</sub> OUT	TTL/CMOS receiver output.	15	19
R <sub>2</sub> OUT	TTL/CMOS receiver output.	10	18
$\overline{\text{R}}_2\text{OUT}$	Non-inverting receiver-2 output, active in shutdown.	-	20
R <sub>3</sub> OUT	TTL/CMOS receiver output.	-	17
R <sub>4</sub> OUT	TTL/CMOS receiver output.	-	16
R <sub>5</sub> OUT	TTL/CMOS receiver output.	-	15
$\overline{\text{STATUS}}$	TTL/CMOS Output indicating online and shutdown status.	11	21
T <sub>1</sub> IN	TTL/CMOS driver input.	13	14
T <sub>2</sub> IN	TTL/CMOS driver input.	12	13
T <sub>3</sub> IN	TTL/CMOS driver input.	-	12
$\overline{\text{ONLINE}}$	Apply logic HIGH to override <i>AUTO ON-LINE</i> circuitry keeping drivers active (SHUTDOWN must also be logic HIGH, refer to Table 2).	14	23
T <sub>1</sub> OUT	RS-232 driver output.	17	9
T <sub>2</sub> OUT	RS-232 driver output.	8	10
T <sub>3</sub> OUT	RS-232 driver output.	-	11
GND	Ground.	18	25
V <sub>CC</sub>	+3.0V to +5.5V supply voltage.	19	26
$\overline{\text{SHUTDOWN}}$	Apply logic LOW to shut down drivers and charge pump. This overrides all AUTO ON-LINE <sup>®</sup> circuitry and ONLINE (refer to Table 2).	20	22

Table 1. Device Pin Description

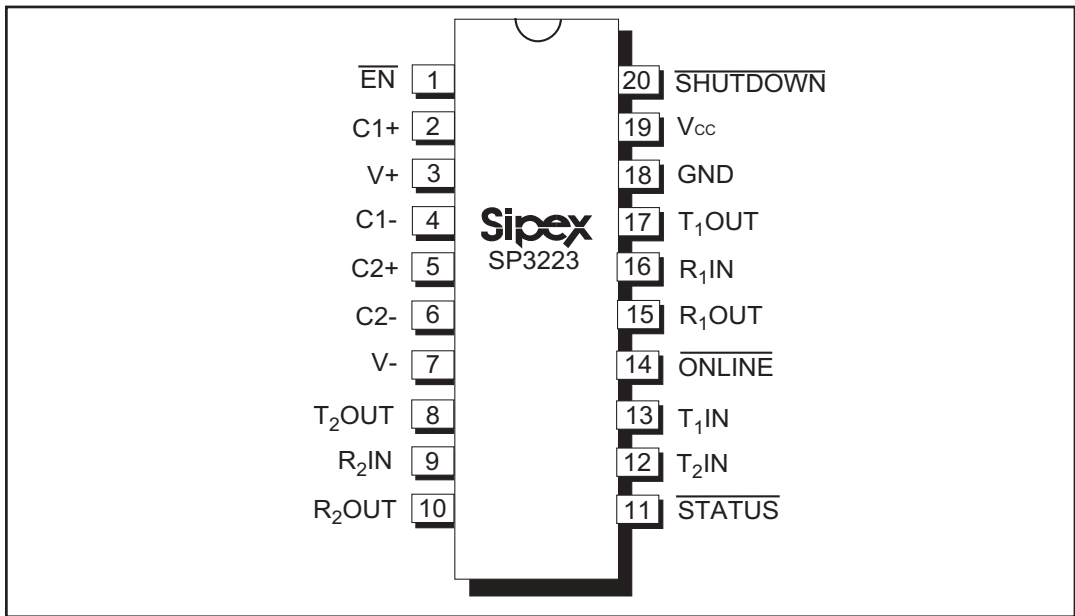


Figure 7. SP3223 Pinout Configuration

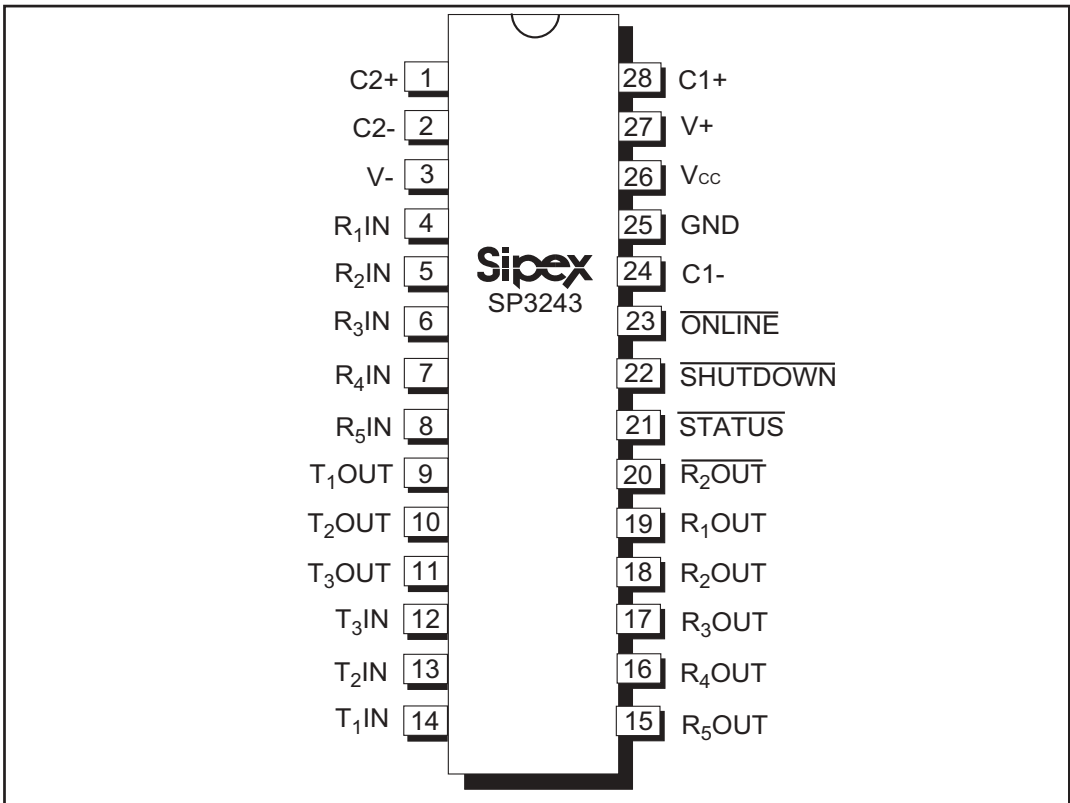


Figure 8. SP3243 Pinout Configuration

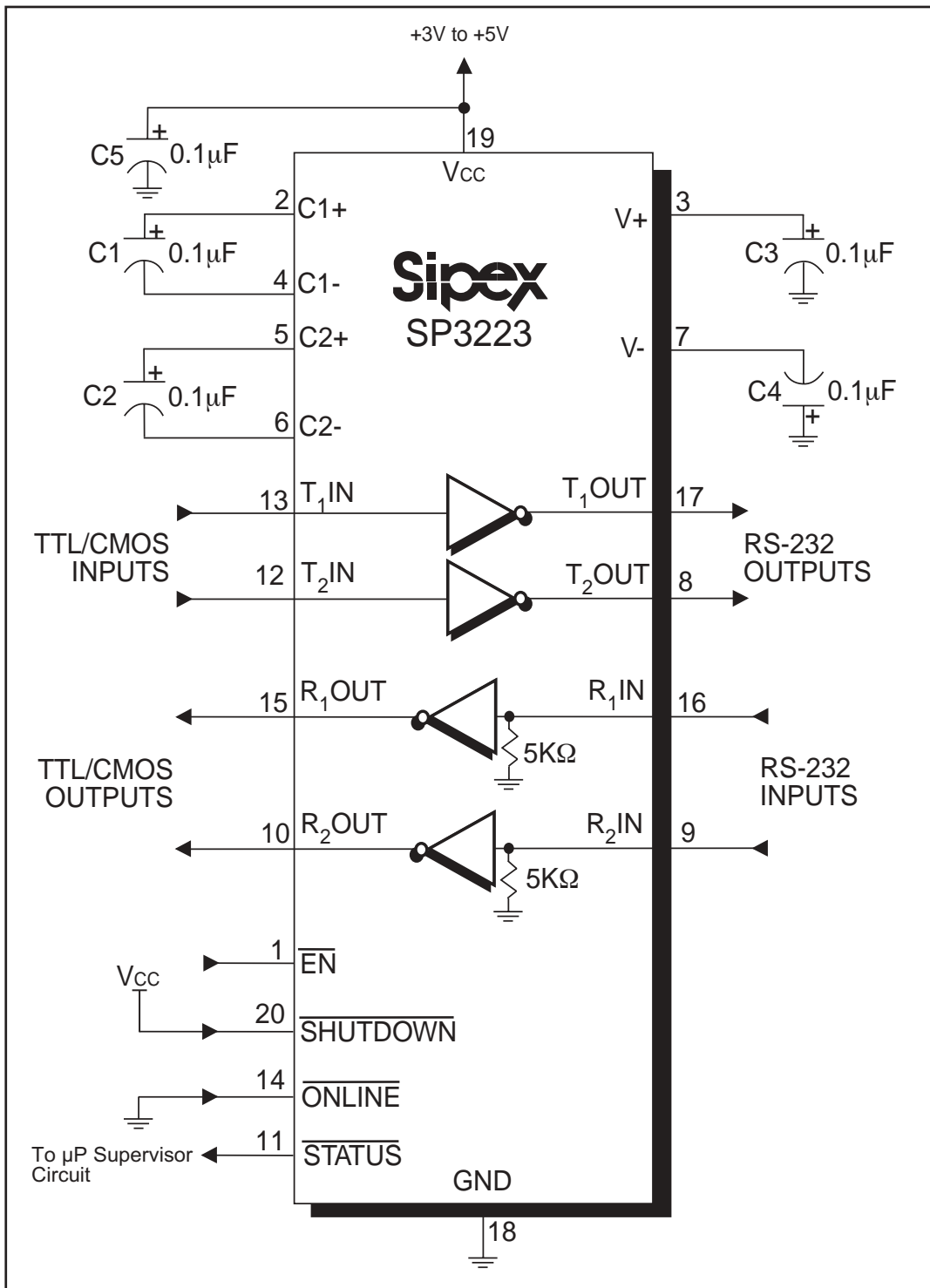


Figure 9. SP3223 Typical Operating Circuit



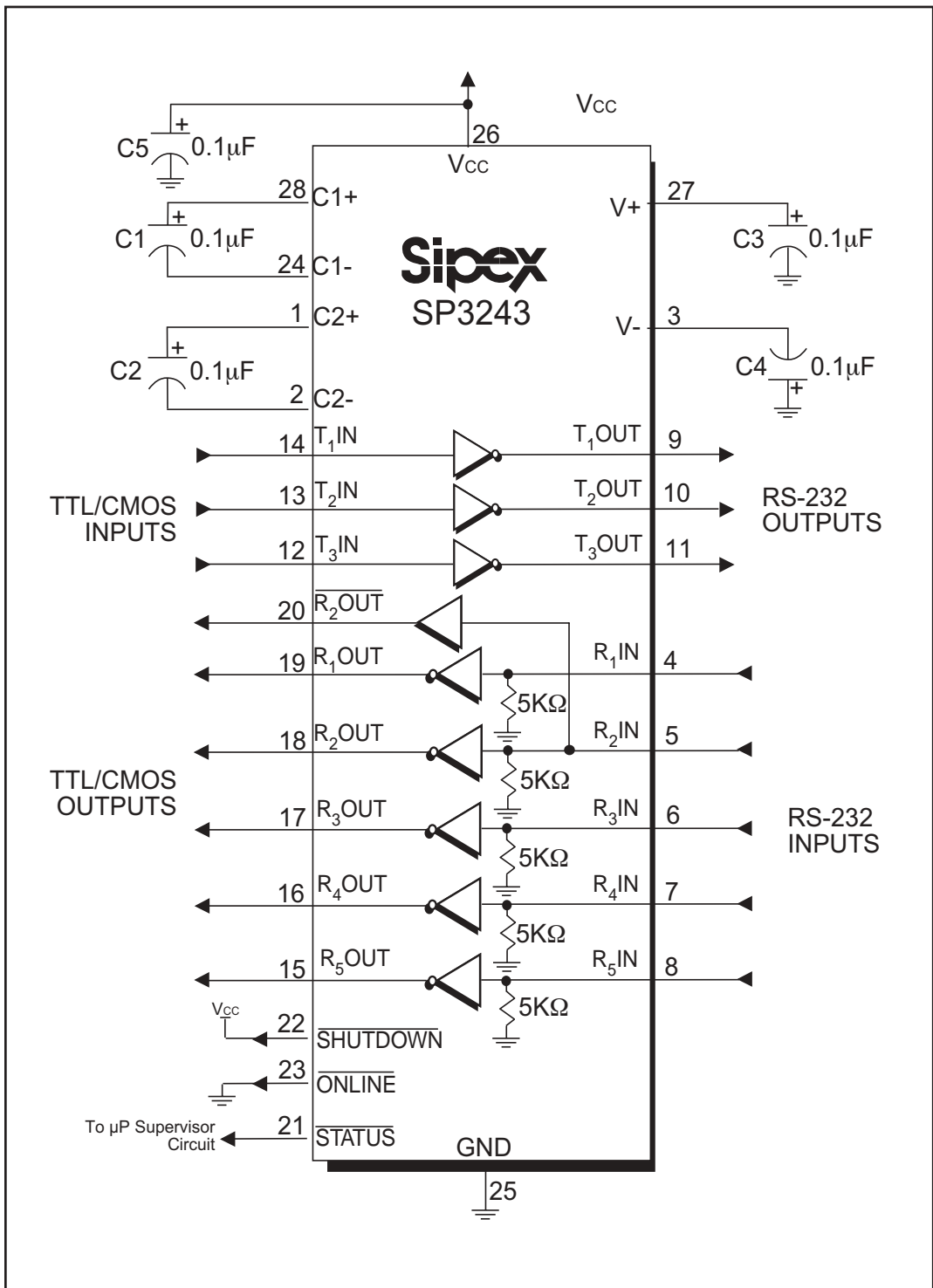
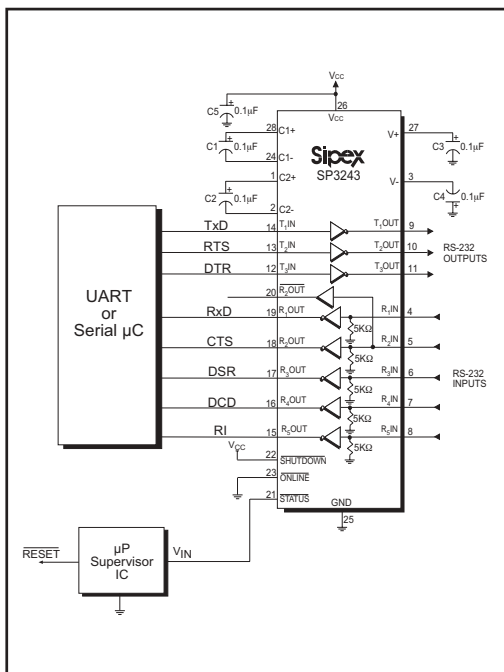


Figure 10. SP3243 Typical Operating Circuit

## DESCRIPTION

The **SP3223** and **SP3243** transceivers meet the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The **SP3223** and **SP3243** devices feature **Sipex's** proprietary and patented (U.S.-- 5,306,954) on-board charge pump circuitry that generates  $\pm 5.5V$  RS-232 voltage levels from a single  $+3.0V$  to  $+5.5V$  power supply. The **SP3223** and **SP3243** devices can operate at a typical data rate of 235kbps fully loaded.

The **SP3223** is a 2-driver/2-receiver device, and the **SP3243** is a 3-driver/5-receiver device ideal for portable or hand-held applications. The **SP3243** includes one complementary always-active receiver that can monitor an external device (such as a modem) in shutdown. This aids in protecting the UART or serial controller IC by preventing forward biasing of the protection diodes where  $V_{CC}$  may be disconnected.



**Figure 11. Interface Circuitry Controlled by Microprocessor Supervisory Circuit**

The **SP3223** and **SP3243** series is an ideal choice for power sensitive designs. The **SP3223** and **SP3243** devices feature **AUTO ON-LINE**<sup>®</sup> circuitry which reduces the power supply drain to a  $1\mu A$  supply current. In many portable or hand-held applications, an RS-232 cable can be disconnected or a connected peripheral can be turned off. Under these conditions, the internal charge pump and the drivers will be shut down. Otherwise, the system automatically comes online. This feature allows design engineers to address power saving concerns without major design changes.

## THEORY OF OPERATION

The **SP3223** and **SP3243** series is made up of four basic circuit blocks:

1. Drivers, 2. Receivers, 3. the Sipex proprietary charge pump, and 4. **AUTO ON-LINE**<sup>®</sup> circuitry.

### Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to  $5.0V$  EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is  $\pm 5.4V$  with no load and  $\pm 5V$  minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. These drivers comply with the EIA-TIA-232F and all previous RS-232 versions. Unused driver inputs should be connected to GND or  $V_{CC}$ .

The drivers can guarantee a data rate of 120Kbps fully loaded with  $3K\Omega$  in parallel with  $1000pF$ , ensuring compatibility with PC-to-PC communication software.

The slew rate of the driver output is internally limited to a maximum of  $30V/\mu s$  in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meets the monotonicity requirements of the standard.

DEVICE: SP3223			
$\overline{\text{SHUTDOWN}}$	$\overline{\text{EN}}$	$T_x\text{OUT}$	$R_x\text{OUT}$
0	0	High Z	Active
0	1	High Z	High Z
1	0	Active	Active
1	1	Active	High Z

DEVICE: SP3243			
$\overline{\text{SHUTDOWN}}$	$T_x\text{OUT}$	$R_x\text{OUT}$	$\overline{R_2\text{OUT}}$
0	High Z	High Z	Active
1	Active	Active	Active

Table 2.  $\overline{\text{SHUTDOWN}}$  and  $\overline{\text{EN}}$  Truth Tables

Note: In *AUTO ON-LINE*® Mode where  $\overline{\text{ONLINE}} = \text{GND}$  and  $\overline{\text{SHUTDOWN}} = V_{CC}$  the device will shut down if there is no activity present at the Receiver inputs.

Figure 12 shows a loopback test circuit used to test the RS-232 Drivers. Figure 13 shows the test results of the loopback circuit with all three drivers active (SP3243) at 120Kbps with typical RS-232 loads in parallel with 1000pF capacitors. Figure 14 shows the test results where one driver was active at 235Kbps and all three drivers loaded with an RS-232 receiver in parallel with a 1000pF capacitor. A solid RS-232 data trans-

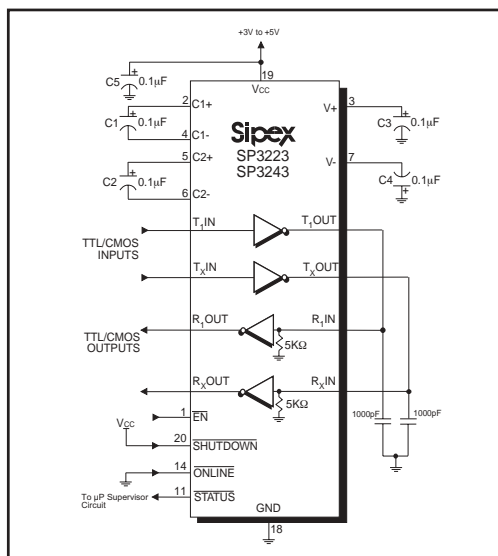


Figure 12. Loopback Test Circuit for RS-232 Driver Data Transmission Rates

mission rate of 120Kbps provides compatibility with many designs in personal computer peripherals and LAN applications.

## Receivers

The receivers convert  $\pm 5.0\text{V}$  EIA/TIA-232 levels to TTL or CMOS logic output levels. Receivers have an inverting output that can be disabled by using the  $\overline{\text{EN}}$  pin.

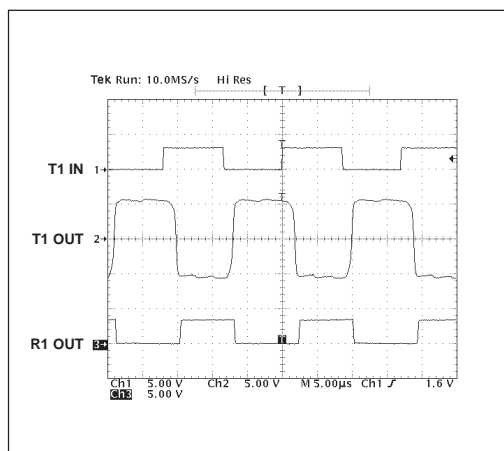


Figure 13. Loopback Test Circuit Result at 120Kbps (All Drivers Fully Loaded)

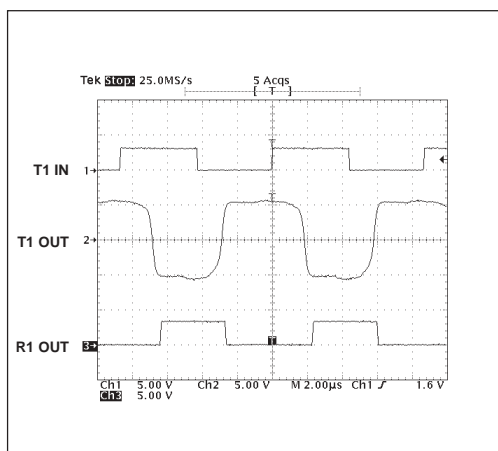


Figure 14. Loopback Test Circuit result at 235Kbps (All Drivers Fully Loaded)

Receivers are active when the *AUTO ON-LINE*<sup>®</sup> circuitry is enabled or when in shutdown. During the shutdown, the receivers will continue to be active. If there is no activity present at the receivers for a period longer than 100 $\mu$ s or when *SHUTDOWN* is enabled, the device goes into a standby mode where the circuit draws 1 $\mu$ A. Driving *EN* to a logic HIGH forces the outputs of the receivers into high-impedance. The truth table logic of the **SP3223** and **SP3243** driver and receiver outputs can be found in *Table 2*.

The **SP3243** includes an additional non-inverting receiver with an output *R<sub>2</sub>OUT*. *R<sub>2</sub>OUT* is an extra output that remains active and monitors activity while the other receiver outputs are forced into high impedance. This allows Ring Indicator (RI) from a peripheral to be monitored without forward biasing the TTL/CMOS inputs of the other devices connected to the receiver outputs.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5K $\Omega$  pulldown resistor to ground will commit the output of the receiver to a HIGH state.

## Charge Pump

The charge pump is a **Sipex**-patented design (U.S. 5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages 5.5V regardless of the input voltage ( $V_{CC}$ ) over the +3.0V to +5.5V range. This is important to maintain compliant RS-232 levels regardless of power supply fluctuations.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

### Phase 1

—  $V_{SS}$  charge storage — During this phase of the clock cycle, the positive side of capacitors  $C_1$  and  $C_2$  are initially charged to  $V_{CC}$ .  $C_1^+$  is then switched to GND and the charge in  $C_1^-$  is transferred to  $C_2^-$ . Since  $C_2^+$  is connected to  $V_{CC}$ , the voltage potential across capacitor  $C_2$  is now 2 times  $V_{CC}$ .

### Phase 2

—  $V_{SS}$  transfer — Phase two of the clock connects the negative terminal of  $C_2$  to the  $V_{SS}$  storage capacitor and the positive terminal of  $C_2$  to GND. This transfers a negative generated voltage to  $C_3$ . This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to  $C_3$ , the positive side of capacitor  $C_1$  is switched to  $V_{CC}$  and the negative side is connected to GND.

### Phase 3

—  $V_{DD}$  charge storage — The third phase of the clock is identical to the first phase — the charge transferred in  $C_1$  produces  $-V_{CC}$  in the negative terminal of  $C_1$ , which is applied to the negative side of capacitor  $C_2$ . Since  $C_2^+$  is at  $V_{CC}$ , the voltage potential across  $C_2$  is 2 times  $V_{CC}$ .

### Phase 4

—  $V_{DD}$  transfer — The fourth phase of the clock connects the negative terminal of  $C_2$  to GND, and transfers this positive generated voltage across  $C_2$  to  $C_4$ , the  $V_{DD}$  storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to  $C_4$ , the positive side of capacitor  $C_1$  is switched to  $V_{CC}$  and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both  $V^+$  and  $V^-$  are separately generated from  $V_{CC}$ , in a no-load condition  $V^+$  and  $V^-$  will be symmetrical. Older charge pump approaches that generate  $V^-$  from  $V^+$  will show a decrease in the magnitude of  $V^-$  compared to  $V^+$  due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 250kHz. The external capacitors can be as low as 0.1 $\mu$ F with a 16V breakdown voltage rating.

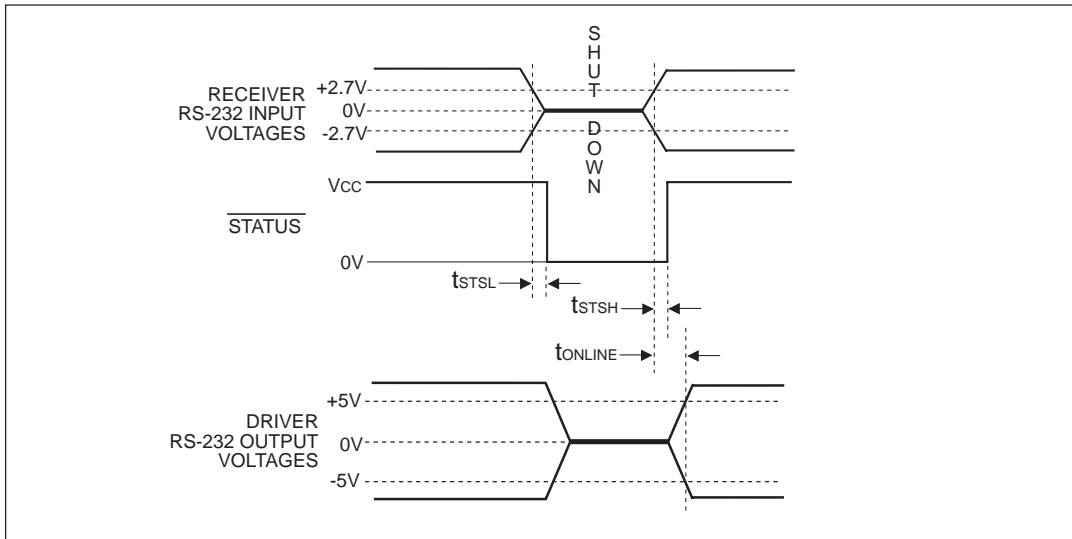


Figure 15. AUTO ON-LINE® Timing Waveforms

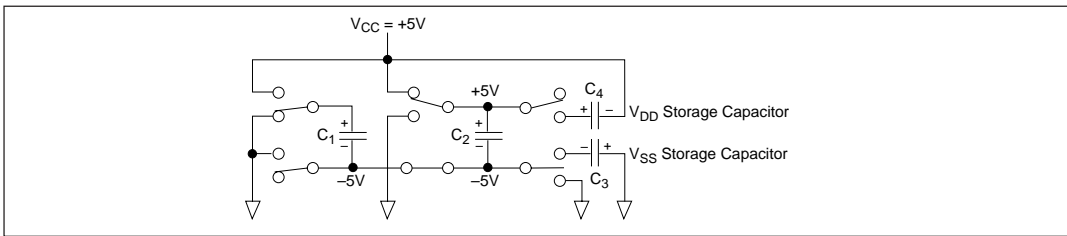


Figure 16. Charge Pump — Phase 1

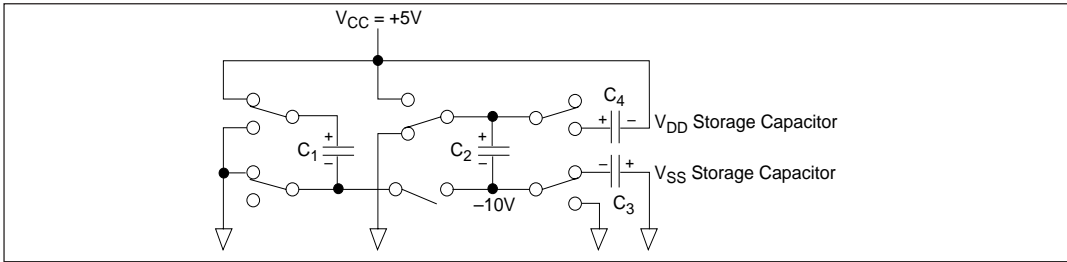


Figure 17. Charge Pump — Phase 2

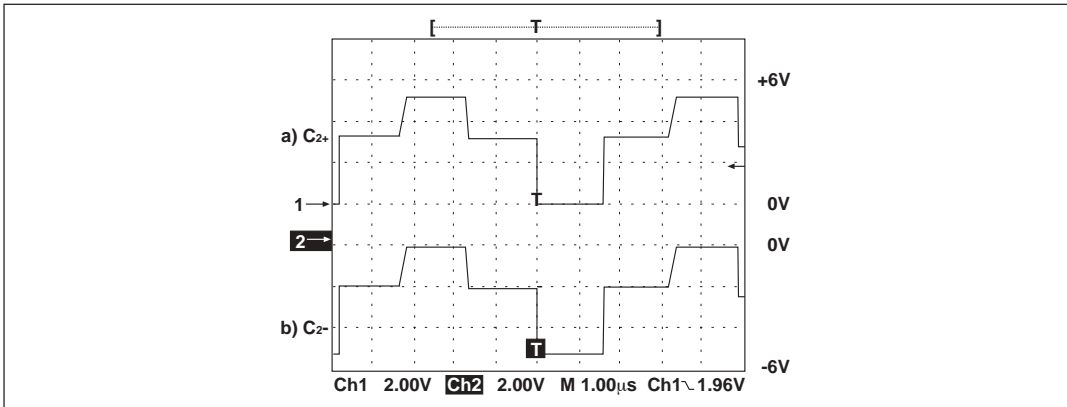


Figure 18. Charge Pump Waveforms

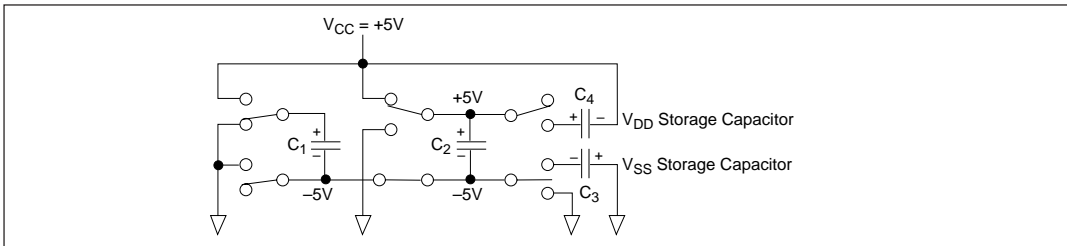


Figure 19. Charge Pump — Phase 3

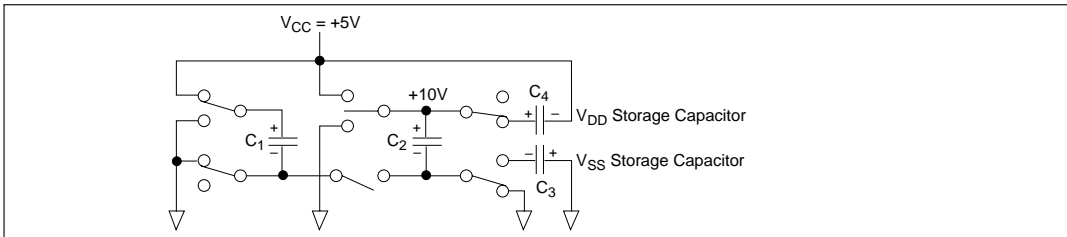


Figure 20. Charge Pump — Phase 4

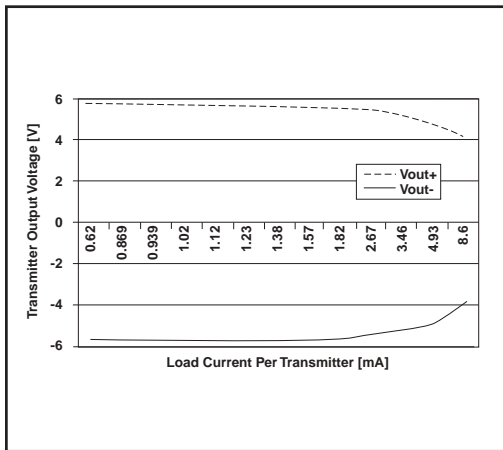


Figure 21. SP3243 Driver Output Voltages vs. Load Current per Transmitter

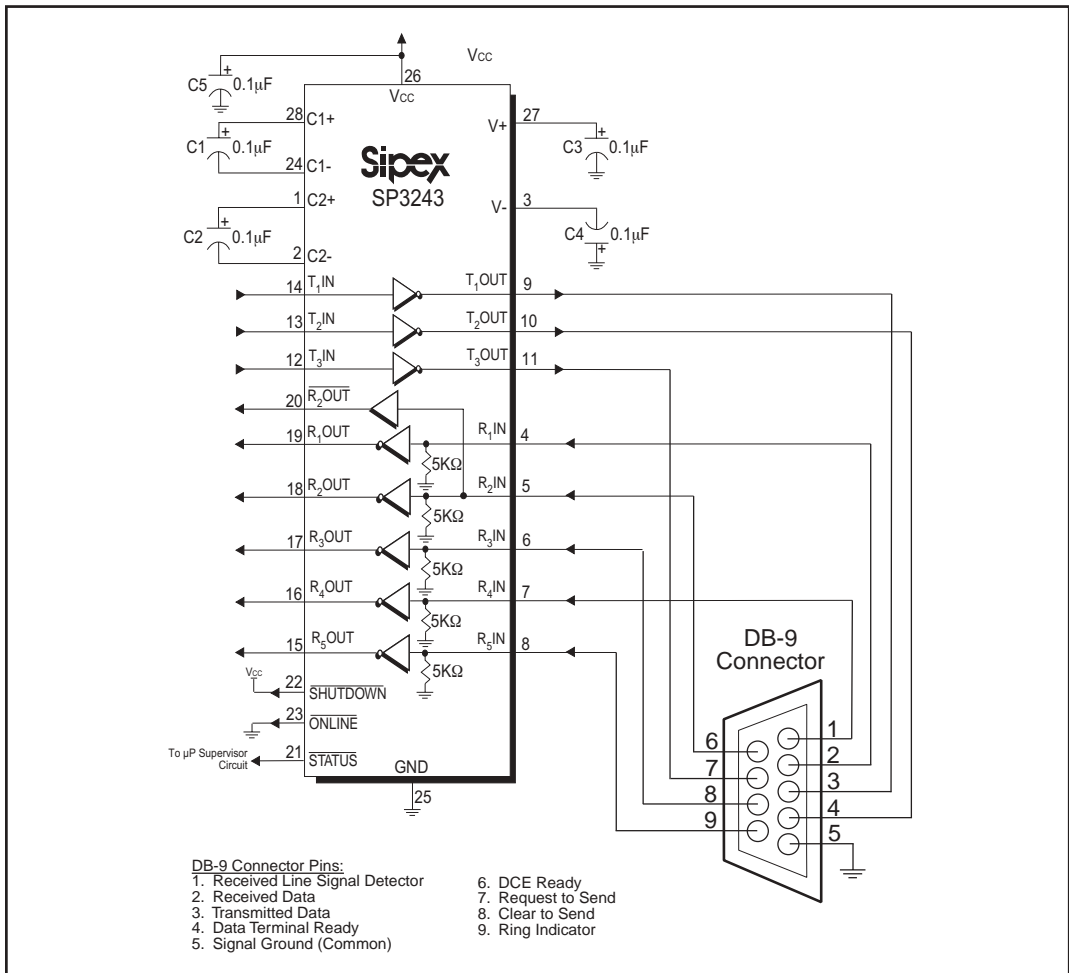


Figure 22. Circuit for the connectivity of the SP3243 with a DB-9 connector

RS-232 SIGNAL AT RECEIVER INPUT	$\overline{\text{SHUTDOWN}}$ INPUT	$\overline{\text{ONLINE}}$ INPUT	$\overline{\text{STATUS}}$ OUTPUT	TRANSCEIVER STATUS
YES	HIGH	LOW	HIGH	Normal Operation (AUTO ON-LINE®)
NO	HIGH	HIGH	LOW	Normal Operation
NO	HIGH	LOW	LOW	Shutdown (AUTO ON-LINE®)
YES	LOW	HIGH/LOW	HIGH	Shutdown
NO	LOW	HIGH/LOW	LOW	Shutdown

Table 3. AUTO ON-LINE® Logic

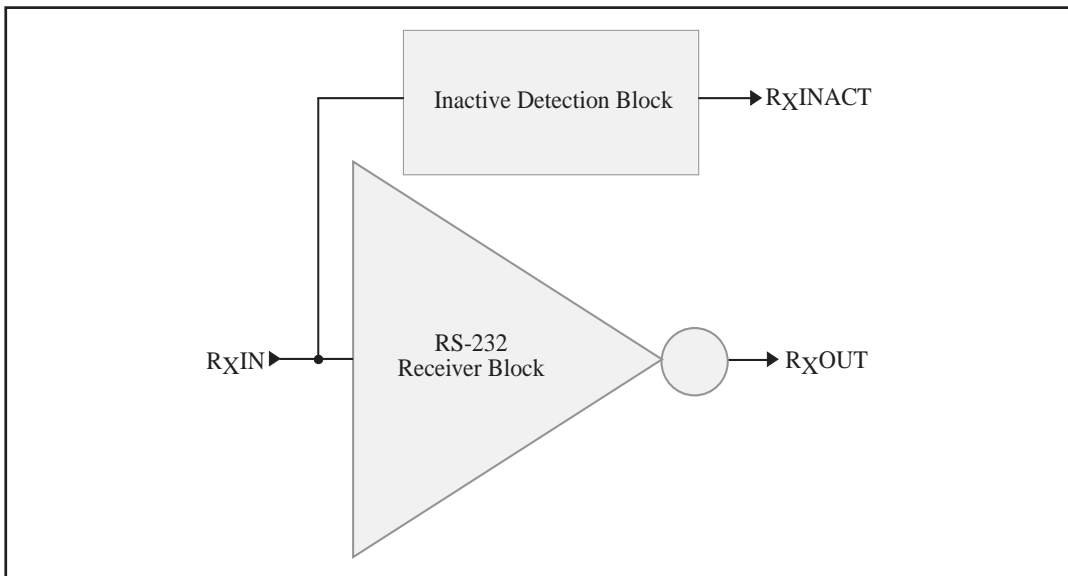


Figure 23. Stage I of AUTO ON-LINE® Circuitry

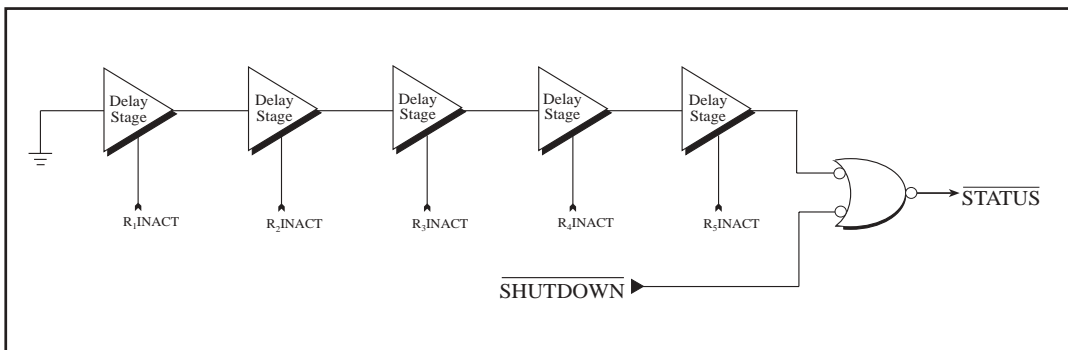


Figure 24. Stage II of AUTO ON-LINE® Circuitry



## AUTO ON-LINE® Circuitry

The **SP3223** and **SP3243** devices have a patent pending **AUTO ON-LINE®** circuitry on board that saves power in applications such as laptop computers, palmtop (PDA) computers, and other portable systems.

The **SP3223** and **SP3243** devices incorporate an **AUTO ON-LINE®** circuit that automatically enables itself when the external transmitters are enabled and the cable is connected. Conversely, the **AUTO ON-LINE®** circuit also disables most of the internal circuitry when the device is not being used and goes into a standby mode where the device typically draws 1 $\mu$ A. This function can also be externally controlled by the **ONLINE** pin. When this pin is tied to a logic LOW, the **AUTO ON-LINE®** function is active. Once active, the device is enabled until there is no activity on the receiver inputs. The receiver input typically sees at least  $\pm 3V$ , which are generated from the transmitters at the other end of the cable with a  $\pm 5V$  minimum. When the external transmitters are disabled or the cable is disconnected, the receiver inputs will be pulled down by their internal 5k $\Omega$  resistors to ground. When this occurs over a period of time, the internal transmitters will be disabled and the device goes into a shutdown or standby mode. When **ONLINE** is HIGH, the **AUTO ON-LINE®** mode is disabled.

The **AUTO ON-LINE®** circuit has two stages:

- 1) Inactive Detection
- 2) Accumulated Delay

The first stage, shown in *Figure 23*, detects an inactive input. A logic HIGH is asserted on **R<sub>X</sub>INACT** if the cable is disconnected or the external transmitters are disabled. Otherwise, **R<sub>X</sub>INACT** will be at a logic LOW. This circuit is duplicated for each of the other receivers.

The second stage of the **AUTO ON-LINE®** circuitry, shown in *Figure 24*, processes all the receiver's **R<sub>X</sub>INACT** signals with an accumulated delay that disables the device to a 1 $\mu$ A supply current.

The **STATUS** pin goes to a logic LOW when the cable is disconnected, the external transmitters are disabled, or the **SHUTDOWN** pin is invoked. The typical accumulated delay is around 20 $\mu$ s.

When the **SP3223** and **SP3243** drivers or internal charge pump are disabled, the supply current is reduced to 1 $\mu$ A. This can commonly occur in hand-held or portable applications where the RS-232 cable is disconnected or the RS-232 drivers of the connected peripheral are turned off.

The **AUTO ON-LINE®** mode can be disabled by the **SHUTDOWN** pin. If this pin is a logic LOW, the **AUTO ON-LINE®** function will not operate regardless of the logic state of the **ONLINE** pin. *Table 3* summarizes the logic of the **AUTO ON-LINE®** operating modes. The truth table logic of the **SP3223** and **SP3243** driver and receiver outputs can be found in *Table 2*.

The **STATUS** pin outputs a logic LOW signal if the device is shutdown. This pin goes to a logic HIGH when the external transmitters are enabled and the cable is connected.

When the **SP3223** and **SP3243** devices are shut down, the charge pumps are turned off. V+ charge pump output decays to V<sub>CC</sub>, the V- output decays to GND. The decay time will depend on the size of capacitors used for the charge pump. Once in shutdown, the time required to exit the shut down state and have valid V+ and V- levels is typically 200 $\mu$ s.

For easy programming, the **STATUS** can be used to indicate DTR or a Ring Indicator signal. Tying **ONLINE** and **SHUTDOWN** together will bypass the **AUTO ON-LINE®** circuitry so this connection acts like a shutdown input pin.

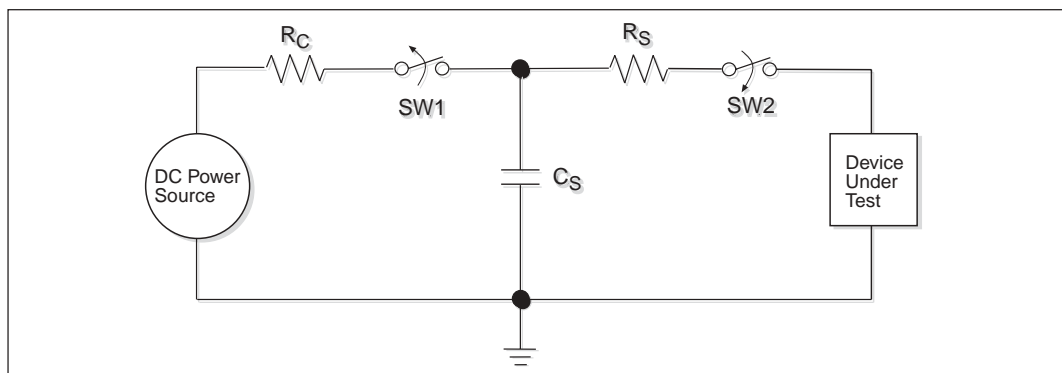
## ESD TOLERANCE

The **SP3223/3243** series incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients.

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of

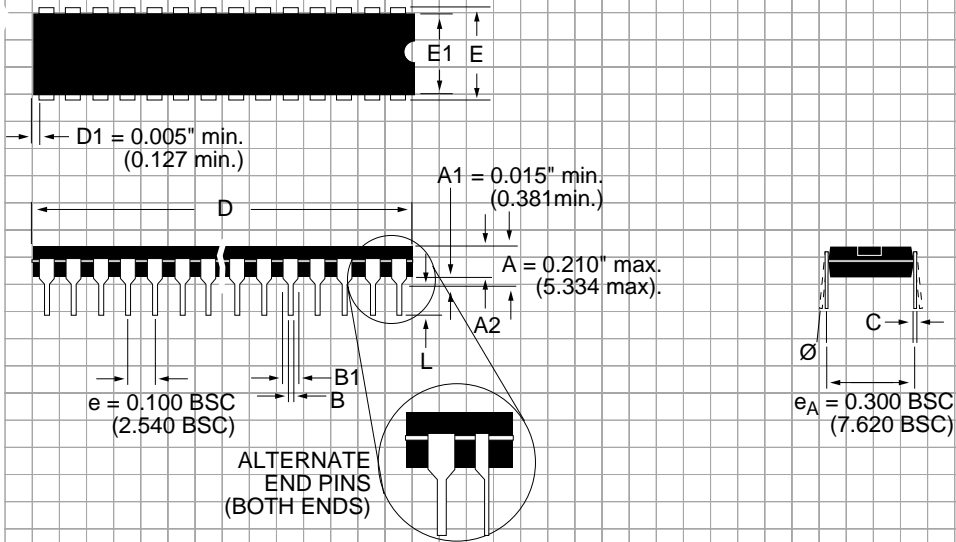
this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in *Figure 25*. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

For the Human Body Model, the current limiting resistor ( $R_s$ ) and the source capacitor ( $C_s$ ) are  $1.5k\Omega$  and  $100pF$ , respectively.



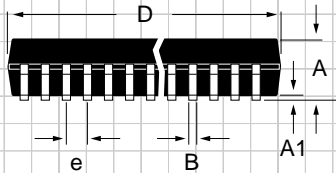
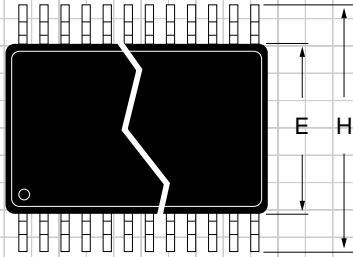
*Figure 25. ESD Test Circuit for Human Body Model*

# PACKAGE: PLASTIC DUAL-IN-LINE (NARROW)



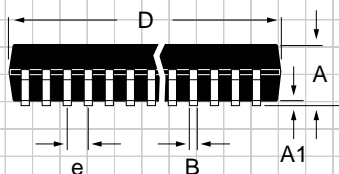
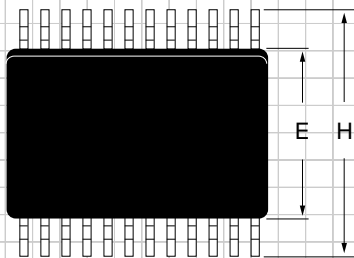
DIMENSIONS (Inches) Minimum/Maximum (mm)	16-PIN	20-PIN	28-PIN
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.068/0.078 (1.73/1.99)
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.002/0.008 (0.05/0.21)
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.010/0.015 (0.25/0.38)
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.397/0.407 (10.07/10.33)
D	0.780/0.800 (19.812/20.320)	0.980/1.060 (24.892/26.924)	0.205/0.212 (5.20/5.38)
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.0256 BSC (0.65 BSC)
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.301/0.311 (7.65/7.90)
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.022/0.037 (0.55/0.95)
$\emptyset$	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/8° (0°/8°)

**PACKAGE: PLASTIC SHRINK  
SMALL OUTLINE  
(SSOP)**



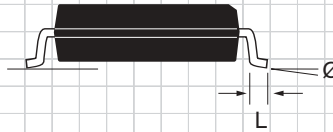
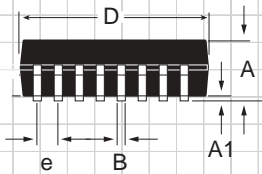
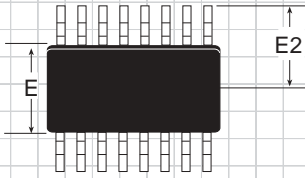
DIMENSIONS (Inches) Minimum/Maximum (mm)	16-PIN	20-PIN	24-PIN	28-PIN
A	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)
A1	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)
B	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)
D	0.239/0.249 (6.07/6.33)	0.278/0.289 (7.07/7.33)	0.317/0.328 (8.07/8.33)	0.397/0.407 (10.07/10.33)
E	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)
e	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)
H	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)
L	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)

**PACKAGE: PLASTIC  
SMALL OUTLINE (SOIC)  
(WIDE)**



DIMENSIONS (Inches) Minimum/Maximum (mm)	28-PIN
A	0.093/0.104 (2.352/2.649)
A1	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)
D	0.697/0.713 (17.70/18.09)
E	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)

# PACKAGE: PLASTIC THIN SMALL OUTLINE (TSSOP)



DIMENSIONS in inches (mm) Minimum/Maximum	
A	- /0.043 (- /1.10)
A1	0.002/0.006 (0.05/0.15)
B	0.007/0.012 (0.19/0.30)
D	0.252/0.260 (6.40/6.60)
E	0.169/0.177 (4.30/4.50)
e	0.026 BSC (0.65 BSC)
E2	0.126 BSC (3.20 BSC)
L	0.020/0.030 (0.50/0.75)
Ø	0°/8°

## ORDERING INFORMATION

Model	Temperature Range	Package Types
SP3223CP	0°C to +70°C	20-pin PDIP
SP3223CA	0°C to +70°C	20-pin SSOP
SP3223CY	0°C to +70°C	20-pin TSSOP
SP3223EP	-40°C to +85°C	20-pin PDIP
SP3223EA	-40°C to +85°C	20-pin SSOP
SP3223EY	-40°C to +85°C	20-pin TSSOP
SP3243CT	0°C to +70°C	28-pin Wide SOIC
SP3243CA	0°C to +70°C	28-pin SSOP
SP3243ET	-40°C to +85°C	28-pin Wide SOIC
SP3243EA	-40°C to +85°C	28-pin SSOP

Please consult the factory for pricing and availability on a Tape-On-Reel option.



ANALOG EXCELLENCE

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