

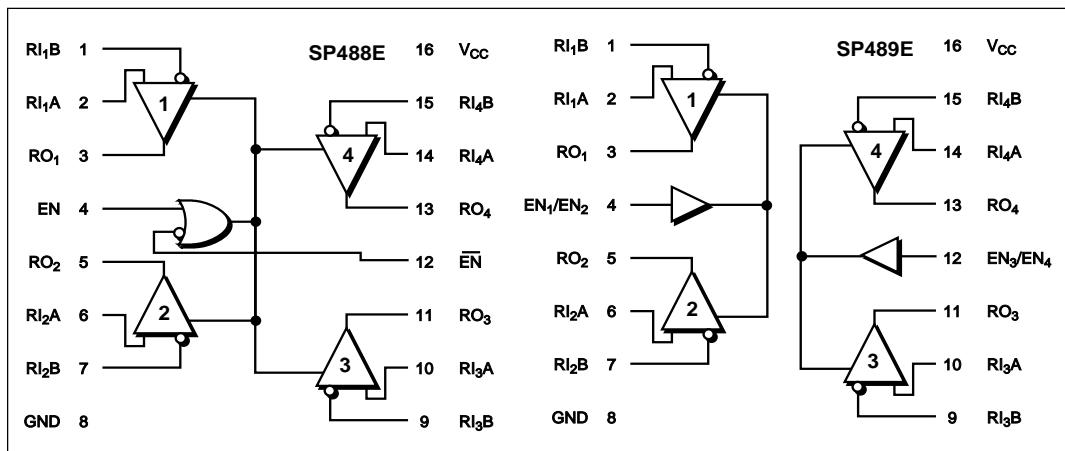
Enhanced Quad RS-485/RS-422 Line Receivers

- RS-485 or RS-422 Applications
- Quad Differential Line Receivers
- Receiver Output Disable
- -7V to +12V Common Mode Input Range
- 1mA Supply Current
- Single +5V Supply Operation
- Superior Drop-in Replacement for SN75173, SN75175, LTC488 and LTC489
- Improved ESD Specifications:
 - ±15kV Human Body Model
 - ±15kV IEC1000-4-2 Air Discharge
 - ±8kV IEC1000-4-2 Contact Discharge



DESCRIPTION...

The **SP488E** and **SP489E** are low-power quad differential line receivers that meet the specifications of RS-485 and RS-422 serial protocols with enhanced ESD performance. The ESD tolerance has been improved on these devices to over ±15kV for both Human Body Model and IEC1000-4-2 Air Discharge Method. These devices are superior drop-in replacements to Sipex's **SP488** and **SP489** devices as well as popular industry standards. As with the original versions, the **SP488E** features a common receiver enable control and the **SP489E** provides independent receiver enable controls for each pair of receivers. Both feature wide common-mode input ranges. The receivers have a fail-safe features which forces a logic "1" output when receiver inputs are left floating. Both are available in 16-pin plastic DIP and SOIC packages.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC}	+7V
Input Voltages		
Logic	-0.5V to (V_{CC} + 0.5V)
Receiver	±14V
Receiver Output Voltage	-0.5V to (V_{CC} + 0.5V)
Input Currents		
Logic	±25mA
Storage Temperature	-65°C to +150°C
Power Dissipation		
Plastic DIP	375mW (derate 7mW/°C above +70°C)
Small Outline	375mW (derate 7mW/°C above +70°C)
Lead Temperature (soldering, 10 sec)	300°C

SPECIFICATIONS

$V_{CC} = 5V \pm 5\%$; typicals at 25°C; $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DC CHARACTERISTICS					
Digital Inputs					
Voltage					
V_{IL}	2.0		0.8	Volts	$EN, \overline{EN}, EN_1/EN_2, EN_3/EN_4$
V_{IH}			±2	Volts	
Input Current				µA	$0V \leq V_{IN} \leq V_{CC}$
RECEIVER INPUTS					
Input Resistance	12			kOhm	$-7V \leq V_{CM} \leq 12V$
Differential Input Threshold	-0.2		+0.2	Volts	$-7V \leq V_{CM} \leq 12V$
Input Current (A, B)				mA	$V_{CC} = 0V$ or 5.25V; I_{IN2}
Maximum Data Rate	10		+1.0 -0.8	mA	$V_{IN} = +12V$
				Mbps	$V_{IN} = -7V$
RECEIVER OUTPUTS					
Output Voltage				V	
V_{OH}	3.5		0.4	V	$I_O = -4mA; V_{ID} = +0.2V$
V_{OL}			±1	µA	$I_O = +4mA; V_{ID} = -0.2V$
High Impedance Output Current					$0.4V \leq V_O \leq 2.4V,$ $EN = \emptyset, EN = 1,$ $EN_1/EN_2 = EN_3/EN_4 = \emptyset$
POWER REQUIREMENTS					
Supply Voltage	4.75	5.00	5.25	Volts	
Supply Current		1	5	mA	No load
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
-C	0		+70	°C	
-E	-40		+85	°C	
Storage Temperature			+150	°C	
Package					
$-P$	16-pin Plastic DIP				
$-T$	16-pin SOIC				

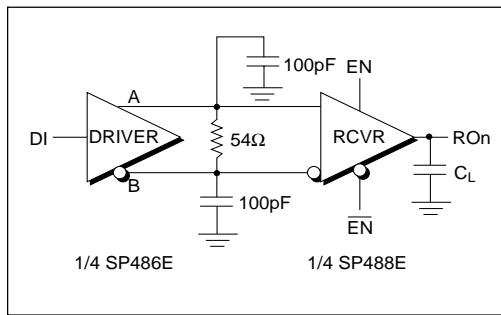


Figure 1. Timing Test Circuit

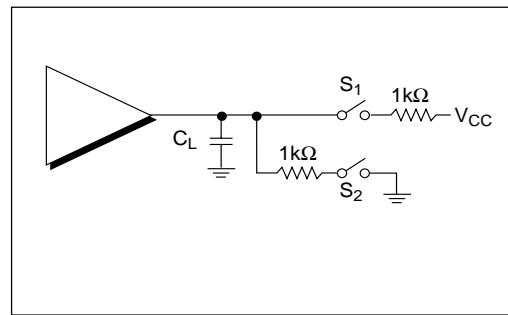


Figure 2. Enable/Disable Timing Test Circuit

SP488 PINOUT

Pin 1 — RI₁B — Receiver 1 input B.

Pin 2 — RI₁A — Receiver 1 input A.

Pin 3 — RO₁ — Receiver 1 Output — If Receiver 1 output is enabled, if RI₁A > RI₁B by 200mV, Receiver output is high. If Receiver 1 output is enabled, and if RI₁A < RI₁B by 200mV, Receiver 1 output is low.

Pin 4 — EN — Receiver Output Enable. Please refer to **SP488E Truth Table (1)**.

Pin 5 — RO₂ — Receiver 2 Output — If Receiver 2 output is enabled, if RI₂A > RI₂B by 200mV, Receiver 2 output is high. If Receiver 2 output is enabled, and if RI₂A < RI₂B by 200mV, Receiver 2 output is low.

Pin 6 — RI₂A — Receiver 2 input A.

Pin 7 — RI₂B — Receiver 2 input B.

Pin 8 — GND — Digital Ground.

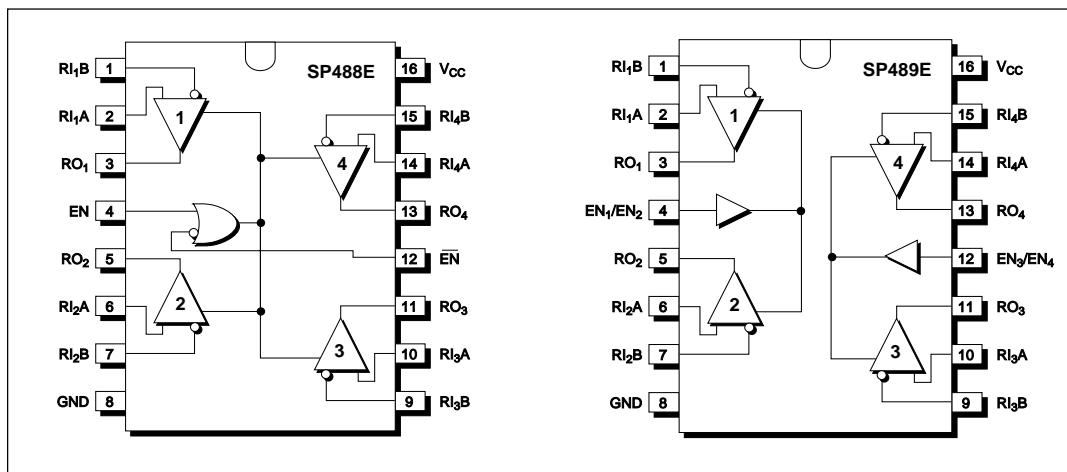
Pin 9 — RI₃B — Receiver 3 input B.

Pin 10 — RI₃A — Receiver 3 input A.

Pin 11 — RO₃ — Receiver 3 Output — If Receiver 3 output is enabled, if RI₃A > RI₃B by 200mV, Receiver 3 output is high. If Receiver 3 output is enabled, and if RI₃A < RI₃B by 200mV, Receiver 3 output is low.

Pin 12 — $\overline{\text{EN}}$ — Receiver Output Enable. Please refer to **SP488E Truth Table (1)**.

PINOUT



Pin 13 — RO_4 — Receiver 4 Output — If Receiver 4 output is enabled, if $RI_4A > RI_4B$ by 200mV, Receiver 4 output is high. If Receiver 4 output is enabled, and if $RI_4A < RI_4B$ by 200mV, Receiver 4 output is low.

Pin 14 — RI_4A — Receiver 4 input A.

Pin 15 — RI_4B — Receiver 4 input B.

Pin 16 — Supply Voltage V_{CC} — $4.75V \leq V_{CC} \leq 5.25V$.

SP489E PINOUT

Pin 1 — RI_1B — Receiver 1 input B.

Pin 2 — RI_1A — Receiver 1 input A.

Pin 3 — RO_1 — Receiver 1 Output — If Receiver 1 output is enabled, if $RI_1A > RI_1B$ by 200mV, Receiver output is high. If Receiver 1 output is enabled, and if $RI_1A < RI_1B$ by 200mV, Receiver 1 output is low.

Pin 4 — $EN1/EN2$ — Receiver 1 and 2 Output Enable. Please refer to **SP489E Truth Table (2)**.

Pin 5 — RO_2 — Receiver 2 Output — If Receiver 2 output is enabled, if $RI_2A > RI_2B$ by 200mV, Receiver 2 output is high. If Receiver 2 output is enabled, and if $RI_2A < RI_2B$ by 200mV, Receiver 2 output is low.

Pin 6 — RI_2A — Receiver 2 input A.

Pin 7 — RI_2B — Receiver 2 input B.

Pin 8 — GND — Digital Ground.

DIFFERENTIAL	ENABLES		OUTPUT
A — B	EN	\overline{EN}	RO
$V_{ID} \geq 0.2V$	H X	X L	H H
$-0.2V < V_{ID} < +0.2V$	H X	X L	X X
$V_{ID} \leq -0.2V$	H X	X L	L L
X	L	H	Hi-Z

Table 1. SP488E Truth Table

Pin 9 — RI_3B — Receiver 3 input B.

Pin 10 — RI_3A — Receiver 3 input A.

Pin 11 — RO_3 — Receiver 3 Output — If Receiver 3 output is enabled, if $RI_3A > RI_3B$ by 200mV, Receiver 3 output is high. If Receiver 3 output is enabled, and if $RI_3A < RI_3B$ by 200mV, Receiver 3 output is low.

Pin 12 — $EN3/EN4$ — Receiver 3 and 4 Output Enable. Please refer to **SP489E Truth Table (2)**.

Pin 13 — RO_4 — Receiver 4 Output — If Receiver 4 output is enabled, if $RI_4A > RI_4B$ by 200mV, Receiver 4 output is high. If Receiver 4 output is enabled, and if $RI_4A < RI_4B$ by 200mV, Receiver 4 output is low.

Pin 14 — RI_4A — Receiver 4 input A.

Pin 15 — RI_4B — Receiver 4 input B.

Pin 16 — Supply Voltage V_{CC} — $4.75V \leq V_{CC} \leq 5.25V$.

FEATURES...

The **SP488E** and **SP489E** are low-power quad differential line receivers meeting RS-485 and RS-422 standards. The **SP488E** features active high and active low common receiver enable controls; the **SP489E** provides independent, active high receiver enable controls for each pair of receivers. Both feature tri-state outputs and a -7V to +12V common-mode input range permitting a $\pm 7V$ ground difference between devices on the communications bus. The **SP488E/489E** are equipped with a fail-safe feature which forces a logic high at the receiver output when the input is left floating. Data rates up to 10Mbps are supported. Both are available in 16-pin plastic DIP and SOIC packages.

DIFFERENTIAL	ENABLES	OUTPUT
A — B	EN_1/EN_2 or EN_3/EN_4	RO
$V_{ID} \geq 0.2V$	H	H
$-0.2V < V_{ID} < +0.2V$	H	X
$V_{ID} \leq -0.2V$	H	L
X	L	Hi-Z

Table 2. SP489E Truth Table

AC PARAMETERS

$V_{cc} = 5V \pm 5\%$; typicals at $25^\circ C$; $T_{AMB} = 25^\circ C$ unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
PROPAGATION DELAY					
Receiver Input to Output Low to HIGH (t_{PLH})		45	60	ns	$C_L = 15pF$; Figure 1, 3
High to LOW (t_{PLH})		45	60	ns	
Differential Receiver Skew (t_{SKD})		5	60	ns	$t_{SKD} = t_{PHL} - t_{PLH} $
RECEIVER ENABLE					
To Output HIGH		30	60	ns	$C_L = 15pF$; Figures 2 and 4 (S2 closed)
To Output LOW		35	60	ns	$CL = 15pF$; Figures 2 and 4 (S1 closed)
RECEIVER DISABLE					
From Output LOW		35	60	ns	$CL = 15pF$; Figures 2 and 4 (S1 closed)
From Output HIGH		30	60	ns	$CL = 15pF$; Figures 2 and 4 (S2 closed)

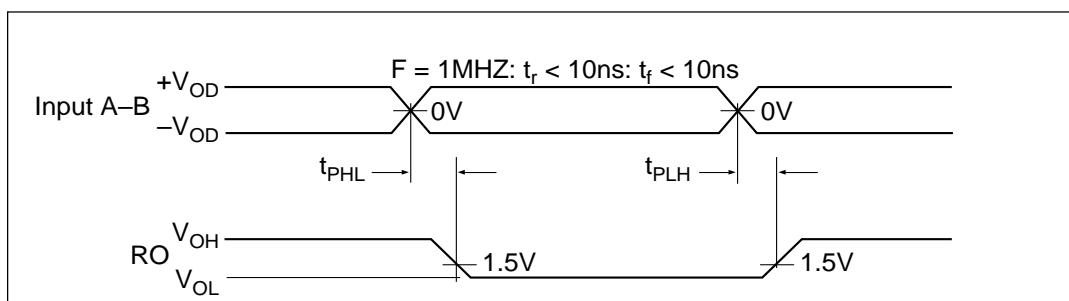


Figure 3. Receiver Propagation Delays

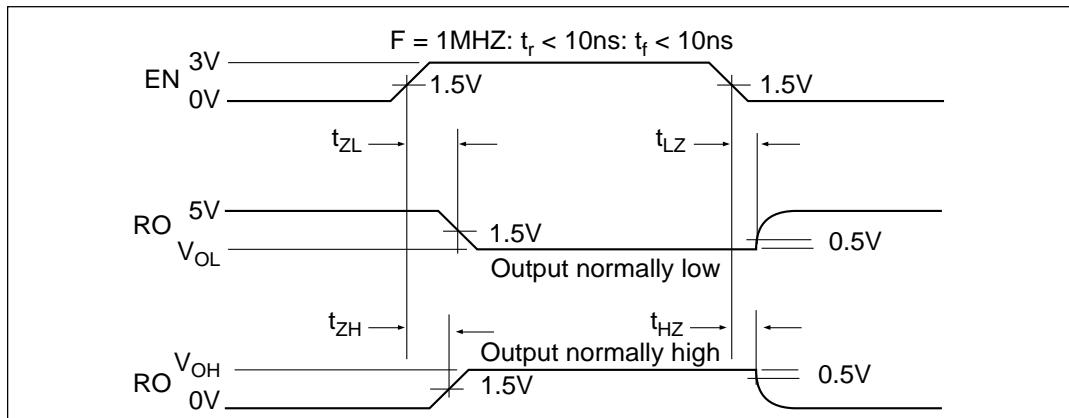


Figure 4. Receiver Enable/Disable Timing

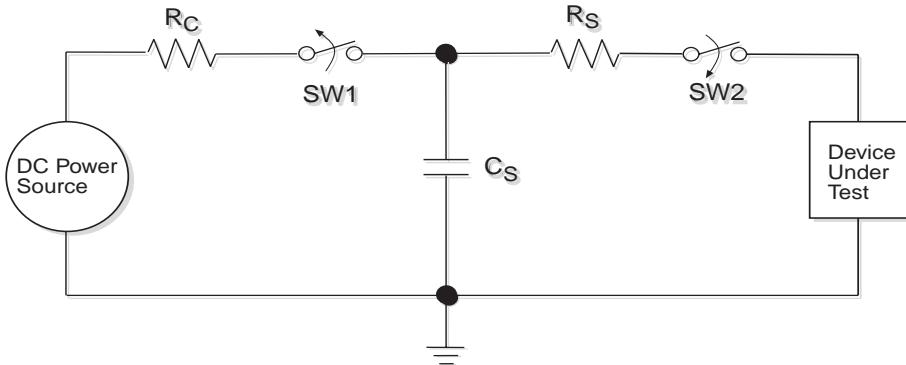


Figure 5. ESD Test Circuit for Human Body Model

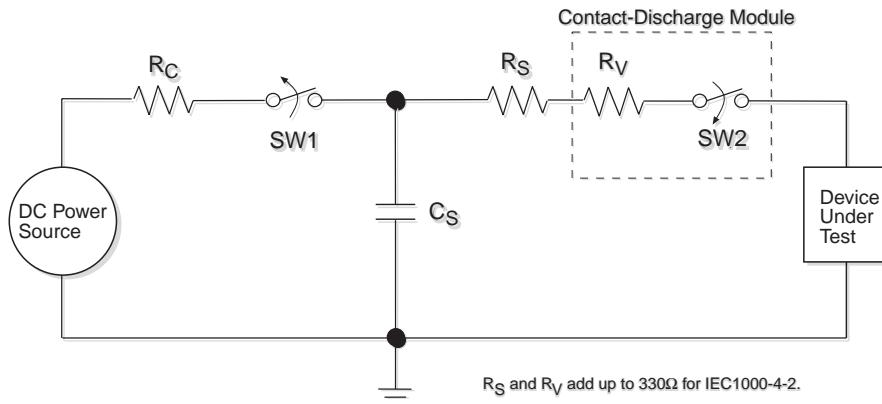


Figure 6. ESD Test Circuit for IEC1000-4-2

ESD TOLERANCE

The **SP488E** and **SP489E** devices incorporate ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least $\pm 15\text{kV}$ without damage nor latch-up.

There are different methods of ESD testing applied:

- a) MIL-STD-883, Method 3015.7
- b) IEC1000-4-2 Air-Discharge
- c) IEC1000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in *Figure 5*. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-1000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside

environment and human presence. The premise with IEC1000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC1000-4-2 is shown on *Figure 6*. There are two methods within IEC1000-4-2, the Air Discharge method and the Contact Discharge method.

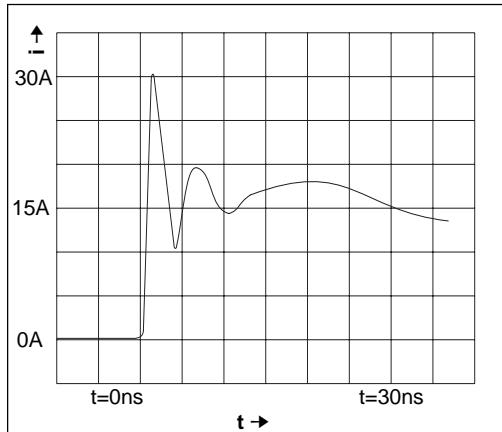


Figure 7. ESD Test Waveform for IEC1000-4-2

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD

potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as handheld systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

The circuit model in *Figures 5 and 6* represent the typical ESD testing circuit used for all three methods. The C_s is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_s , the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

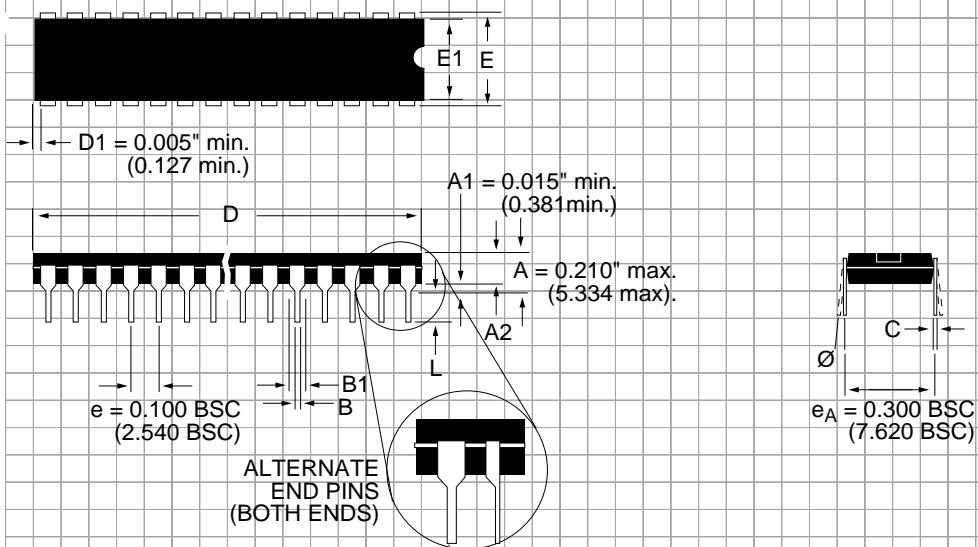
For the Human Body Model, the current limiting resistor (R_s) and the source capacitor (C_s) are 1.5kW an 100pF, respectively. For IEC-1000-4-2, the current limiting resistor (R_s) and the source capacitor (C_s) are 330W an 150pF, respectively.

The higher C_s value and lower R_s value in the IEC1000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

DEVICE PIN TESTED	HUMAN BODY MODEL	IEC1000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	$\pm 15kV$	$\pm 15kV$	$\pm 8kV$	4
Receiver Inputs	$\pm 15kV$	$\pm 15kV$	$\pm 8kV$	4

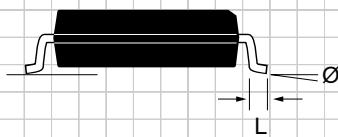
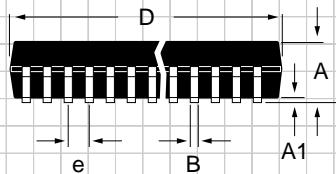
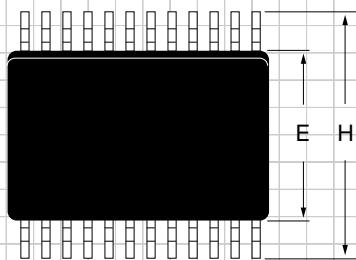
Table 3. Transceiver ESD Tolerance Levels

PACKAGE: PLASTIC DUAL-IN-LINE (NARROW)



DIMENSIONS (Inches) Minimum/Maximum (mm)	16-PIN
A2	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)
D	0.780/0.800 (19.812/20.320)
E	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)
Ø	0°/15° (0°/15°)

PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (WIDE)



DIMENSIONS (Inches) Minimum/Maximum (mm)		16-PIN
A	0.093/0.104 (2.352/2.649)	
A1	0.004/0.012 (0.102/0.300)	
B	0.013/0.020 (0.330/0.508)	
D	0.398/0.413 (10.10/10.49)	
E	0.291/0.299 (7.402/7.600)	
e	0.050 BSC (1.270 BSC)	
H	0.394/0.419 (10.00/10.64)	
L	0.016/0.050 (0.406/1.270)	
Ø	0°/8° (0°/8°)	

ORDERING INFORMATION

Quad RS485 Receivers:

Model	Enable/Disable	Temperature Range	Package
SP488ECP	Common; active Low and Active High ..	0°C to +70°C	16-pin Plastic DIP
SP488ECT	Common; active Low and Active High ..	0°C to +70°C	16-pin SOIC
SP488EEP	Common; active Low and Active High ..	-40°C to +85°C	16-pin Plastic DIP
SP488EET	Common; active Low and Active High ..	-40°C to +85°C	16-pin SOIC
SP489ECP	One per driver pair; active High ..	0°C to +70°C	16-pin Plastic DIP
SP489ECT	One per driver pair; active High ..	0°C to +70°C	16-pin SOIC
SP489EEP	One per driver pair; active High ..	-40°C to +85°C	16-pin Plastic DIP
SP489EET	One per driver pair; active High ..	-40°C to +85°C	16-pin SOIC

Please consult the factory for pricing and availability on a Tape-On-Reel option.



SIGNAL PROCESSING EXCELLENCE

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