HARRIS Semiconductor

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PART WITHDRAWN
PROCESS OBSOLETE
NO NEW DESIGNS

Features

- Maximum Rating 500V
- Ability to Interface and Drive Standard and Current Sensing N-Channel Power MOSFET/IGBT Devices
- Creation and Management of a Floating Power Supply for Upper Rail Drive
- Simultaneous Conduction Lockout
- Overcurrent Protection
- Single Low Current Bias Supply Operation
- Latch Immune CMOS Logic
- Peak Drive in Excess of 0.5A

Half Bridge 500VDC Driver

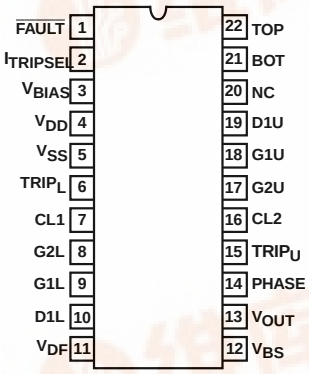
The SP600 is a smart power high voltage integrated circuit (HVIC) optimized to drive MOS gated power devices in half-bridge topologies. It provides the necessary control and management for PWM motor drive, power supply, and UPS applications.

Ordering Information

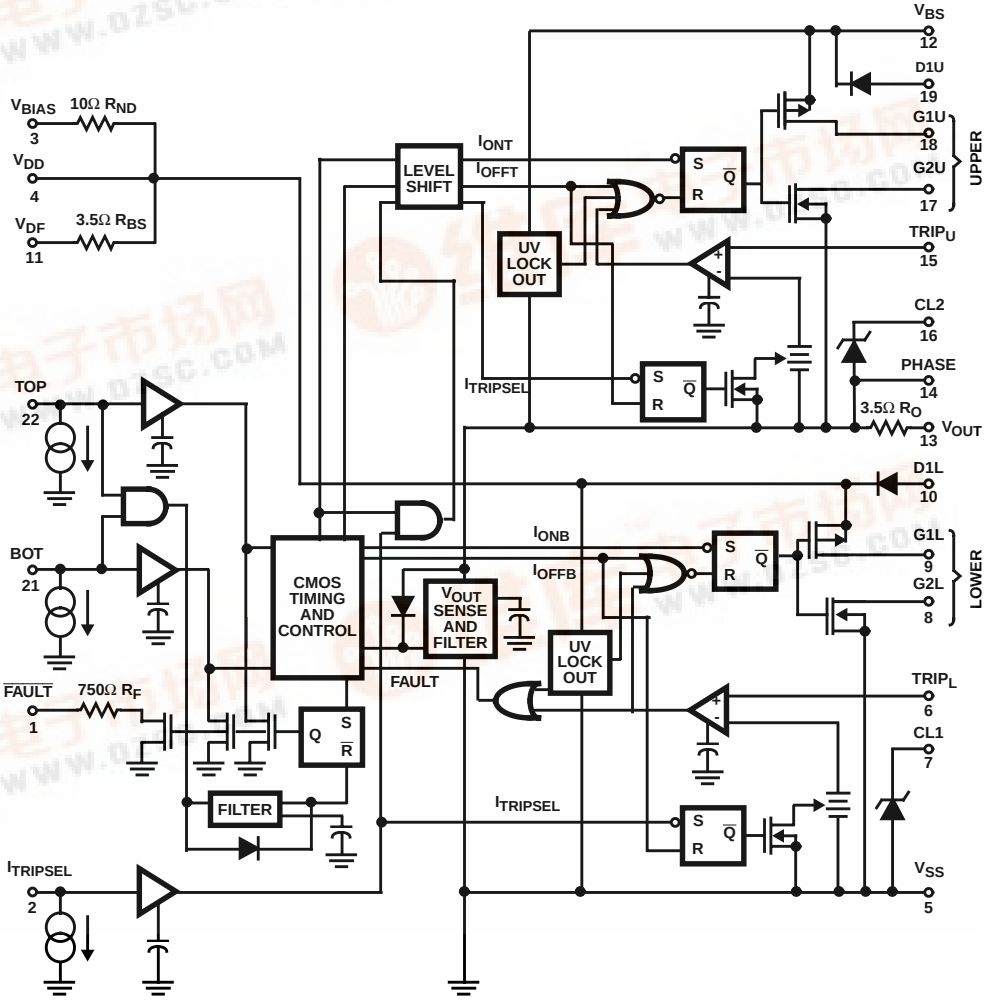
PART	TEMPERATURE	PACKAGE
SP600	-40°C to +85°C	22 Lead Plastic DIP

Pinout

SP600 (PDIP)
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings

Full Temperature Range, All Voltage Referenced to V_{SS} Unless Otherwise Noted. Note 1, Note 2.

Low Voltage Power Supply, V_{BIAS} (Note 1) . . . . . $18V_{DC}$
Floating Low Voltage Boot Strap . . . . . $18V_{DC}$
Power Supply to Phase, V_{BS}
Low Voltage Signal Pins
Fault, $I_{TRIPSEL}$, V_{DD}, $TRIP_L$, CL1, G2L . . . $-0.5V_{DC}$ to V_{DD} +0.5
G1L, D1L, V_{DF}, TOP, BOT
CL2, $TRIP_U$, G1U, G2U, D1U to Phase. . . . -0.5_{VDC} to V_{BS} +0.5
High Voltage Pins
Phase, V_{PHASE} . . . . . $500V_{DC}$
(V_{BS}, V_{OUT}, $TRIP_U$, CL2, G2U and D1U: 0V-18V Higher Than Phase)
Dynamic High Voltage Rating Phase, ... 10,000V/µs
$DV_{PHASE/DT}$

Thermal Information

Thermal Resistance θ_{JA}
Plastic DIP Package . . . . . $75^oC/W$
Maximum Package Power Dissipation at $T_A = +85^oC$, P_O
Plastic DIP Package 500mW
Operating Ambient Temperature Range, T_A . . . . . -25^oC to $+85^oC$
Storage Temperature Range, T_S. . . . . -40^oC to $+150^oC$
Lead Temperature (Soldering 10s) . . . . . $+265^oC$

NOTES:

1. Care must be taken in the application of V_{BIAS} as not to impose high peak dissipation demands on a relatively small metallized noise dropping resistor (R_{ND}). Prolonged high peak currents may result if $+15V_{DC}$ is applied abruptly and/or if the local bypass capacitor C_{DD} is large. It is suggested that C_{DD} be ≤ 10MFD. If it is desirable to switch the $15V_{DC}$ source or if a C_{DD} is larger, additional series impedance may be required.
2. Consult factory for additional package offerings.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

(V_{BIAS} = 15V, Pulsed <300ms), Unless Otherwise Noted, All Parameters Referenced to V_{SS} Except $TRIP_U$, CL2, G1U, D1U, and V_{BS} Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Input Current (5V < V_{TOP}, V_{BOT}, $V_{TRIPSEL}$ < 15V)	I_{IN}	+25°C	-	20	30	µA
		-40°C to +85°C	-	30	33	µA
I_{BIAS} Quiescent Current (All Inputs Low)	I_{BIAS_L}	+25°C	-	1.7	2.05	mA
		-40°C to +85°C	-	1.7	2.1	mA
I_{BIAS} Quiescent Current ($V_{OUT} \geq V_{BIAS}$, and All Inputs Low)	I_{BIAS_H}	+25°C	-	1.7	2.05	mA
		-40°C to +85°C	-	1.7	2.1	mA
I_{BS} Quiescent Current Bootstrap Supply	I_{BS}	+25°C	-	875	1000	µA
		-40°C to +85°C	-	900	1060	µA
TOP Threshold Level	V_{TOP}	+25°C	7	8	9	V
		-40°C to +85°C	6.95	8	9.1	V
BOTTOM Threshold Level	V_{BOT}	+25°C	7	8	9	V
		-40°C to +85°C	6.9	8	9.1	V
Current TRIPSELECT Threshold Level	$V_{TRIPSEL}$	+25°C	7	8	9	V
		-40°C to +85°C	6.95	8	9.1	V
Trip Lower and Upper Comparator Threshold Level - Normal ($I_{TRIPSEL} = V_{SS}$)	$V_{TRIP\ L/U_N}$	+25°C	90	105	125	mV
		-40°C to +85°C	90	105	127	mV
Trip Lower and Upper Comparator Threshold Level - Boost ($I_{TRIPSEL} = V_{DD}$) % of Measured $V_{TRIP\ L/U_N}$	$V_{TRIP\ L/U_B}$	+25°C	110	130	150	%
		-40°C to +85°C	109	130	152	%
Under Voltage Lockout Thresholds (V_{DD} and V_{BS})	V_{LOCK}	+25°C	9	10	11.5	V
		-40°C to +85°C	9.7	10.5	11.8	V
Phase Out of Status Voltage Threshold (PHASE)	V_{OSVT}	+25°C	5	7	9	V
		-40°C to +85°C	4.7	7	9.6	V

Electrical Specifications

(V_{BIAS} = 15V, Pulsed <300ms), Unless Otherwise Noted, All Parameters Referenced to V_{SS} Except $TRIP_U$, CL2, G1U, D1U, and V_{BS} Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE **(Continued)**

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Faultbar Impedance at I_{FBAR} = 1mA	RF	+25°C	500	760	1000	Ω
		-40°C to +85°C	450	760	1100	Ω
Upper/Lower Source Impedances (I_{SOURCE} = 10mA)	$R_{SO\ L/U}$	+25°C	12	17	23	Ω
		-40°C to +85°C	7	17	29	Ω
Upper/Lower Sink Impedances (I_{SINK} = 10mA)	$R_{SI\ L/U}$	+25°C	8	12	16	Ω
		-40°C to +85°C	5	12	20	Ω
Bootstrap Supply Current Limiting Impedance	R_{BS}	+25°C	2	3.5	5	Ω
		-40°C to +85°C	1.4	3.5	5.6	Ω
Noise Dropping Resistor Impedance	R_{ND}	+25°C	6	10	14	Ω
		-40°C to +85°C	5.4	10	14.6	Ω
High Voltage Leakage (500V V_{BS}, V_{OUT}, PHASE, $TRIP_U$, CL2, G1U, G2U, and D1U to V_{SS}. All other Pins at V_{SS})	I_{LK}	+25°C	-	1	3	µA
Miller Clamp Diodes; D1U and D1L (I_D = 10mA)	$V_{D1U/L}$	+25°C	0.40	0.90	1.40	V
Noise Clamping Zeners; CL2 and CL1 (I_Z = 10mA)	$V_{CL2/1\text{-}LOW}$	+25°C	6.35	6.61	6.85	V
		-40°C to +85°C	6.15	6.61	7.15	V
Noise Clamping Zeners; CL2 and CL1 (I_Z = 50mA)	$V_{CL2/1\text{-}HIGH}$	+25°C	7.0	8.5	8.0	V
V_{OUT} Limiting Resistance	R_O	+25°C	2	3.5	5	Ω
		-40°C to +85°C	1.4	3.5	5.6	Ω

NOTE: Maximum Steady State ÷ 15V_{DC} Supply Current = I_{BIAS_L} ÷ I_{BS}

Switching Specifications

(All Referenced to V_{SS}, Except: $TRIP_U$, Cl2, G1U, G2U, and D1U Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE)

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Refresh One Shot Timer	t_{REF}	+25°C	200	350	500	µs
		-40°C to +85°C	180	350	540	µs
Delay Time of Trip I/U Voltage ($I_{TRIPSEL}$ low) to G2U/G2L Low (50% Overdrive)	$t_{OFF_{TN}}$	+25°C	2	3	4	µs
		-40°C to +85°C	1.85	3	4.35	µs
Delay Time of Trip I Voltage ($I_{TRIPSEL}$ low) to Faultbar Low	t_{FN}	+25°C	2	3	4	µs
		-40°C to +85°C	1.85	3	4.35	µs
Delay Time of Phase Out of Status to Faultbar Low (TOP High)	t_{OSVF}	+25°C	500	700	900	ns
		-40°C to +85°C	400	700	1050	ns
Minimum Logic Input Pulse Width: TOP and BOTTOM	t_{MINIW}	+25°C	300	430	600	ns
		-40°C to +85°C	275	430	660	ns
Minimum G1U/G1L On Time	t_{ON}	+25°C	1.6	2.3	3.1	µs
		-40°C to +85°C	1.5	2.4	3.4	µs
Minimum Pulsed Off Time, G2U/G2L	t_{OFF}	+25°C	1.3	2.0	3.4	µs
		-40°C to +85°C	1.05	2.1	3.9	µs
Turn On Delay Time of G1U (BISTATE MODE)	t_{ON_D}	+25°C	2.5	3.2	4.5	µs
		-40°C to +85°C	2.1	3.3	5.2	µs

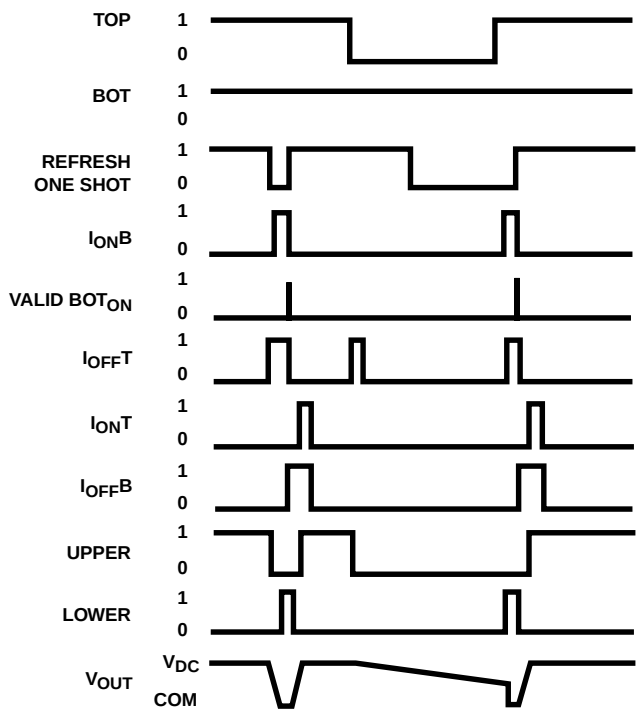
Switching Specifications (All Referenced to V_{SS}, Except: $TRIP_U$, Cl2, G1U, G2U, and D1U Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE) **(Continued)**

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Turn On Delay Time of G1L (BISTATE MODE)	t_{ON_D}	+25°C	2.5	3.2	4.5	µs
		-40°C to +85°C	2.1	3.3	5.2	µs
Turn On Delay Time of G1U (THREE-STATE MODE)	t_{ON_D}	+25°C	0.75	1.0	1.5	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Turn On Delay Time of G1L (THREE-STATE MODE)	t_{ON_D}	+25°C	0.75	1.0	1.5	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Turn Off Delay Time of G2U and G2L	t_{OFF_D}	+25°C	0.75	1.0	1.45	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Minimum Dead Time: G1U off to G1L on, or G1L off to G1U on (BISTATE MODE)	$t_{D.T.}$	+25°C	1.5	2.5	3.5	µs
		-40°C to +85°C	1.2	2.6	4	µs
Fault Reset Delay to Clear Faultbar	$t_{R.T.}$	+25°C	3.4	4.5	6.6	µs
		-40°C to +85°C	3.15	4.8	7.4	µs
Rise Time of Upper and Lower Driver (Load = 2000pF)	$t_{R\ U/L}$	+25°C	25	50	100	ns
		-40°C to +85°C	15	50	115	ns
Fall Time of Upper and Lower Driver (Load = 2000pF)	$t_{F\ U/L}$	+25°C	25	50	100	ns
		-40°C to +85°C	15	50	115	ns

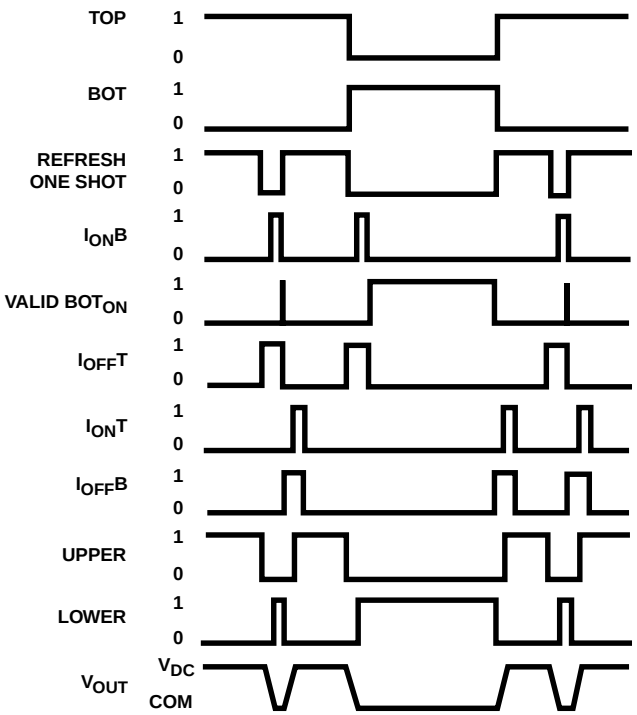
Recommended Operating Conditions and Functional Pin Description (All Voltages Referenced to V_{SS}, Unless Otherwise Noted. See Figure 1)

PARAMETER	CONDITION
FAULTBAR	Open Drain Fault Indicator Output
$I_{TRIPSELECT}$	Digital Input Command to Increase $TRIP_L$ and $TRIP_U$ Threshold by 30%
V_{BIAS}	14.5V to 16.5V with 15V nominal, ≅ 1.5mA DC BIAS Current
V_{DD}	C_{DD} to V_{SS}
V_{SS}	COMMON
TRIP I	100mV Signal to Shut Off LOWER Drive and Trigger a Fault Output
CL1	Lower Noise Clamp Zener
G2L and G1L	Low Impedance Driver Designed to Drive Power MOS Transistors (LOWER)
V_{DF}	Current Limiting Charging Resistor for Bootstrap Capacitor Power Supply
V_{BS}	Bootstrap Supply, Normally a Diode Drop Below V_{DD} Voltage with Respect to the Floating PHASE Reference
V_{OUT}	Load Connection Node
PHASE	Floating Reference Point for High Side Control Circuitry: V_{BS}, $TRIP_U$, CL2, G1U, G2U and D1U
$TRIP_U$	100mV Signal, Referenced to PHASE, to Shut Off UPPER Drive
CL2	Upper Noise Clamp Zener
G2U and G1U	Low Impedance Driver Designed to Drive Power MOS Transistors (UPPER)
TOP	Digital Input to Command the UPPER On
BOT	Digital Input to Command the LOWER On
D1U	Miller Clamp UPPER to V_{BS}
D1L	Miller Clamp LOWER to V_{DD}

Timing Diagram



THREE-STATE MODE SLOWER THAN REFRESH ONE SHOT TIMER



BISTATE MODE SLOWER THAN REFRESH ONE SHOT TIMER

NOTE: BOT switching not relevant.

Typical Circuit Configuration

TRUTH TABLE

Applicable to Typical Circuit Configuration (Figure 1)

INPUTS						OUTPUTS		
TOP	BOT	$TRIP_L$	$TRIP_U$	PHASE	V_{BIAS}	UPPER	LOWER	FAULT BAR
0	0	0	X	X	1	0	0	1
1	1	0	0	1	1	1	0	1
1	1	0	1	1	1	0	0	0
1	1	0	X	0	1	0	0	0
X	X	1	X	X	1	0	0	0
0	1	0	X	X	1	0	1	1
1	0	0	X	X	1	0	0	1
X	X	X	X	X	0	0	0	0

NOTE: 0 = False, 1 = True, X = Don't Care

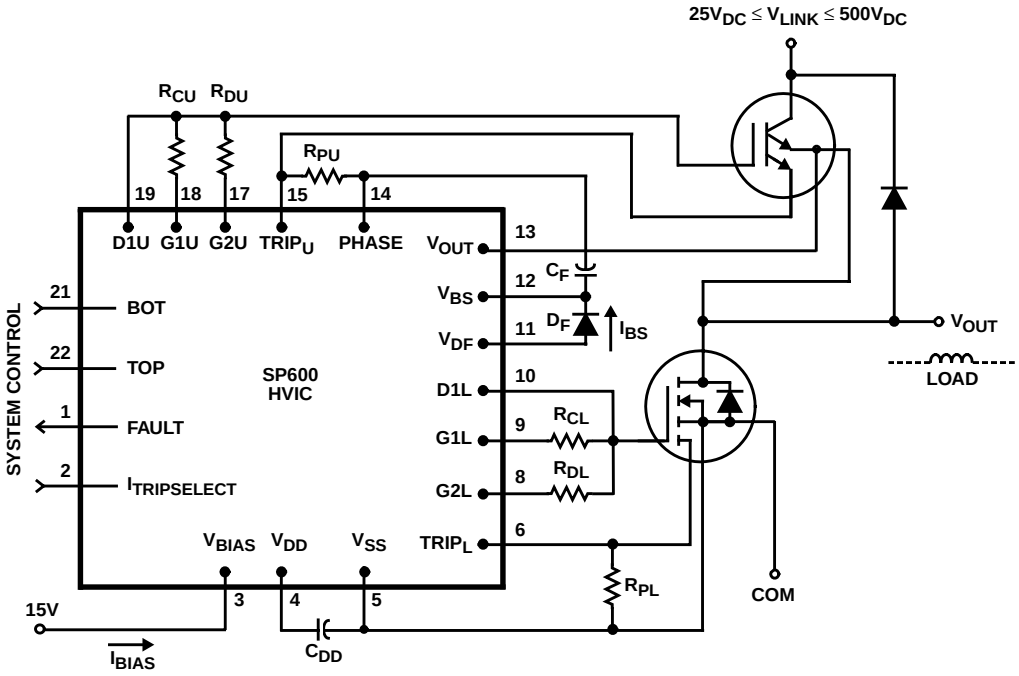


FIGURE 1. TYPICAL CIRCUIT CONFIGURATION

LEGEND		
Application Specific	R_{CU}	Upper Gate Charging Resistor
Application Specific	R_{DU}	Upper Gate Discharge Resistor
Application Specific	R_{PU}	Upper Current Pilot Resistor
Application Specific	R_{CL}	Lower Gate Charging Resistor
Application Specific	R_{DL}	Lower Gate Discharging Resistor
Application Specific	R_{PL}	Lower Current Pilot Resistor
3µF at ≥ 15DC	C_{DD}	Local LV Filter Capacitor
0.22µF Ceramic X7R at ≥ $15V_{DC}$	C_F	Flying Capacitor for Bootstrap Supply
Harris P/N A114M or Equiv PRV ≥ V_{LINK}	D_F	Flying Diode for Bootstrap Supply

NOTE: Refer to ‘Additional Product Offerings’ for information concerning power output devices.

Functional Description

The SP600 provides a flexible, digitally controlled power function which is intended to be used as PWM drivers of N-Channel MOSFETs and/or IGBTs for up to 240VAC line rectified totem-pole applications. The CMOS driveable inputs are filtered and captured by the control logic to determine the output state. The logic includes fixed timing to prohibit simultaneous conduction of the external power switches and, thru the V_{OUT} sense detector, verifies the output voltage state is in agreement with the controlled inputs. The >11V_{DC} floating power supply required to drive the upper rail external power device is created and managed by the HVIC through C_F and D_F. This capacitor is refreshed from the V_{DD} supply each time V_{OUT} goes low. If the upper channel is commanded on for a long period of time, the bootstrap capacitor CF is automatically refreshed by bringing V_{OUT} low. This is accomplished by turning off the upper rail MOSFET/IGBT, momentarily turning on the lower rail output device, followed by returning control back to the upper switch. Otherwise, C_F would gradually deplete its charge allowing the upper switch to come out of saturation. The upper and lower gate drivers allow for controlled charge and discharge rates as well as facilitate the use of nearly lossless current sensing power MOS devices. The over current trip level can be boosted 30% on a pulse by pulse basis by logic level '1' applied to $I_{TRIPSELECT}$. A $\overline{FAULT}$ output signal is generated when any of the following occurs:

V bias is low
Over current is detected
V phase doesn't agree with the input signal

Reset of $\overline{FAULT}$ is provided by externally removing power or by holding both TOP and BOT inputs low for the required reset time (trt_{MAX}).

Each application can be individually optimized by the selection of external components tailored to ensure proper overall system operation including:

Determining the ratings and sizing of MOSFETs and IGBTs, mixed or matched, as well as flyback diodes (FBD).

The selection of separate gate charge (R_C) and discharge (R_D) impedance chosen per the load capacitance, frequency of operation, and D_I/D_T dependent recovery characteristics of the associated FBDs. R_D should also be sized to prevent simultaneous bridge conduction by ensuring gate discharge in the allotted turn off pulse width ($t_{OFF\ MIN}$).

The selection of over current detection resistors (R_P), compatible with current sense MOSFETs/IGBTs or shunt(s) may be used.

For the floating bootstrap supply D_F and C_F must be determined. D_F must support the worse case system bus voltage and handle the charging currents of C_F. Proper selection should take into consideration T_{RR} and T_{FR} per the desired operating frequency. Proper selection of C_F is a trade off between the minimum t_{ON} time of the lower rail to charge up the capacitor, the amount of charge transfer required by the load, and cost. Due to automatic refresh the capacitor is replenished every 350µs TYP (or even sooner if input commands the TOP to switch at a faster repetition rate).

The local filter capacitor (C_{DD}) should be sized sufficiently large enough to transfer the charge to C_F without causing a significant droop in V_{DD}. As a rule of thumb it should be at least 10 times larger than C_F and be located adjacent to the V_{DD} and V_{SS} pins to minimize series resistance and inductance.

Refer to Application Note AN8829 for more details about module operation and selection of external components.