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SP8607 600MHz÷2

The SP8607 is an emitter coupled logic divider which features ECL10K compatible outputs when used with external pulldown resistors. The inputs are AC coupled.

FEATURES

- ECL Compatible Outputs
- AC-Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 80mW
- Temperature Range:
 - -55°C to +125°C (A Grade) -30°C to +70°C (B Grade)

OUTPUT OUTPUT OF A 3 O OUTPUT OF A 3 OUTPUT OF A 4 OUTPUT OF

Fig. 1 Pin connections - bottom view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{EE} -8VOutput current 10mAStorage temperature range $-65^{\circ}C$ to $+150^{\circ}C$ Max. junction temperature $+175^{\circ}C$ Max. clock input voltage 2.5V p-p

ORDERING INFORMATION

SP8607 A CM SP8607 B CM SP8607 AC CM

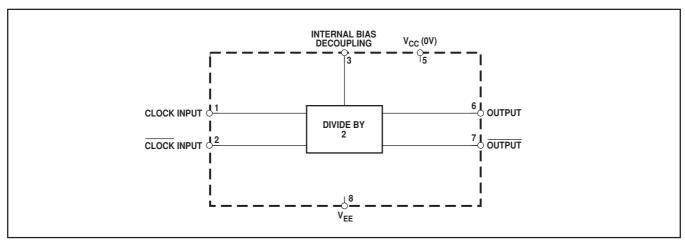


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range Supply voltage, V_{CC} = 0V, V_{EE} = $-5\cdot2V\pm0\cdot25V$ Temperature, T_{AMB} = -55° C to $+125^{\circ}$ C (A Grade), -30° C to $+70^{\circ}$ C (B Grade)

Characteristic	Symbol	Value				Notes
		Min.	Max.	Units	Conditions	Notes
Maximum frequency (sinewave input)	f _{MAX}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f _{MIN}		40	MHz	Input = 400-800mV p-p	
Power supply current	I _{EE}		18	mA	$V_{EE} = -5.2V$, outputs unloaded	
Output low voltage	V _{OL}	−1.8	-1.4	V	$V_{EE} = -5.2V$	3
Output high voltage	V _{OH}	-0.85	-0.7	V	$V_{EE} = -5.2V$	3
Minimum output swing	V _{OUT}	400		mV	$V_{EE} = -5.2V$	

- The temperature coefficients of V_{OH} = +1·63mV/°C, and V_{OL} = +0·34mV/°C but these are not tested.
 The test configuration for dynamic testing is shown in Fig.5.
 Tested at 25°C only.

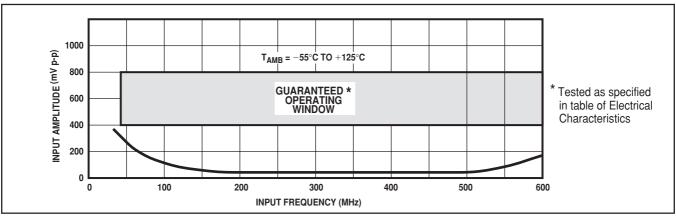


Fig. 3 Typical input characteristic of SP8607A

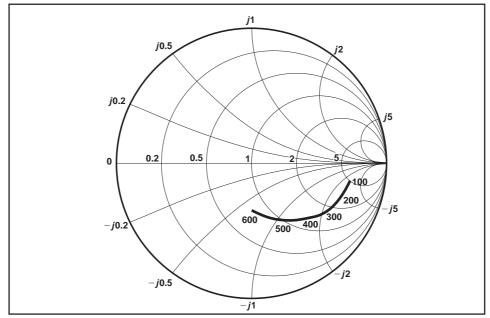


Fig. 4 Typical input impedance. Test conditions: supply voltage = -5.2V, ambient temperature = 25°C, frequencies in MHz, Impedances normalised to 50Ω

OPERATING NOTES

- 1. The clock inputs (pins 1 and 2) can be driven single ended or differentially and should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 3, to ground. 2. In the absence of a signal the device will self-oscillate. If this is undesirable, it may be prevented by connecting a $15 \mathrm{k}\Omega$ resistor from the unused input to V_{EE} . This will reduce the input sensitivity by approximately $100 \mathrm{mV}$.
- 3. The circuit will operate down to DC but slew rate must be better than $100V/\mu s$.
- 4. The outputs are compatible with ECLII. There is an internal load of $4k\Omega$ on each output. The outputs can be interfaced to ECL10K by the addition of 1-5k Ω pulldown resistors from the outputs to V_{EE} to increase output voltage swing.
- 5. Input impedance is a function of frequency, See Fig. 4.
- 6. All components should be suitable for the frequency in use.

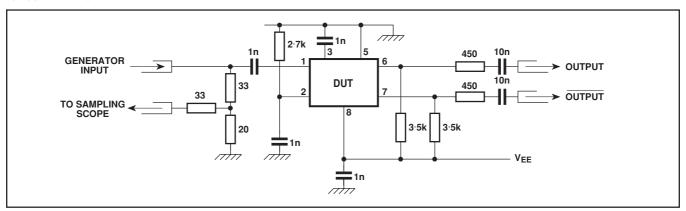


Fig. 5 Test circuit

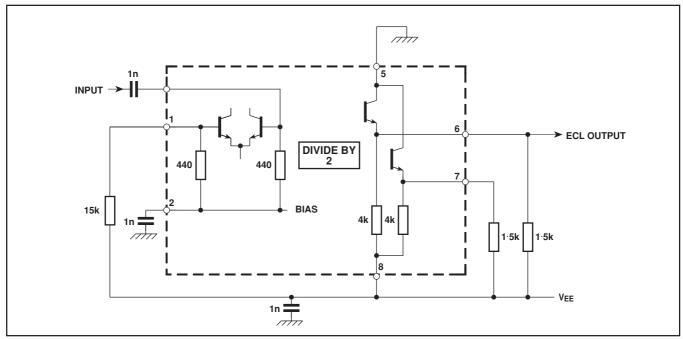
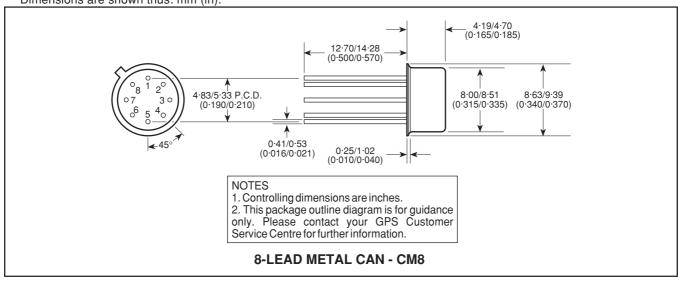


Fig. 6 Typical application showing interfacing

PACKAGE DETAILS

Dimensions are shown thus: mm (in).





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