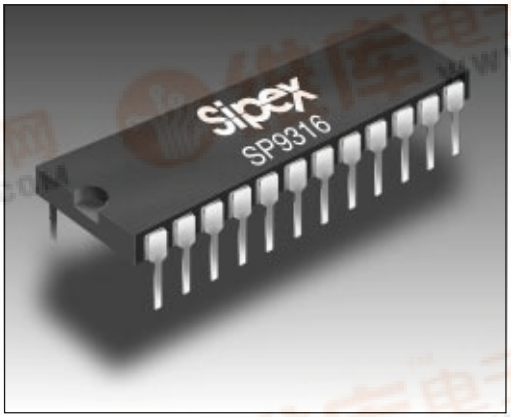
SIGNAL PROCESSING EXCELLENCE

SP9316

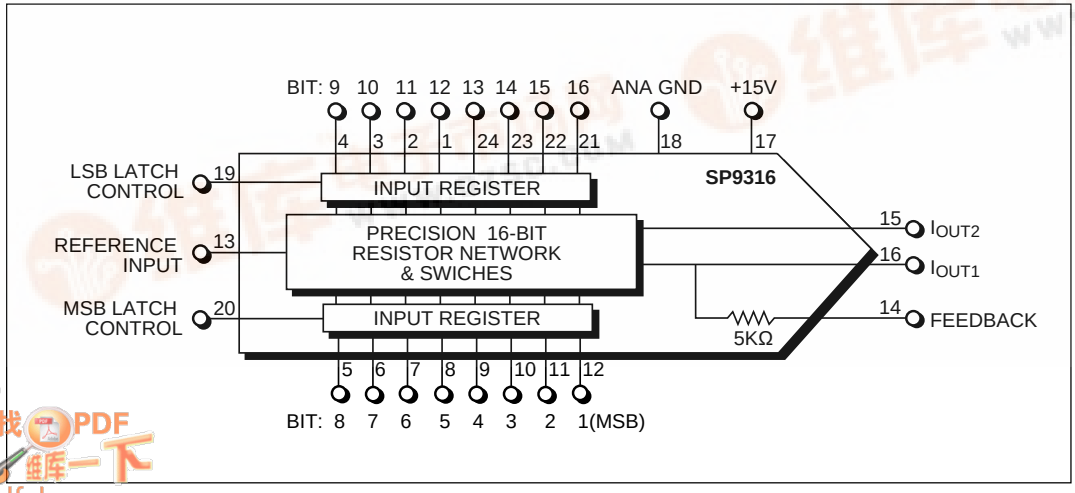
16–Bit CMOS Multiplying DAC

- High Stability with No Laser–Trimming
- 15–Bit Monotonicity over Temperature
- Single Power Supply Operation
- Upper/Lower Byte Input Registers
- 2– and 4–Quadrant Multiplication
- 60mW Power Dissipation



DESCRIPTION…

The **SP9316** is a 16–bit, monolithic CMOS, multiplying digital-to-analog converter with two 8–bit input registers for direct microprocessor interface. It offers two– and four–quadrant multiplying capability with TTL/DTL and CMOS logic compatibility. Operating from a single +15V supply, power dissipation is less than 60mW. The **SP9316** is packaged in 24-pin ceramic or molded plastic. Models are available for operation over the commercial (0°C to 70°C) and military (–55°C to +125°C) temperature ranges. For product screened to MIL–STD–883, please consult the factory.

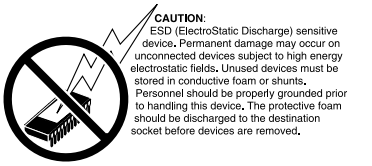


ABSOLUTE MAXIMUM RATINGS

(T_A=25°C unless otherwise noted)

These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{DD} to GND ..... –0.3V, +17V
Digital Input Voltage to GND ..... –0.3V ,V_{DD} +0.3V
V_{REF} or V_{RFB} to GND ..... ±25V
Output Voltage (Pin 15, Pin 16) ..... –0.3V, V_{DD} +0.3V
Power Dissipation (Any Package) to +75°C 450mW
Derates above 75°C by ..... 6mW/°C
Dice Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C



SPECIFICATIONS

(T_A=25°C; V_{DD} =+15V, V_{REF} = +10V; I_{O1} = AGND = GND = 0V; unipolar unless otherwise noted.)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
STATIC PERFORMANCE					
Resolution	16			Bits	
Integral Non-Linearity					Note 5
C-4			±0.006	%FSR	
B-4			±0.006	%FSR	
Differential Non-Linearity					Note 7
C-4			±0.006	%FSR	
B-4			±0.006	%FSR	
Offset Error			60	µV	Note 3
Gain Error		0.1	0.2	%FSR	Note 4
AC PERFORMANCE CHARACTERISTICS					
Propagation Delay		300		ns	Note 9
Current Settling Time					Major code settling times
To 0.01% FSR (strobed)		2.0		µs	
To 0.00076% FSR (strobed)		3.0		µs	
Output Capacitance					
C_{O1}		170		pF	Digital input V_{IH}
C_{O2}		30		pF	Digital input V_{IH}
C_{O3}		80		pF	Digital input V_{IL}
C_{O4}		100		pF	Digital input V_{IL}
Glitch Energy		250		nV-s	Note 10
Multiplying Feedthrough Error					
		3.0		mV_{P-P}	Note 11
		0.3		mV_{P-P}	Note 12
STABILITY					
All Grades:					Note 4
Gain Error TC		±1.0	±4.0	ppm/°C	Note 6
Offset			±1.0	ppm/°C	
Integral Non-Linearity TC		±0.1	±1.0	ppm/°C	
			±1.0	ppm/°C	Note 5
Monotonicity Guaranteed					
C-4	14			Bits	
B-4	14			Bits	
Power Supply Rejection		±0.0001	±0.002	%/%	V_{DD} = 14.0V to 16.0V
LONG-TERM STABILITY					
Differential Non-linearity		1		ppm/°C	
Offset		±0.5		ppm/°C	
Gain		±1		ppm/°C	
REFERENCE INPUT					
Input Impedance	2.5	5.0	7.5	KΩ	
Voltage Range	–10		+10	Volts	
SWITCHING CHARACTERISTICS					
Strobe Width	80	60		ns	
Data Setup Time	80	70		ns	
Data Hold Time	40	20		ns	

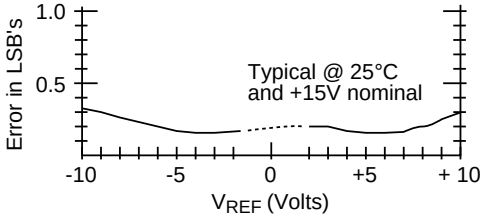
SPECIFICATIONS (continued)

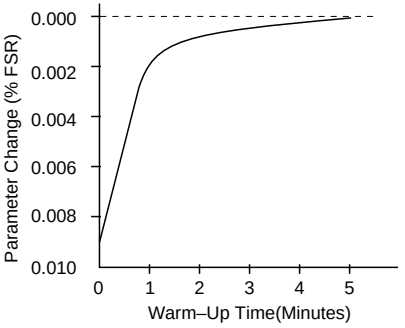
(T_A=25°C; V_{DD} =+15V, V_{REF} = +10V; I_{O1} = AGND = GND = 0V; unipolar unless otherwise noted.)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DIGITAL INPUTS					
Logic Levels					
V_{IH}	2.4		V_{DD}	Volts	
V_{IL}	-0.3		0.8	Volts	
Input Current		±1.0	±10.0	µA	Note 1
Input Capacitance			8	pF	Note 2
Coding					
2-Quadrant Unipolar		Binary			
4-Quadrant Bipolar		Offset Binary			
ANALOG OUTPUT					
Small Signal -3dB Bandwidth		1		MHz	
Output Capacitance					
C_{OUT1}		90		pF	
C_{OUT2}		70		pF	
POWER REQUIREMENTS					
Supply Current		2.0	4.0	mA	DIG IN = V_{IL} or V_{IH}
Voltage Range V_{DD}	+5	+15	+16	Volts	
Power Dissipation			60	mW	DIG IN = V_{IL} or V_{IH}
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
Commercial	0		+70	°C	
Military	-55		+125	°C	
Storage Temperature	-65		+150	°C	
Package					
Commercial		24–pin Plastic DIP			
Military		24–pin CerDIP			

Notes and Cautions:

1. Logic inputs are MOS gates. I_{IN} typically is less than 1nA @ 25°C.
2. Guaranteed by design, but not production tested.
3. Unipolar: Using the internal $R_{FEEDBACK}$ with nulled external amplifier in a constant 25°C ambient (offset doubles every 10°C).
4. Using internal feedback resistor.
5. Integral Linearity, for this product, is measured as the arithmetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value for any given input combination.
   Differential Linearity is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
6. The **SP9316** series is designed to be used only in those applications where the current output is virtual ground; i.e. the summing junction of an op amp in the inverting mode. The internal feedback resistor must be used to achieve temperature tracking. See applications information for recommended circuit configurations.
7. For military temperature range product, screened to MIL-STD-883C, please consult the factory.
8. Sample tested only to ensure compliance.
9. I_{O1} load R_L = 100Ω, C_{EXT} = 13pF; all data inputs 0V to V_{DD} or V_{DD} to 0V; from 50% digital input change to 90% of final analog output.
10. V_{REF} = 0V, DAC register alternatively loaded with all 0's and all 1's.
11. Measured at output I_{O1}; V_{REF} = $20V_{P-P}$; F = 10kHz sinewave.
12. Measured at output I_{O1}; V_{REF} = $20V_{P-P}$; F = 1kHz sinewave.





PIN ASSIGNMENTS

Pin 1 — DB_{12} — Data Bit 12.

Pin 2 — DB_{11} — Data Bit 11.

Pin 3 — DB_{10} — Data Bit 10.

Pin 4 — DB_{9} — Data Bit 9.

Pin 5 — DB_{8} — Data Bit 8.

Pin 6 — DB_{7} — Data Bit 7.

Pin 7 — DB_{6} — Data Bit 6.

Pin 8 — DB_{5} — Data Bit 5.

Pin 9 — DB_{4} — Data Bit 4.

Pin 10 — DB_{3} — Data Bit 3.

Pin 11 — DB_{2} — Data Bit 2.

Pin 12 — DB_{1} — Data Bit 1 (MSB).

Pin 13 — V_{REF} In — Voltage Reference Input.

Pin 14 — R_{FB} — Feedback Resistor.

Pin 15 — I_{OUT2} — Current Output.

Pin 16 — I_{OUT1} — Inverted Current Output.

Pin 17 — VDD — +15V Power Supply.

Pin 18 — GND — Analog GND.

Pin 19 — LSB LATCH — LSB Latch control. Level–triggered. Data is latched with strobe at logic 0; logic 1 allows data to update DAC directly.

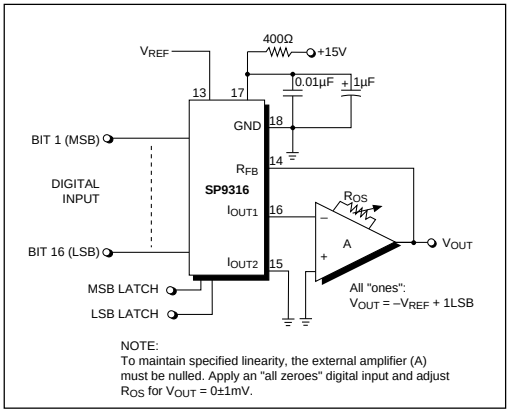


Figure 1. Unipolar Operation

Pin 20 — MSB LATCH — MSB Latch control. Level–triggered. Logic 0 strobes data into latch; logic 1 allows data to update DAC directly.

Pin 21 — DB_{16} — Data Bit 16 (LSB) .

Pin 22 — DB_{15} — Data Bit 15.

Pin 23 — DB_{14} — Data Bit 14.

Pin 24 — DB_{13} — Data Bit 13.

FEATURES...

The **SP9316** is a 16-bit, monolithic CMOS, multiplying digital-to-analog converter with two 8-bit input registers for direct microprocessor interface. It offers two– and four–quadrant multiplying capability with TTL/DTL and CMOS logic compatibility. It is ideally suited for Automated Test Equipment, medical instrumentation and high–energy physics applications. Operating from a single +15V supply, power dissipation is less than 60mW. High accuracy and monotonicity are achieved without laser–trimming through the use of a highly accurate, low–TCR thin–film resistor process. A unique digital decoding technique of the 4 MSB's results in excellent linearity and stability over both time and temperature. The **SP9316** is packaged in hermetic 24-pin ceramic or molded plastic. Models are available for operation over the commercial (0°C to 70°C) and military (–55°C to +125°C) temperature ranges. For product screened to MIL–STD–883, please consult the factory.

USING THE SP9316

General Configuration

The **SP9316** can be configured for unipolar voltage operation (2-quadrant multiplication) or bipolar voltage operation (4-quadrant multiplication.) Coding is binary and offset binary respectively. In bipolar operation both the reference signal and the number represented by the digital input applied to the **SP9316** may be of either positive or negative polarity.

Individual latch controls are provided for the high and low bytes which may be tied together for a single 16-bit word update. The data is latched with the strobe at logic 0. The latches are level–triggered and can be made transparent by tying them to logic 1. However, use of the latches is recommended in most applications as they significantly reduce data bit skew, which affects the glitch performance.

Layout, Grounding and Guarding

16-bit system performance can be maintained with suitable attention paid to the layout, grounding and guarding techniques employed. All grounds should be of as low resistance as possible. Analog and digital grounds should be individually star-pointed and tied together as close as possible to the **SP9316**. Good layout techniques dictate that the high–speed digital inputs should be kept separate from low–level analog outputs. The DAC output and op amp input are high impedance and so are sensitive to interference from the digital input lines. Careful pinout design of the **SP9316** has reduced this problem to a minimum, but guarding of these points should be considered. Figures 3 and 4 detail the low impedance guard track layout.

Amplifier Selection

The **SP9316** allows the designer to obtain the optimum performance for each application. Selection of the correct operational amplifier, and the layout of the associated components are critical to the success of the design. To obtain the optimum linearity performance, the amplifiers must have an open loop gain in excess of 100,000 or 100dB. Care should be taken to ensure that the summing junction is as close to analog ground as possible. Most applications demand that the input offset be kept below 100µV. To maintain accuracy over temperature, the amplifiers should have low bias currents and offset voltage temperature coefficients.

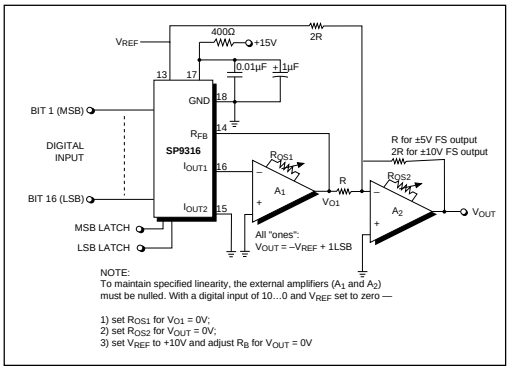


Figure 2. Bipolar Operation

Binary Input	Analog Output
111…111	$-V_{REF}(1-2^{-N})$
100…001	$-V_{REF}(+2^{-N})$
100…000	$-V_{REF}(\ )$
011…111	$-V_{REF}(-2^{-N})$
000…001	$-V_{REF}(2^{-N})$
000…000	0

Table 1. Unipolar Transfer Function

In bipolar applications, attention must be paid to the choice of resistors R and 2R (see *figure 2*). As the analog voltage output increases from zero to full-scale, the power dissipated by the feedback resistor increases and the resistor heats up. This causes a small change in the resistance value which could lead to an alteration to the transfer function, which may be seen as integral linearity errors. The internal resistor network has been designed using ultra-stable thin-film nichrome. It is important that the temperature coefficient of the external resistors match those in the DAC as closely as possible. Resistors with a temperature coefficient of 10ppm/°C or better should be used.

LONG TERM DRIFT

When measuring the stability of the **SP9316**, great care should be taken to ensure that the drift of the measurement instruments can be sepa-

Offset Binary Input	Analog Output
111…111	$-V_{REF}(1-2^{-(N-1)})$
100…001	$-V_{REF}(2^{-(N-1)})$
100…000	0
011…111	$V_{REF}(2^{-(N-1)})$
000…001	$V_{REF}(1-2^{-(N-1)})$
000…000	V_{REF}

Table 2. Bipolar Transfer Function

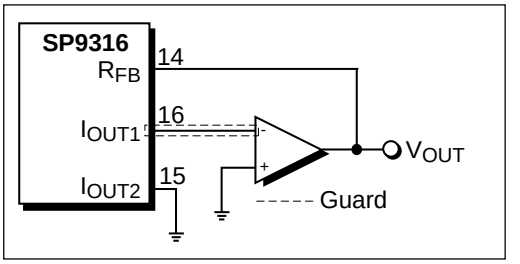


Figure 3. Unipolar Guarding

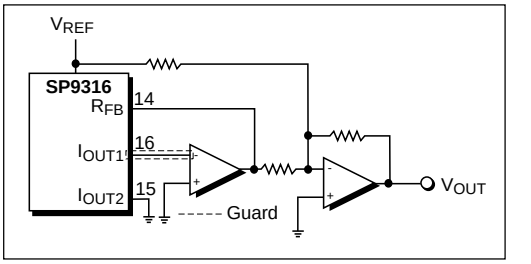


Figure 4. Bipolar Guarding

rated from the device drift, and that all measurements are taken at identical temperatures. The long–term drift of the **SP9316** voltage output system transfer function, after initial op amp trim, will largely be determined by the choice of the external components. For minimum offset error the op amps should be trimmed after one hour of continuous operation. The **SP9316** contribution to the offset drift after that time will be ±0.1ppm/°C per 1000 hours. The long–term gain drift error contribution of the **SP9316** is ±1 ppm/°C per 1000 hours. Also to be considered are the temperature coefficients of the external resistors, the op amp drift specifications and the stability of the reference. The **SIPEX HS2700LD**, with a stability drift of 3ppm/°C, is recommended as a suitable voltage reference.

The unique segmented architecture of the **SP9316** resistor network, plus the low–TCR nichrome materials and processes used in its manufacture, results in an exceptionally low linearity drift with time. Typical differential linearity drift with temperature is 0.1ppm/°C.

APPLICATION

Digitally–Controlled Low Pass Filter

The **SP9316** can be used to construct active filters which display very low noise and distortion characteristics. Low pass filters can be designed to provide digital control over center frequency, gain and Q-factor. The **SP9316** is an ideal high resolution element for this application. *Figure 5* shows a low–pass filter designed to be independent of the resistance of the **SP9316** network by using it as a programmable gain element. The filter characteristic is given by:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-R_3}{R_1}\left(\frac{1}{1+ j\omega\left(\frac{R_3R_4C}{R_2D}\right)}\right)$$

where D is the binary code applied to the DAC and C is the value of the capacitor.

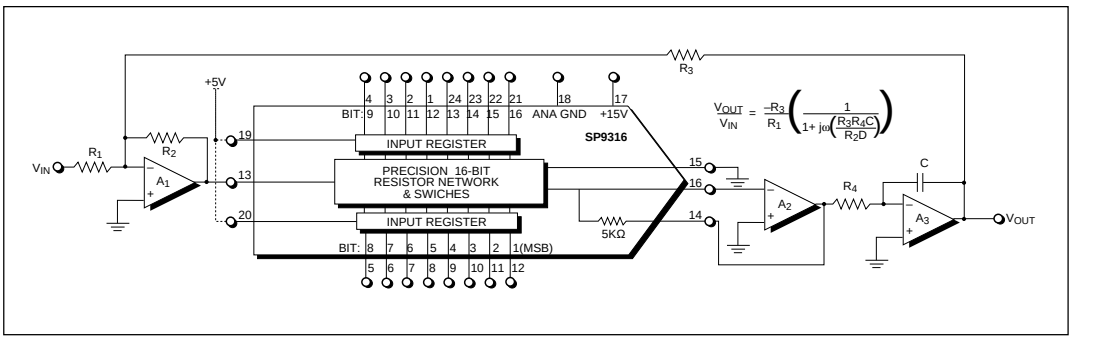


Figure 5. Digitally–Controlled Low–Pass Filter

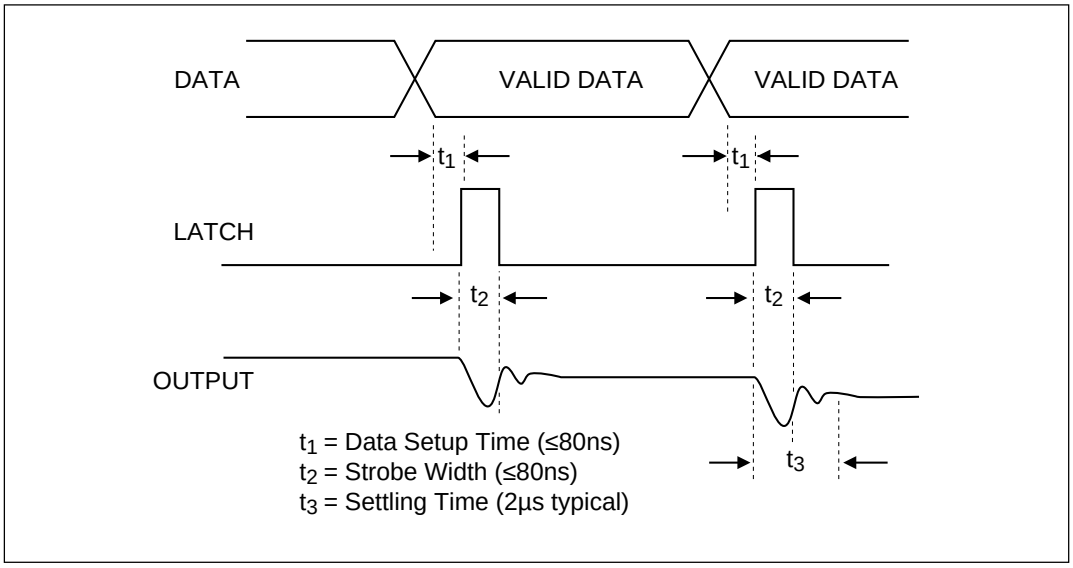


Figure 6. Timing

Ordering Information

Model	Linearity	Package
0°C to +70°C:		
SP9316C-4	14-Bit Linearity	24–pin, 0.6" Plastic DIP
-55°C to +125°C, MIL-STD-883C Screened:		
SP9316B-4	14-Bit Linearity	24–pin, 0.6" CerDIP

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