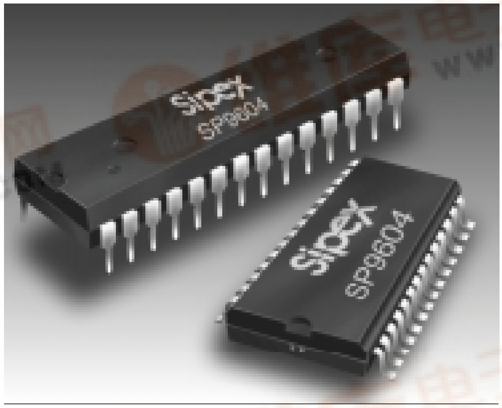
Sipex

SP9604

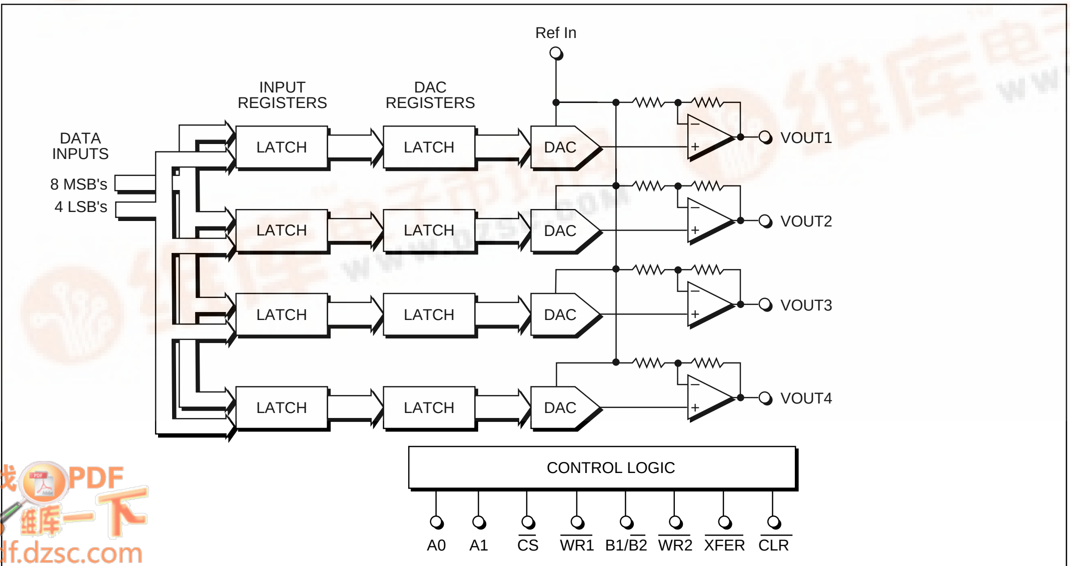
Quad, 12–Bit, Low Power Voltage Output D/A Converter

- Low Cost
- Four 12–Bit DAC's on a Single Chip
- Very Low Power — 30 mW (8mW/DAC)
- Double-Buffered Inputs
- ± 5V Supply Operation
- Voltage Outputs, ± 4.5V Range
- Midscale Preset, Zero Volts Out
- Guaranteed ±0.5 LSB Max INL
- Guaranteed ±0.75 LSB Max DNL
- 250kHz 4-Quadrant Multiplying Bandwidth
- 28–pin SOIC and Plastic DIP Packages
- Either 12 or 8 bit µP bus



DESCRIPTION

The **SP9604** is a very low power replacement for the popular SP9345, Quad 12-Bit Digital-to-Analog Converter. It features ±4.5V output swings when using ±5 volt supplies. The converter is double-buffered for easy microprocessor interface. Each 12-bit DAC is independently addressable and all DACs may be simultaneously updated using a single transfer command. The output settling-time is specified at 30µs. The **SP9604** is available in 28–pin SOIC and plastic DIP packages, specified over commercial temperature range.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{DD} - GND .... -0.3V,+6.0V
V_{SS} - GND .... +0.3V, -6.0V
V_{DD} - V_{SS} .... -0.3V, +12.0V
V_{REF} .... V_{SS}, V_{DD}
D_{IN} .... V_{SS}, V_{DD}
Power Dissipation
Plastic DIP 375mW
(derate 7mW/°C above +70°C)
Small Outline 375mW
(derate 7mW/˚C above +70˚C)

CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

(Typical @ 25˚C, $T_{MIN} \le T_A \le T_{MAX}$; V_{DD} = +5V, V_{SS} = -5V, V_{REF} = +3V; CMOS logic level digital inputs; specifications apply to all grades unless otherwise noted.)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DIGITAL INPUTS					
Logic Levels					
V_{IH}	2.4			Volts	
V_{IL}			0.8	Volts	
4 Quad, Bipolar Coding		Offset Binary			
REFERENCE INPUT					
Voltage Range		±3	±4.5	Volts	Note 5
Input Resistance	1.5	2.2		kΩ	D_{IN} = 1,877; code dependent
ANALOG OUTPUT					
Gain					
-K		±0.5	±2.0	LSB	V_{REF} = ±3V; Note 3
-J		±1.0	±4.0	LSB	V_{REF} = ±3V; Note 3
		±1.0	±5.0	LSB	V_{REF} = ±4.5V; Note 3
Initial Offset Bipolar		±0.25	±3.0	LSB	D_{IN} = 2,048
Voltage Range Bipolar		±3.0	±4.5	Volts	
Output Current	±5.0			mA	V_{REF} = ±3V
	±0.5			mA	V_{REF} = ±4.5V
STATIC PERFORMANCE					
Resolution	12			Bits	
Integral Linearity					
-K		±0.25	±0.5	LSB	V_{REF} = ±3V; Note 3
-J		±0.5	±1.0	LSB	V_{REF} = ±3V; Note 3
		±0.5	±3.0	LSB	V_{REF} = ±4.5V; Note 3
Differential Linearity					
-K		±0.25	±0.75	LSB	
-J		±0.25	±1.0	LSB	
Monotonicity		Guaranteed			
DYNAMIC PERFORMANCE					
Settling Time					
Small Signal		4		µs	to 0.024%
Full Scale		30		µs	to 0.024%
Slew Rate		0.3		V/µs	
Multiplying Bandwidth		250		KHz	

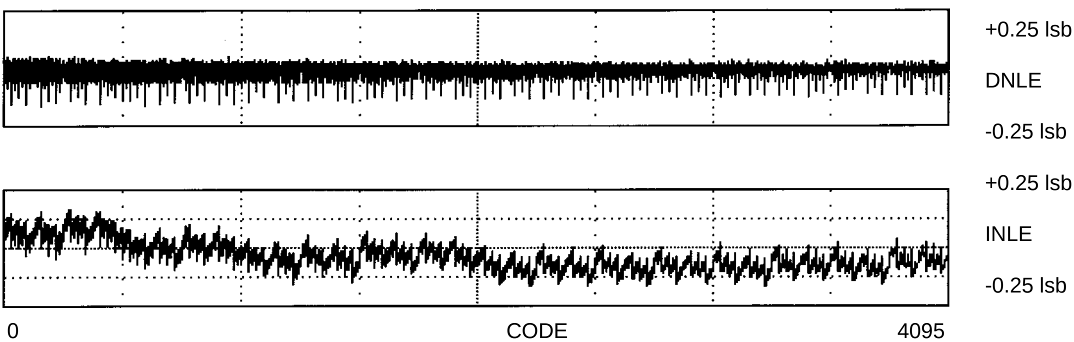
SPECIFICATIONS (continued)

(Typical @ 25˚C, $T_{MIN} \leq T_A \leq T_{MAX}$; V_{DD} = +5V, V_{SS} = -5V, V_{REF} = +3V; CMOS logic level digital inputs; specifications apply to all grades unless otherwise noted.)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
STABILITY					
Gain		15		ppm/˚C	t_{MIN} to t_{MAX}
Bipolar Zero		15		ppm/˚C	t_{MIN} to t_{MAX}
SWITCHING CHARACTERISTICS					
t_{DS} Data Set Up Time	140	100		ns	to rising edge of WR1
t_{DN} Data Hold Time	0			ns	Figure 4
t_{WR} Write Pulse Width	140	100		ns	
t_{XFER} Transfer Pulse Width	140	100		ns	
t_{WC} Total Write Command	280	200		ns	
POWER REQUIREMENTS					Note 5
V_{DD}					+5V, ±3%; Note 4, 5
–J, –K		3	4	mA	
V_{SS}					-5V, ±3%; Note 4, 5
–J, –K		3	4	mA	
Power Dissipation		30		mW	
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
-J, -K	0		+70	°C	
Storage	-60		+150	°C	
Package					
-_P	28-pin Plastic DIP				
-_S	28-pin SOIC				

Notes:

1. Integral Linearity, for the **SP9604**, is measured as the arithmetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value for any given input condition.
2. Differential Linearity is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
3. 1 LSB = $2*V_{REF}/4{,}096$.
4. V_{REF} = 0V.
5. The following power up sequence is recommended to avoid latch up: VSS (-5V), VDD (+5V), REF IN.



DNLE, INLE Plots

PIN ASSIGNMENTS

Pin 1 — V_{OUT4} — Voltage Output from DAC4.

Pin 2 — V_{SS} — –5V Power Supply Input.

Pin 3 — V_{DD} — +5V Power Supply Input.

Pin 4 — $\overline{CLR}$ — $\overline{Clear}$. Gated with $\overline{WR2}$ (pin 11). Active low. Clears all DAC outputs to 0V.

Pin 5 — REF IN — Reference Input for DACs.

Pin 6 — GND — Ground.

Pin 7 — B1/$\overline{B2}$ — Byte 1/$\overline{Byte 2}$ — Selects Data Input Format. A logic "1" on pin 7 selects the 12–bit mode, and all 12 data bits are presented to the DAC(s) unchanged; a logic "0" selects the 8–bit mode, and the four LSBs are connected to the four MSBs, allowing an 8–bit MSB–justified interface.

Pins 8 and 9 — A_0 & A_1 — Address for DAC Selection. A_1/A_0 = 0/0 = DAC1; 0/1 = DAC2; 1/0 = DAC3; 1/1 = DAC4.

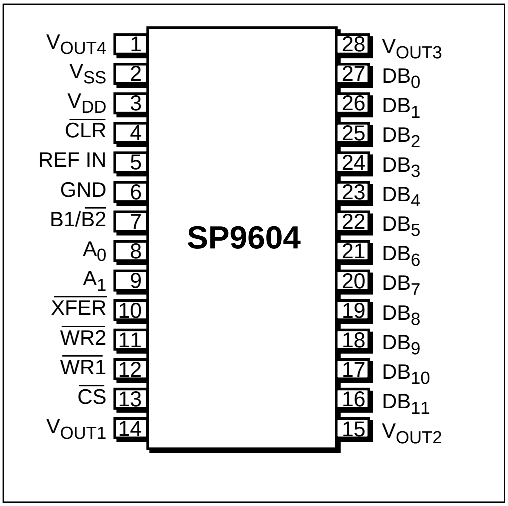
Pin 10 — $\overline{XFER}$ — $\overline{Transfer}$. Gated with $\overline{WR2}$ (pin 11); loads all DAC registers simultaneously. Active low.

Pin 11 — $\overline{WR2}$ — $\overline{Write Input 2}$ — In conjunction with $\overline{XFER}$ (pin 10), controls the transfer of data from the input registers to the DAC registers. In conjunction with $\overline{CLR}$ (pin 4), the DAC registers are forced to 1000 0000 0000 and the DAC outputs will settle to 0V. Active low.

Pin 12 — $\overline{WR1}$ — $\overline{Write Input1}$ — In conjunction with $\overline{CS}$ (pin 13), enables input register selection, and controls the transfer of data from the input bus to the input registers. Active low.

Pin 13 — $\overline{CS}$ — $\overline{Chip Select}$ — Enables writing data to input registers and/or transferring data from input bus to DAC registers. Active low.

PINOUT — 28–PIN PLASTIC DIP & SOIC



Pin 14 — V_{OUT1} — Voltage Output from DAC1.

Pin 15 — V_{OUT2} — Voltage Output from DAC2.

Pin 16 — DB_{11} — Data Bit 11; Most Significant Bit.

Pin 17 — DB_{10} — Data Bit 10.

Pin 18 — DB_9 — Data Bit 9.

Pin 19 — DB_8 — Data Bit 8.

Pin 20 — DB_7 — Data Bit 7.

Pin 21 — DB_6 — Data Bit 6.

Pin 22 — DB_5 — Data Bit 5.

Pin 23 — DB_4 — Data Bit 4.

Pin 24 — DB_3 — Data Bit 3.

Pin 25 — DB_2 — Data Bit 2.

Pin 26 — DB_1 — Data Bit 1.

Pin 27 — DB_0 — Data Bit 0; LSB

Pin 28 — V_{OUT3} — Voltage Output from DAC3.

FEATURES

The **SP9604** is a low–power replacement for the popular SP9345, Quad 12-Bit Digital-to-Analog Converter. This Quad, Voltage Output, 12-Bit Digital-to-Analog Converter features ±4.5V output swings when using ±5 volt supplies. The input coding format used is standard offset binary. (Please refer to *Table 1*.)

The converter utilizes double-buffering on each of the 12 parallel digital inputs, for easy microprocessor interface. Each 12-bit DAC is independently addressable and all DACs may be simultaneously updated using a single $\overline{XFER}$ command. The output settling-time is specified at 30µs to full 12–bit accuracy when driving a 5Kohm, 50pf load combination. The **SP9604**, Quad 12-Bit Digital-to-Analog Converter is ideally suited for applications such as ATE, process controllers, robotics, and instrumentation. The **SP9604** is available in 28–pin plastic DIP or SOIC packages, specified over the commercial (0°C to +70°C) temperature range.

THEORY OF OPERATION

The **SP9604** consists of five main functional blocks — input data multiplexer, data registers, control logic, four 12-bit D/A converters, and four bipolar output voltage amplifiers. The input data multiplexer is designed to interface to either 12- or 8-bit microprocessor data busses. The input data format is controlled by the B1/$\overline{B2}$ signal — a logic "1" selects the 12-bit mode, while a logic "0" selects the 8-bit mode. In the 12-bit mode the data is transferred to the input registers without changes in its format. In the 8-bit mode, the four least significant bits (LSBs) are connected to the four most significant bits (MSBs), allowing an 8-bit MSB-justified interface. All data inputs are enabled

INPUT			OUTPUT
MSB		LSB	
1111	1111	1111	VREF - 1 LSB
1111	1111	1110	VREF - 2 LSB
1000	0000	0001	0 + 1 LSB
1000	0000	0000	0
0000	0000	0001	-VREF + 1 LSB
0000	0000	0000	-VREF
$1\ LSB = \frac{2V_{REF}}{2^{12}}$			

Table 1. Offset Binary Coding

using the $\overline{CS}$ signal in both modes. The digital inputs are designed to be both TTL and 5V CMOS compatible.

In order to reduce the DAC full scale output sensitivity to the large weighting of the MSB's found in conventional R-2R resistor ladders, the 3 MSB's are decoded into 8 equally weighted levels. This reduces the contribution of each bit by a factor of 4, thus, reducing the output sensitivity to mis–matches in resistors and switches by the same amount. Linearity errors and stability are both improved for the same reasons.

Each D/A converter is separated from the data bus by two registers, each consisting of level-triggered latches, *Figure 1*. The first register (input register) is 12-bits wide. The input register is selected by the address input A_0 and A_1 and is enabled by the $\overline{CS}$ and $\overline{WR1}$ signals. In the 8-bit mode, the enable signal to the 8 MSB's is disabled by a logic low on B1/$\overline{B2}$ to allow the 4 LSB's to be updated. The second register (DAC register), accepts the decoded 3 MSB's plus the 9 LSB's. The four DAC registers are updated simultaneously for all DAC's using the $\overline{XFER}$ and $\overline{WR2}$ signals. Using the $\overline{CLR}$ and $\overline{WR2}$ signals or the power-on-reset, (enabled when the power is switched on) the DAC registers are set to 1000 0000 0000 and the DAC outputs will settle to 0V.

Using the control logic inputs, the user has full control of address decoding, chip enable, data transfer and clearing of the DAC's. The control logic inputs are level triggered, and like the data inputs, are TTL and CMOS compatible. The truth table (*Table 2*) shows the appropriate functions associated with the states of the control logic inputs.

The DACs themselves are implemented with a precision thin–film resistor network and CMOS transmission gate switches. Each D/A converter is used to convert the 12–bit input from its DAC register to a precision voltage.

The bipolar voltage output of the **SP9604** is created on-chip from the DAC Voltage Output (V_{DAC}) by using an operational amplifier and two feedback resistors connected as shown in *Figure 2*. This configuration produces a ±4.5V bipolar output range with standard offset binary coding.

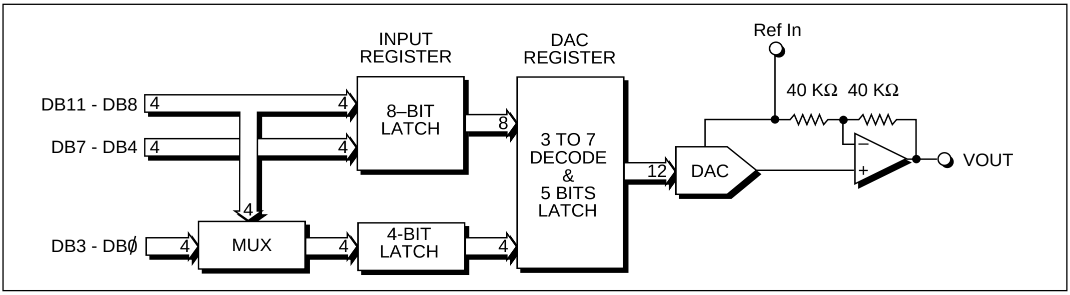


Figure 1. Detailed Block Diagram (only one DAC shown)

USING THE SP9604 WITH DOUBLE-BUFFERED INPUTS

Loading Data

To load a 12-bit word to the input register of each DAC, using a 12-bit data bus, the sequence is as follows:

1) Set $\overline{XFER}$=1, B1/$\overline{B2}$=1, $\overline{CLR}$=1, $\overline{WR1}$=1, $\overline{WR2}$=1, $\overline{CS}$=1.
2) Set A_1 and A_0 (the DAC address) to the desired DAC — 0,0 = DAC_1; 0,1 = DAC_2 1,0 = DAC_3; 1,1 = DAC_4.
3) Set D11 (MSB) through D0 (LSB) to the desired digital input code.
4) Load the word to the selected DAC by cycling $\overline{WR1}$ and $\overline{CS}$ through the following sequence:
   "1" — "0" — "1"
5) Repeat sequence for each input register.

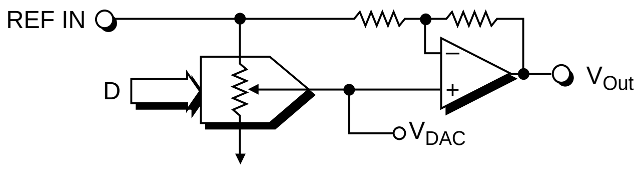
To load a 12-bit word to the input register of each DAC, using an 8-bit data bus, the sequence is as follows:

1) Set $\overline{XFER}$=1, B1/$\overline{B2}$=1, $\overline{CLR}$=1, $\overline{WR1}$=1, $\overline{WR2}$=1, $\overline{CS}$=1.
2) Set D11 through D4 to the 8 MSB's of the desired digital input code.
3) Load the 8 MSB's of the digital word to the selected input register by cycling $\overline{WR1}$ and $\overline{CS}$ through the "1" — "0" — "1" sequence.
4) Reset B1/$\overline{B2}$ from "1" —— "0"
5) Set D11 (MSB) through D8 to the 4 LSB's of the digital input code.
6) Load the 4 LSB's by cycling $\overline{WR1}$ and $\overline{CS}$ through the "1" — "0" — "1" sequence.
7) Repeat sequence for each input register.

A_1	A_0	$\overline{CS}$	$\overline{WR1}$	B1/$\overline{B2}$	$\overline{WR2}$	$\overline{XFER}$	$\overline{CLR}$	FUNCTION
0	0	‾|_|‾	‾|_|‾	1	1	X	X	Address DAC 1 and load input register
0	0	‾|_|‾	‾|_|‾	0	1	X	X	Address DAC 1 and load 4 LSBs
0	1	‾|_|‾	‾|_|‾	1	1	X	X	Address DAC 2 and load input register
0	1	‾|_|‾	‾|_|‾	0	1	X	X	Address DAC 2 and load 4 LSBs
1	0	‾|_|‾	‾|_|‾	1	1	X	X	Address DAC 3 and load input register
1	0	‾|_|‾	‾|_|‾	0	1	X	X	Address DAC 3 and load 4 LSBs
1	1	‾|_|‾	‾|_|‾	1	1	X	X	Address DAC 4 and load input register
1	1	‾|_|‾	‾|_|‾	0	1	X	X	Address DAC 4 and load 4 LSBs
X	X	**	**	X	‾|_|‾	‾|_|‾	1	Transfer data from input registers to DAC registers
X	X	X	X	X	‾|_|‾	1	‾|_|‾	Sets all DAC output voltages to 0V
X	X	1	1	X	0	0	‾|_|‾	Temporarily force all DAC output voltages to 0V, while $\overline{CLR}$ is low
X	X	1	X	X	X	X	X	Invalid state with any other control line active
X	X	X	1	X	X	X	X	Invalid state with any other control line active

X = Don't care; ** = Don't care; however, $\overline{CS}$ and $\overline{WR1}$ = 1 will inhibit changes to the input registers.

Table 2. Control Logic Truth Table



$$V_{Out} = \left(\frac{D}{2048} - 1\right) \times \text{REF IN}$$

$$V_{DAC} = \frac{D}{4{,}096} \times \text{REF IN}$$

Figure 2. Transfer Function

TRANSFERRING DATA

To transfer the four 12-bit words in the four input registers to the four DAC registers:

1) Set $\overline{\text{CLR}}$=1, $\overline{\text{CS}}$=1, $\overline{\text{WR1}}$=1.
2) Cycle $\overline{\text{WR2}}$ and $\overline{\text{XFER}}$ through the "1" — "0" — "1" sequence.

To set the outputs of the four DAC's to 0V, cycle $\overline{\text{WR2}}$ and $\overline{\text{CLR}}$ through the "1" — "0" — "1" sequence, while keeping $\overline{\text{XFER}}$=1.

One Latch, or No Latches

The latches that form the registers can be used in a "semi-" transparent mode, and a "fully-" transparent mode. In order to use the **SP9604** in either mode the user must be interfaced to a 12-bit bus only (B1=1).

The semi-transparent mode is set up such that the second set of latches is transparent and the first set is used to latch the incoming data. Data is latched into the first set rather than the second set, in order to minimize glitch energy induced from the data formatting. In this mode, $\overline{\text{XFER}}$, $\overline{\text{WR2}}$ and $\overline{\text{CS}}$ are tied low, and $\overline{\text{WR1}}$ is used to strobe the data to the addressed DAC. Each DAC is addressed using the address lines A_0 and A_1. After the appropriate DAC has been selected and the data is settled at the digital inputs, bringing $\overline{\text{WR1}}$ low will transfer the data to the addressed DAC. The user should be sure to bring $\overline{\text{WR1}}$ high again so that the next selected DAC will not be overwritten by the last digital code. This mode of operation may be useful in applications where preloading of the input registers is not necessary, *Figure 3a*.

A fully transparent mode is realized by tying $\overline{\text{WR1}}$, $\overline{\text{CS}}$, $\overline{\text{WR2}}$, and $\overline{\text{XFER}}$ all low. In this mode, anything that is written on the 12-bit data bus will be passed directly to the selected DAC. Since both latches are not being used, the previous digital word will be overwritten by the new data as soon as the address changes. This may be useful should the user want to calibrate a circuit, by taking full scale or zero scale readings for all four DAC's, *Figure 3b*.

Zeroing DAC Outputs

While keeping $\overline{\text{XFER}}$ pin high, the DAC outputs can be set to zero volts two different ways. The first involves the $\overline{\text{CLR}}$ and $\overline{\text{WR2}}$ pins. In normal operation, the $\overline{\text{CLR}}$ pin is tied high, thus, disabling the clear function. By cycling $\overline{\text{WR2}}$ and $\overline{\text{CLR}}$ through "1"—"0"—"1" sequence, a digital code of 1000 0000 0000 is written to all four DAC registers, producing a half scale output or zero volts. The second utilizes the built in power-on-reset. Using this feature, the **SP9604** can be configured such that during power-up, the second register will be digitally “zeroed”, producing a zero volt output at each of the four DAC outputs. This is achieved by powering the unit up with $\overline{\text{XFER}}$ in a high state. Thus, with no external circuitry, the **SP9604** can be powered up with the analog outputs at a known, zero volt output level.

Temporarily forcing all DAC outputs to 0V

Set $\overline{\text{WR1}}$=1, $\overline{\text{CS}}$=1, $\overline{\text{WR2}}$=0, $\overline{\text{XFER}}$=0. The DAC registers can be temporarily forced to 1000 0000 0000 by bringing the $\overline{\text{CLR}}$ pin low. This will force the DAC outputs to 0V, while the $\overline{\text{CLR}}$ pin remains low. When the $\overline{\text{CLR}}$ pin is brought back high, the digital code at the DAC registers will again appear at the DAC's digital inputs, and the analog outputs will return to their previous values.

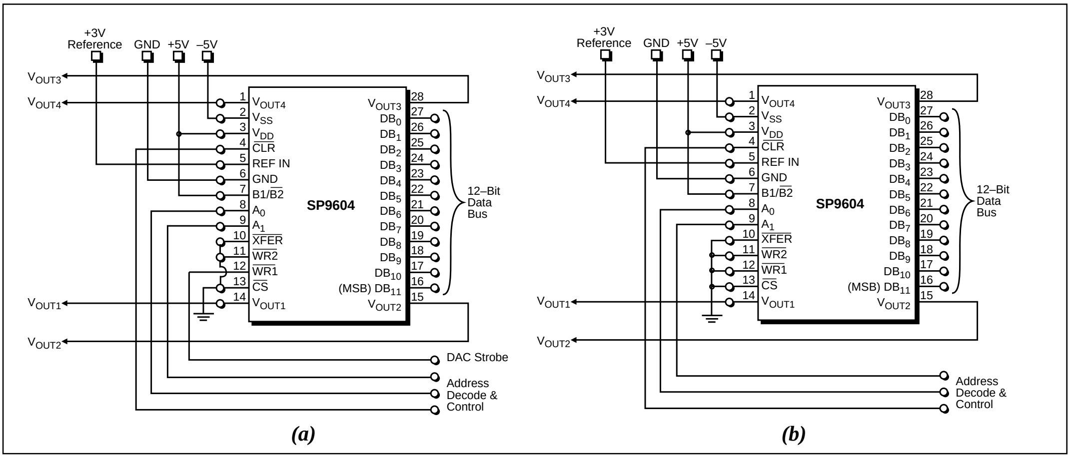


Figure 3. Latch Control Options — (a) Semi–Transparent Latch Mode; (b) Fully–Transparent Latch Mode

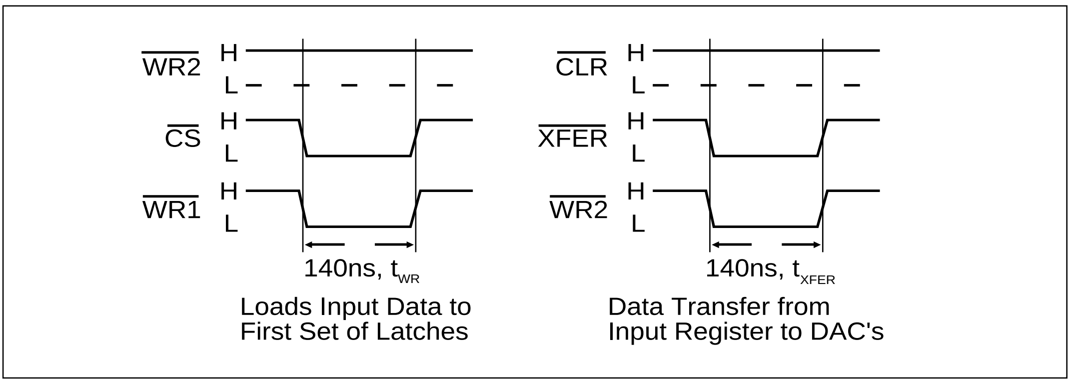
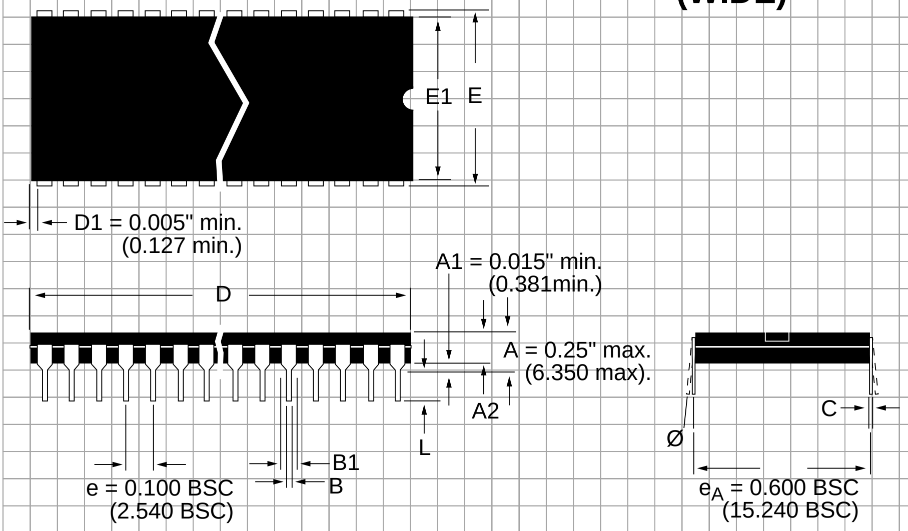


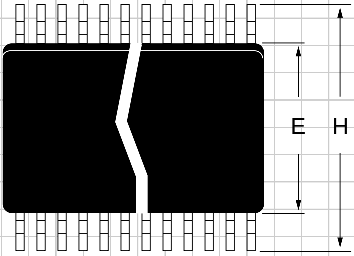
Figure 4. Timing

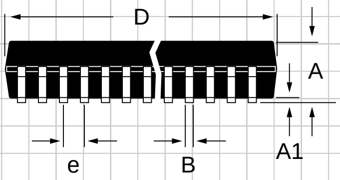
PACKAGE: PLASTIC DUAL–IN–LINE (WIDE)

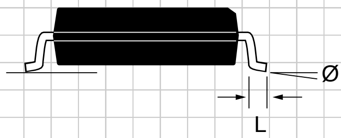


DIMENSIONS (Inches) Minimum/Maximum (mm)	24–PIN	28–PIN	32–PIN	40–PIN	48–PIN
A2	0.125/0.195 (3.175/4.953)	0.125/0.195 (3.175/4.953)	0.125/0.195 (3.175/4.953)	0.125/0.195 (3.175/4.953)	0.125/0.195 (3.175/4.953)
B	0.014/0.022 (0.366/0.559	0.014/0.022 (0.366/0.559	0.014/0.022 (0.366/0.559	0.014/0.022 (0.366/0.559)	0.014/0.022 (0.366/0.559)
B1	0.030/0.070 (0.762/1.778)	0.030/0.070 (0.762/1.778)	0.030/0.070 (0.762/1.778)	0.030/0.070 (0.762/1.778)	0.030/0.070 (0.762/1.778)
C	0.008/0.015 (0.203/0.381)	0.008/0.015 (0.203/0.381)	0.008/0.015 (0.203/0.381)	0.008/0.015 (0.203/0.381)	0.008/0.015 (0.203/0.381)
D	1.150/1.290 (29.21/32.76)	1.380/1.565 (35.05/39.75)	1.645/1.655 (41.78/42.04)	1.980/2.095 (50.29/53.21)	2.385/2.480 (60.57/62.99)
E	0.600/0.625 (15.24/15.87)	0.600/0.625 (15.24/15.87)	0.600/0.625 (15.24/15.87)	0.600/0.625 (15.24/15.87)	0.600/0.625 (15.24/15.87)
E1	0.485/0.580 (12.31/14.73)	0.485/0.580 (12.31/14.73)	0.485/0.580 (12.31/14.73)	0.485/0.580 (12.31/14.73)	0.485/0.580 (12.31/14.73)
L	0.115/0.200 (2.921/5.080)	0.115/0.200 (2.921/5.080)	0.115/0.200 (2.921/5.080)	0.115/0.200 (2.921/5.080)	0.115/0.200 (2.921/5.080)
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)

PACKAGE: PLASTIC SMALL OUTLINE (SOIC)







DIMENSIONS (Inches) Minimum/Maximum (mm)	28–PIN
A	0.090/0.100 (2.29/2.54)
A1	0.004/0.010 (0.102/0.254)
B	0.014/0.020 (0.36/0.48)
D	0.706/0.718 (17.93/18.24)
E	0.340/0.350 (8.64/8.89)
e	0.050 BSC (1.270 BSC)
H	0.463/0.477 (11.76/12.12)
L	0.020/0.042 (0.51/1.07)
Ø	0°/8° (0°/8°)

ORDERING INFORMATION

Model	Temperature Range	Package
Monolithic 12-Bit Quad DAC Voltage Output:		
SP9604JP	0˚C to +70˚C	28-pin, 0.6" Plastic DIP
SP9604KP	0˚C to +70˚C	28-pin, 0.6" Plastic DIP
SP9604JS	0˚C to +70˚C	28–pin, 0.35" SOIC
SP9604KS	0˚C to +70˚C	28–pin, 0.35" SOIC

Please consult the factory for pricing and availability on a Tape-On-Reel option.

Sipex Corporation

SIGNAL PROCESSING EXCELLENCE

Sipex Corporation

Headquarters and
Sales Office
22 Linnell Circle
Billerica, MA 01821
TEL: (978) 667-8700
FAX: (978) 670-9001
e-mail: sales@sipex.com

Sales Office
233 South Hillview Drive
Milpitas, CA 95035
TEL: (408) 934-7500
FAX: (408) 935-7600