SPT7870

SPT
SIGNAL PROCESSING TECHNOLOGIES

SPT7870
10-BIT, 100 MSPS ECL A/D CONVERTER

FEATURES

- 10-Bit, 100 MSPS Analog-to-Digital Converter
- Monolithic Bipolar
- Single-Ended Bipolar Analog Input
- -1.0 V to +1.0 V Analog Input Range
- Internal Sample-and-Hold
- Internal Voltage Reference
- Programmable Data Output Formats
- Single Ended ECL/PECL Outputs
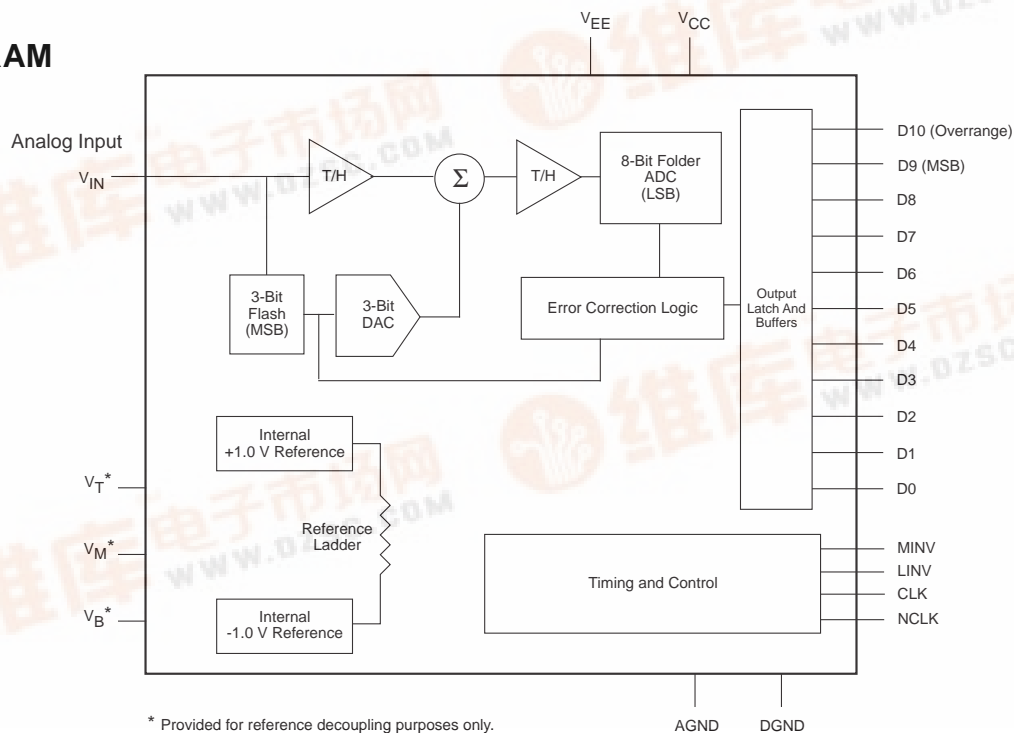- TTL Version Available as the SPT7871

APPLICATIONS

- Professional Video
- HDTV
- Communications
- Imaging
- Digital Oscilloscopes

GENERAL DESCRIPTION

The SPT7870 is a 10-bit, 100 MSPS analog-to-digital converter, with a two stage sub-ranging flash/folder architecture. The bipolar, single-ended analog input provides an easy interface for most applications. Programmable data output formats provide additional ease of implementation and flexibility. The device supports high-speed ECL- and PECL-level outputs.

The resolution and performance of this device makes it well suited for professional video and HDTV applications. The on-chip track-and-hold provides for excellent AC performance enabling this device to be a converter of choice for RF communications and digital sampling oscilloscopes. The SPT7870 is available in a 44L cerquad package in the industrial temperature range and in die form.

BLOCK DIAGRAM

* Provided for reference decoupling purposes only.

Signal Processing Technologies, Inc.

4755 Forge Road, Colorado Springs, Colorado 80907, USA
Phone: (719) 528-2300   FAX: (719) 528-2370   E-Mail: www.spt.com

ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages

V_{CC} .... 0 to +6.5 V
V_{EE} .... 0 to -6.5 V

Input Voltages

Analog Input .... $V_{EE} \leq V_{IN} \leq V_{CC}$
LINV/MINV Inputs .... -0.5 V to V_{CC} + 0.5 V
CLK/NCLK Inputs .... V_{EE} to 0 V

Output

Digital Outputs .... +30 to -30 mA

Temperature

Operating Temperature .... -40 to + 85 °C
Junction Temperature .... + 175 °C
Lead, Soldering (10 seconds) .... + 300 °C
Storage .... -60 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=+25 °C, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±1.0 V, f_{Clock}=80 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC Performance						
Resolution				10		Bits
Differential Linearity	f_{Clock} = 6.4 MHz	I	-1.0	±0.5	+1.25	LSB
Integral Linearity, Best Fit	f_{Clock} = 6.4 MHz	I		±1.0	±2.0	LSB
	Full Temperature	V		±2.5		LSB
No Missing Codes	f_{Clock} = 6.4 MHz	I		Guaranteed		
Analog Input						
Input Voltage Range		V		±1.0		V
Input Bias Current		I	-100	25	100	µA
Input Resistance		I	50	150		kΩ
	Full Temperature	V		100		kΩ
Input Capacitance		V		5		pF
Input Bandwidth	Full Power	IV	150	180		MHz
±FS Offset Error		I		±20	±100	mV
Timing Characteristics						
Maximum Conversion Rate		IV	100			MSPS
Minimum Conversion Rate		V			2	MSPS
Pipeline Delay (Latency)		IV		2		Clock
Transient Response		V		10		ns
Overvoltage Recovery Time		V		10		ns
Output Delay (t_d)		V		3		ns
Aperture Delay Time		V		1		ns
Aperture Jitter Time		V		5		ps (rms)
Dynamic Performance						
Effective Number of Bits						
f_{IN} =10 MHz		I	8.1	8.5		Bits
f_{IN} = 25 MHz		I	8.1	8.5		Bits
f_{IN} = 25 MHz	f_{Clock} = 100 MHz	V		8.0		Bits
f_{IN} = 50 MHz		I	7.4	7.8		Bits
f_{IN} = 50 MHz	f_{Clock} = 100 MHz	V		7.5		Bits
Signal-To-Noise Ratio						
f_{IN} =10 MHz		I	52	55		dB
f_{IN} = 25 MHz		I	52	54		dB
f_{IN} = 25 MHz	f_{Clock} = 100 MHz	V		51		dB
f_{IN} = 50 MHz		I	52	54		dB
f_{IN} = 50 MHz	f_{Clock} = 100 MHz	V		50		dB
Total Harmonic Distortion[1]						
f_{IN} = 10 MHz		I	-56	-63		dBc
f_{IN} = 25 MHz		I	-55	-60		dBc
f_{IN} = 25 MHz	f_{Clock} = 100 MHz	V		-56		dBc
f_{IN} = 50 MHz		I	-47	-51		dBc
f_{IN} = 50 MHz	f_{Clock} = 100 MHz	V		-50		dBc

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ELECTRICAL SPECIFICATIONS

T_A=+25 °C, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±1.0 V, f_{Clock}=80 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Performance						
Signal-to-Noise & Distortion (SINAD)						
f_{IN} = 10 MHz		I	51	54		dB
f_{IN} = 25 MHz		I	51	53		dB
f_{IN} = 25 MHz	f_{Clock} = 100 MHz	V		50		dB
f_{IN} = 50 MHz		I	46.5	48		dB
f_{IN} = 50 MHz	f_{Clock} = 100 MHz	V		47		dB
Spurious Free Dynamic Range						
f_{IN} = 10 MHz		V		65		dB FS
f_{IN} = 25 MHz		V		62		dB FS
f_{IN} = 50 MHz		V		52		dB FS
Two-Tone Intermodulation						
Dist. Rejection[2]		V		-65		dBc
Differential Phase		V		0.5		Degree
Differential Gain		V		1		%
Power Supply Requirements						
+V_{CC} Supply Voltage		IV	4.75	5.0	5.25	V
- V_{EE} Supply Voltage		IV	-4.95	-5.2	-5.45	V
+V_{CC} Supply Current		VI		127	151	mA
- V_{EE} Supply Current		VI		202	240	mA
Power Dissipation		VI		1.7	2.0	W
Power Supply Rejection Ratio		IV		30		dB
Digital Inputs						
LINV, MINV		V		CMOS/TTL		Logic
Clock Inputs						
Logic 1 Voltage		VI	-1.1			V
Logic 0 Voltage		VI			-1.5	V
Maximum Input Current Low		VI	-100		+100	μA
Maximum Input Current HIgh		VI	-100		+100	μA
Pulse Width Low (t_{pwl})		IV	4.0		250	ns
Pulse Width High (t_{pwh})		IV	4.0		250	ns
Rise/Fall Time	20% to 80%	IV			1.5	ns
Digital Outputs						
Logic 1 Voltage (ECL)	50 Ω to -2 V, DGND=0.0 V	VI	-1.1	-0.9		V
Logic 0 Voltage (ECL)	50 Ω to -2 V, DGND=0.0 V	VI		-1.7	-1.5	V
Logic 1 Voltage (PECL)	50 Ω to +3 V, DGND=+5.0 V	IV	3.9	4.1		V
Logic 0 Voltage (PECL)	50 Ω to +3 V, DGND=+5.0 V	IV		3.3	3.5	V
t_{rise}	10% to 90%	V		2.0		ns
t_{fall}	10% to 90%	V		2.0		ns

[1]2048 pt FFT using distortion harmonics 2 through 10.
[2]Measured as a second order (f1-f2) intermodulation product from a two-tone test, with each input tone at 0 dBm.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Timing Diagram
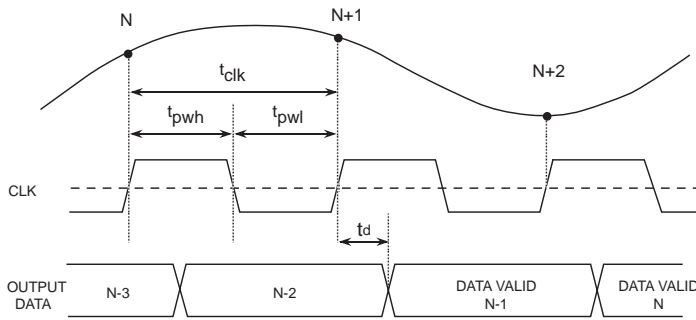
THEORY OF OPERATION

The SPT7870 uses a two stage subranging architecture incorporating a 3-bit flash MSB conversion stage followed by an 8-bit interpolating folder conversion stage. Digital error correction logic combines the results of both stages to produce a 10-bit data conversion digital output.

The analog signal is input directly to the 3-bit flash converter which performs a 3-bit conversion and in turn drives an internal DAC used to set the second stage voltage reference level. The 3-bit result from the flash conversion is input to the digital error correction logic and used in calculation of the upper most significant bits of the data output.

The analog input is also input directly to an internal track-and-hold amplifier. The signal is held and amplified for use in the second stage conversion. The output of this track-and-hold is input into a summing junction that takes the difference between the track-and-hold amplifier and the 3-bit DAC output. The residual is captured by a second track-and-hold which holds and amplifies this residual voltage.

The residual held by the track-and-hold amplifier is input to an 8-bit interpolating folder stage for data conversion. The 8-bit converted data from the folder stage is input into the digital error correction logic and used in calculation of the lower significant bits.

The error correction logic incorporates a proprietary scheme for compensation of any internal offset and gain errors that might exist to determine the 10-bit conversion result. The resultant 10 bit data conversion is internally latched and presented on the data output pins via buffered output drivers.

TYPICAL INTERFACE CIRCUIT

The SPT7870 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7870 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

The SPT7870 requires the use of two supply voltages, V_{EE} and V_{CC}. Both supplies should be treated as analog supply sources. This means the V_{EE} and V_{CC} ground returns of the device

Table I - Data Output Timing Parameters

Timing Parameter	Min	Typ	Max
f_{clock}	2 MHz		100 MHz
Clock Pulse Width High (t_{pwh})	4.0 ns		250 ns
Clock Pulse Width Low (t_{pwl})	4.0 ns		250 ns
Switching Delay (t_d)		3 ns	
Clock Latency		2 clock cycles	

should both be connected to the analog ground plane. All other -5.2 V requirements of the external digital logic circuit should be connected to the digital ground plane. Each power supply pin should be bypassed as closely as possible to the device with .01 µF and 2.2 µF capacitors as shown in figure 2.

The two grounds available on the SPT7870 are AGND and DGND. DGND is used only for ECL outputs and is to be referenced to the output pulldown voltage. These grounds are not tied together internal to the device. The use of ground planes is recommended to achieve the best performance of the SPT7870. The AGND and the DGND ground planes should be separated from each other and only connected together at the device through an inductance or ferrite bead. Doing this will minimize the ground noise pickup.

ANALOG INPUT

The SPT7870 has a single-ended analog input with a bipolar input range from -1 V to +1 V. The bipolar input allows for easier interface by external op amps when compared to unipolar input devices. Because the input common mode is 0 V, the external op amp can operate without a voltage offset on the output, thereby maximizing op amp head room and minimizing distortion.

In addition, the 0 V common mode allows for a very simple DC coupled analog input connection if desired. The current drive requirements for the analog input are minimal when compared to conventional flash converters due to the SPT7870's low input capacitance of only 5 pF and very high input impedance of 150 kΩ.

CLOCK INPUTS

The clock inputs are designed to be driven differentially with ECL levels. For optimal noise performance, the clock input rise time should be a maximum of 1.5 ns. Because of this, the use of *fast* logic is recommended. The analog input signal is latched on the rising edge of the CLK.

The clock may be driven single-ended since the NCLK pin is internally biased to -1.3 V. NCLK may be left open but a .01 µF bypass capacitor from NCLK to AGND is recommended. NOTE: System performance may be degraded due to increased clock noise or jitter.

The performance of the SPT7870 is specified and tested with a 50% clock duty cycle. However, at sample rates greater

than 80 MSPS, additional gains in dynamic performance of the device may be obtained by adjusting the clock duty cycle. Typically, operation between 55 to 60% duty cycle will yield improved results.

INTERNAL VOLTAGE REFERENCE

The SPT7870 incorporates an on-chip voltage reference. The top and bottom reference voltages are each internally tied to their respective top and bottom of the internal reference ladder. The pins for the voltage references and the ladder (including the center of the ladder) are brought out to pins on the device for decoupling purposes only (pins V_T, V_M, and V_B). A .01 µF capacitor should be used on each pin and tied to AGND. See the typical interface circuit (figure 2).

The internal voltage reference and the internal error correction logic eliminate the need for driving externally the voltage reference ladder. In fact, *the voltage reference ladder should not be driven* with an external voltage reference source as the internal error correction circuitry already compensates for the internal voltage and no improvement will result.

DIGITAL OUTPUTS

DIGITAL OUTPUT DATA FORMAT - D0 - D9
D0 is the least-significant bit for the digital data output, and D9 is the most-significant bit. Four data output formats are available and are controlled by the MINV and LINV pins. Table III shows the four possible output formats possible as a function of MINV and LINV. Table II shows the output coding data format versus analog input voltage relationship.

Table II - Output Coding Data Format

V_{IN}	D10	D9…D0 (Binary*)	D9…D0 (2's Comp*)
>+1.0 V	1	11 1111 1111	01 1111 1111
(+FS)	0	11 1111 1111	01 1111 1111
+1.0 V -1 LSB	0	11 1111 1110	01 1111 1110
0.0 V	0	10 0000 0000	00 0000 0000
	0	01 1111 1111	11 1111 1111
-1.0 V +1 LSB	0	00 0000 0001	10 0000 0001
(-FS)	0	00 0000 0000	10 0000 0000
<-1.0 V	0	00 0000 0000	10 0000 0000

*Refer to table III for possible output formats.

OVERRANGE BIT - D10

D10 is the overrange bit which is asserted whenever the analog input signal exceeds the positive full scale input by 1 LSB. When this condition occurs the D10 bit will be asserted to logic high and remain high continuously until the overrange condition is removed from the input.

All other output signals will also stay at their maximum encoded output throughout this condition. D10 is not asserted for an underscale condition when the input exceeds the negative full scale.

DIGITAL OUTPUT DATA TIMING

The data is presented on the output pins two clock cycles after the input is sampled with an additional output delay of typically 3 ns. The data is held valid for one clock cycle. Refer to the timing diagram shown in figure 1.

DIGITAL OUTPUT CONTROL PINS - MINV, LINV

Two digital output control pins control the digital output format. See table III. The MINV pin is a CMOS/TTL-compatible input. It inverts the most-significant bit (D9) when tied to +5 V. The MSB (D9) is noninverted when MINV is tied to ground or floated. The MINV pin is internally pulled down to ground.

The LINV pin is a CMOS/TTL-compatible input. It inverts the least-significant bits (D8 through D0) when tied to +5 V. The least-significant bits (D8 through D0) are noninverted when LINV is tied to ground or floated. The LINV pin is internally pulled down to ground.

Table III - Data Output Bits

MINV	LINV	Description of Data
0 V	0 V	Binary (Noninverted)
0 V	+5 V	Two's Complement (Inverted)
+5 V	0 V	Two's Complement (Noninverted)
+5 V	+5 V	Binary (Inverted)

ECL AND PECL DIGITAL OUTPUT LEVELS

The SPT7870 supports ECL (10K and 100K compatible) and PECL logic levels. It has single-ended output drive capability. ECL termination resistors of 50 Ω to -2 V are required as shown in the typical interface circuit in figure 2. To interface to PECL logic levels, supply +5 V to DGND and terminate the digital outputs through 50 Ω resistors to +3 V.

THERMAL MANAGEMENT

SPT recommends that a heat sink be used for this device to ensure rated performance. A heat sink in still air provides adequate thermal performance under laboratory tests. Air flow may be required for operation at elevated ambient temperature. SPT recommends that the junction temperature be maintained under +150 °C.
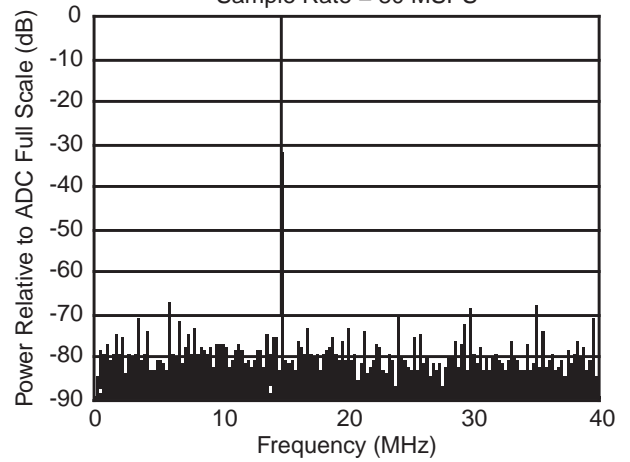
The thermal impedance values for the cerquad package are $\theta_{JC} = 3.3$ °C/W and $\theta_{JA} = 70$ °C/W (junction to ambient in still air with no heat sink).

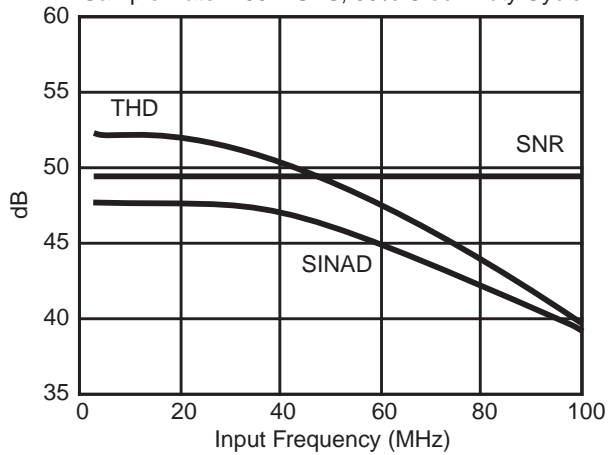# TYPICAL PERFORMANCE CHARACTERISTICS

Dynamic Performance vs. Input Frequency
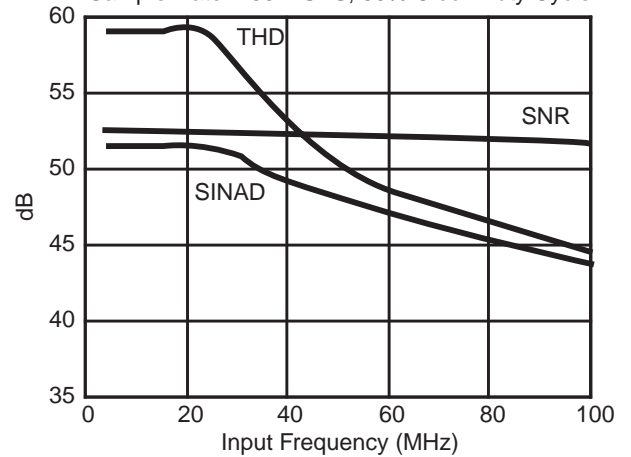**Sample Rate = 80 MSPS**
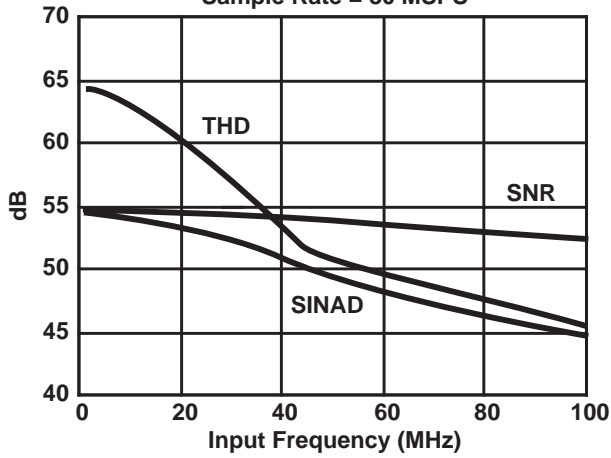
Single Tone at 14.9 MHz
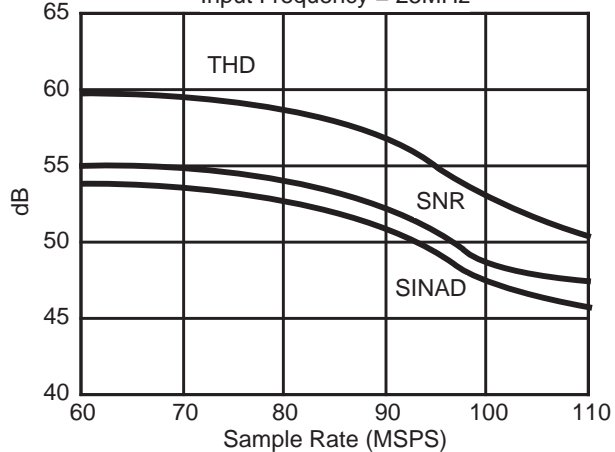Sample Rate = 80 MSPS

Dynamic Performance vs. Input Frequency
Sample Rate=100 MSPS, 50% Clock Duty Cycle

Dynamic Performance vs. Input Frequency
Sample Rate=100 MSPS, 60% Clock Duty Cycle

Dynamic Performance vs. Sample Rate
Input Frequency = 25MHz

Dynamic Performance vs. Temperature
Sample Rate = 80 MSPS
Input Frequency = 25 MHz

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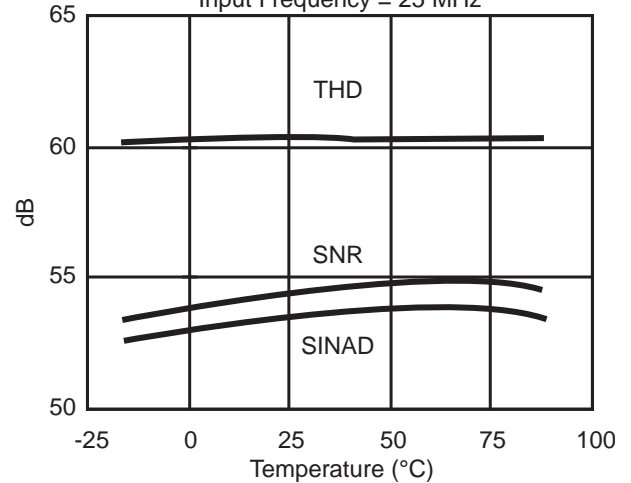
Figure 2 - Typical Interface Circuit
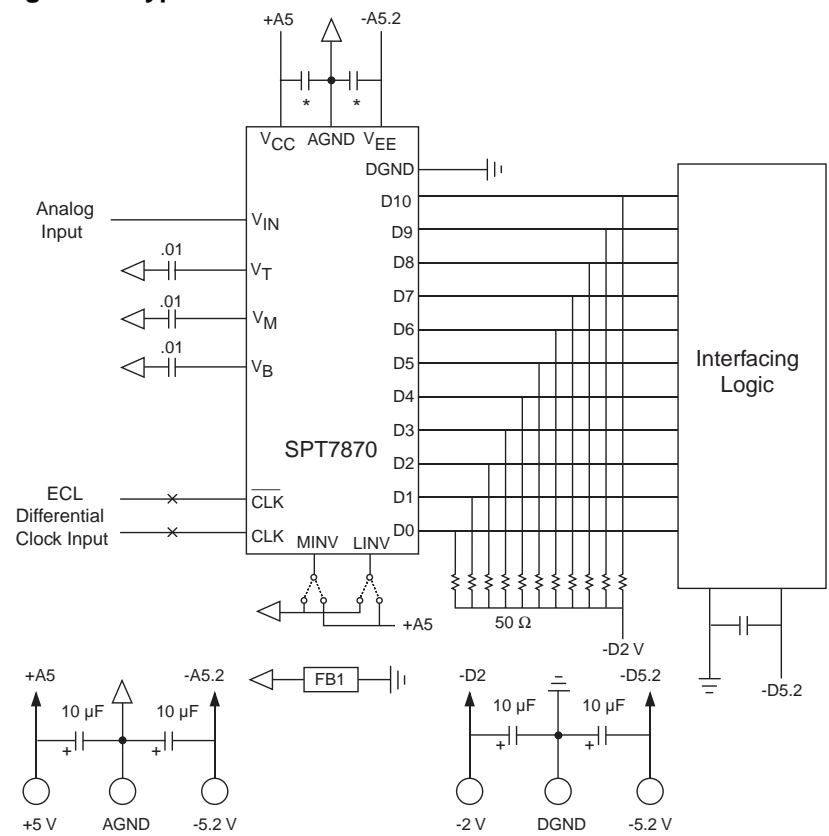
Notes:
1) × = Line termination.

2) * = 0.01 µF chip capacitor in parallel with 2.2 µF Tantalum capacitor.

3) Immediate output buffer is highly recommended to optimize the performance due to reflection.

Figure 3 - SPT7870 Clock Input Equivalent Circuit
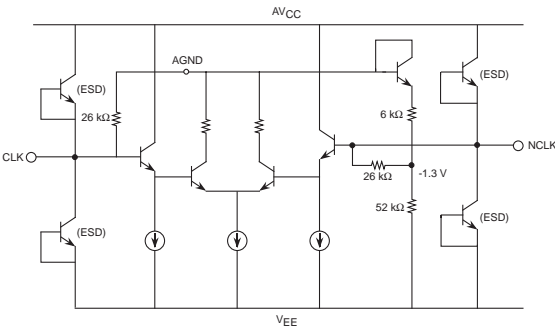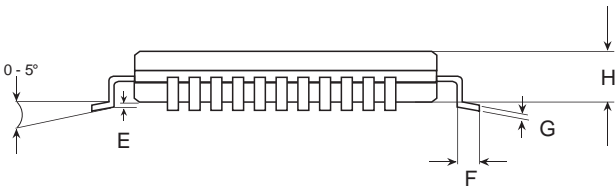

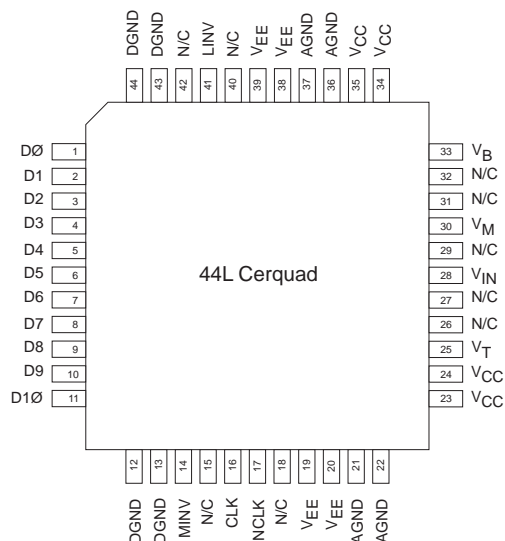**Figure 4 - SPT7870 Digital Outputs Equivalent Circuit**
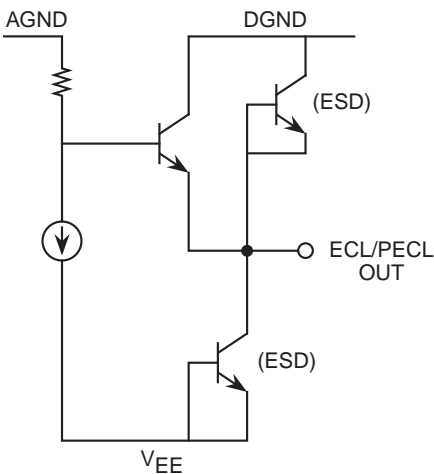
PACKAGE OUTLINE

44L Cerquad
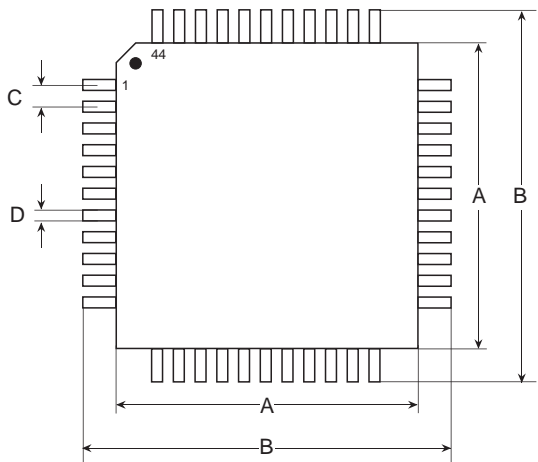
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.550 typ		13.97 typ	
B	0.685	0.709	17.40	18.00
C	0.037	0.041	0.94	1.04
D	0.016 typ		0.41 typ	
E	0.008 typ		0.20 typ	
F	0.027	0.051	0.69	1.30
G	0.006 typ		0.15 typ	
H	0.080	0.150	2.03	3.81

PIN ASSIGNMENTS

44L Cerquad

PIN FUNCTIONS

NAME	I/O	DESCRIPTION
V_{IN}	I	Analog Input
D_0-D_9	O	Digital Output Data (D_0 = LSB)
D_{10}	O	Overflow
CLK	I	Clock (Internal Pull-Down to Ground)
NCLK	I	Inverted Clock (Internal Pull-Down to -1.3 V)
LINV	I	Invert Least Significant Bits (D_0-D_8); CMOS/TTL Level; Invert=+5 V; Internal Pull-Down to Ground
MINV	I	Invert MSB (D_9); CMOS/TTL Level; Invert=+5 V; Internal Pull-Down to Ground
V_T	N/A	Internal Top Reference Decoupling (+1 V typical)
V_M	N/A	Internal Mid-Point Reference Decoupling (0 V typical)
V_B	N/A	Internal Bottom Reference Decoupling (-1 V typical)
V_{CC}	I	+5 V Analog Supply
V_{EE}	I	-5.2 V Supply
N/C	-	Not Connected
AGND	I	Analog Ground
DGND	I	Digital Ground

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SPT7870SIQ	-40 to +85 °C	44L Cerquad
SPT7870SCU	+25 °C	Die*

*Please see the die specification for guaranteed electrical performance.

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