HIGH SPEED CMOS 64K-BIT STATIC RAM

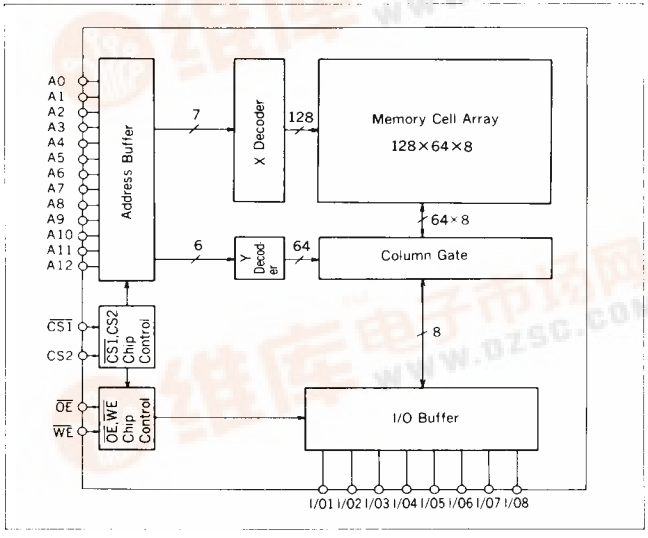
DESCRIPTION

The SRM2264L10/12 is an 8,192 words x 8 bits asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible; and the three-state output allows easy expansion of memory capacity.

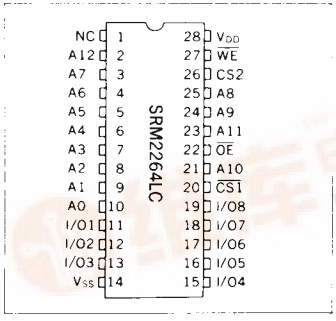
FEATURES

- Fast access time ..... SRM2264L10 100ns (Max)
  SRM2264L12 120ns (Max)
- Low supply current ..... Standby : 0.5μA (Typ)
  Operation: 47mA (Typ) 100ns
  45mA (Typ) 120ns
- Completely static ..... No clock required
- Single power supply ..... 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package ..... SRM2264LC10/12 28-pin DIP(plastic)
  SRM2264LM10/12 28-pin SOP (plastic)

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

A0 to A12	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS1}$, CS2	Chip Select
I/O1 to 8	Data I/O
V_{DD}	Power Supply(+5V)
V_{SS}	Power Supply(0V)
NC	No connection

■ ABSOLUTE MAXIMUM RATINGS

(Vss=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage *	V_I	-0.5 to 7.0	V
Input/Output voltage*	$V_{I/O}$	-0.5 to V_{DD}+O.3	V
Power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature and time	Tsol	260°C, 10s (at lead)	—

* V_I, $V_{I/O}$ (Min) = -1.0V when pulse width is 50 ns

■ RECOMMENDED DC OPERATING CONDITIONS

(V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
	Vss	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	V_{DD} + 0.3	V
	V_{IL}	-0.3 *	—	0.8	V

■ ELECTRICAL CHARACTERISTICS

* If pulse width is less than 50 ns, it is -1.0V

● DC Electrical Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Conditions	SRM2264L10			SRM2264L12			Unit
			Min	Typ*	Max	Min	Typ*	Max	
Input leakage current	I_{LI}	V_I = 0 to V_{DD}	-1	—	1	-1	—	1	μA
Standby supply current	I_{DDS}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}	—	0.5	1.0	—	0.5	1.0	mA
	I_{DDS1}	$\overline{CS1}$=CS2≥V_{DD} -0.2v or CS2≤0.2V	—	0.5	20	—	0.5	20	μA
Average operating current	I_{DDA}	V_I=V_{IL},V_{IH} $I_{I/O}$=0mA t_{cyc}=Min	—	47	82	—	45	80	mA
Operating supply current	I_{DDO}	V_I=V_{IL},V_{IH} $I_{I/O}$=0mA	—	35	60	—	35	60	mA
Output leakage	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, $V_{I/O}$=0 to V_{DD}	-1	—	1	-1	—	1	μA
High level output voltage	V_{OH}	I_{OH}=-1.0mA	2.4	V_{DD}-0.1	—	2.4	V_{DD}-0.1	—	V
Low level output voltage	V_{OL}	I_{OL}=4.0mA	—	0.2	0.4	—	0.2	0.4	V

● Terminal Capacitance

(f = 1MHz, Ta = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address Capacitance	C_{ADD}	V_{ADD} = 0V	—	3	5	pF
Input Capacitance	C_I	V_I = 0V	—	5	6	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	6	7	pF

● AC Electrical Characteristics O Read Cycle

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Conditions	SRM2264L10		SRM2264L12		Unit
			Min	Max	Min	Max	
Read cycle time	tRC	*1	100	—	120	—	ns
Address access time	tACC		—	100	—	120	ns
$\overline{CS1}$ access time	tACS1		—	100	—	120	ns
$\overline{CS2}$ access time	tACS2		—	100	—	120	ns
$\overline{OE}$ access time	tOE		—	50	—	60	ns
$\overline{CS1}$ output set time	tCLZ1	*2	10	—	10	—	ns
$\overline{CS1}$ output floating time	tCHZ1		—	35	—	40	ns
$\overline{CS2}$ output set time	tCLZ2		10	—	10	—	ns
$\overline{CS2}$ output floating time	tCHZ2		—	35	—	40	ns
$\overline{OE}$ output set time	tOLZ		5	—	5	—	ns
$\overline{OE}$ output floating time	tOHZ		—	35	—	40	ns
Output hold time	tOH	*1	10	—	10	—	ns

O Write Cycle

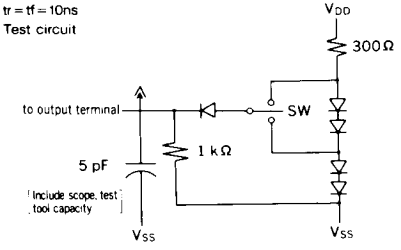
Parameter	Symbol	Conditions	SRM2264L10 Min	SRM2264L10 Max	SRM2264L12 Min	SRM2264L12 Max	Unit
Write cycle time	tWC	*1	100	—	120	—	ns
Chip select time 1	tCW1		80	—	85	—	ns
Chip select time 2	tCW2		80	—	85	—	ns
Address enable time	tAW		80	—	85	—	ns
Address setup time	tAS		0	—	0	—	ns
Write pulse width	tWP		60	—	70	—	ns
Address hold time	tWR		0	—	0	—	ns
Input data setup time	tDW		50	—	50	—	ns
Input data hold time	tDH		0	—	0	—	ns
$\overline{WE}$ output floating	tWHZ	*3	—	35	—	40	ns
$\overline{WE}$ output setup time	tOW		5	—	5	—	ns

*** 1 Test Conditions**

1. Input pulse level : 0.8V to 2.4V
2. tr = tf = 10ns
3. Input and output timing reference levels : 1.5V
4. Output load $I_{TTL} + C_L = 100pF$

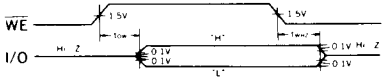
*** 3 Test Conditions**

1. Input pulse level : 0.8V to 2.4V
2. tr = tf = 10ns
3. Test circuit



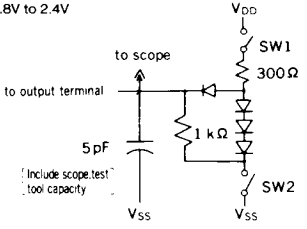
Test : tow, twHZ Hi-Z →"H" and "H" →Hi-Z SW is VDD side
Test : tow, twHZ Hi-Z →"L" and "L" →Hi-Z SW is VSS side

Output turnon turnoff time



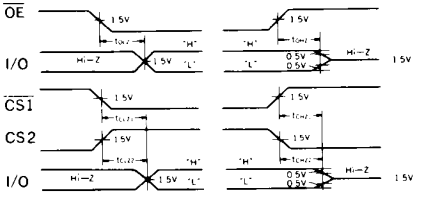
*** 2 Test Conditions**

1. Input pulse level : 0.8V to 2.4V
2. tr = tf = 10ns
3. Test circuit



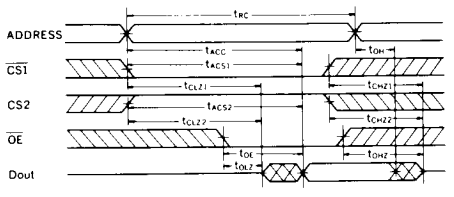
Test : tCHZ1, tCHZ2, tOHZ Both SW1 and SW2 are close
Test : tCLZ1, tCLZ2, tOLZ Hi-Z→"H" SW1 is open, SW2 is close.
Test : tCLZ1, tCLZ2, tOLZ Hi-Z→"L" SW1 is close, SW2 is open.

Output turnon turnoff time

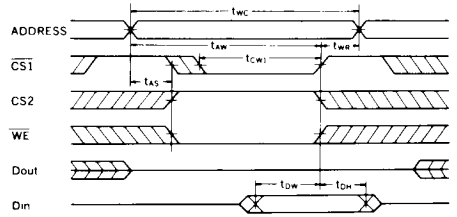


●Timing Chart

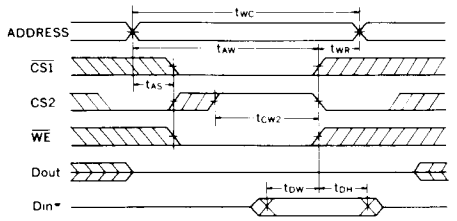
O Read Cycle



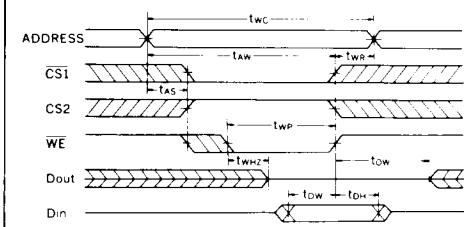
O Write Cycle (1) ($\overline{CS1}$ Control)



○ Write Cycle (2) (CS2 Control)



○ Write Cycle (3) (WE Control)



Note : 1. During read cycle time, $\overline{WE}$ is to be "H" level.
2. During write cycle time that is controlled by $\overline{CS1}$ or CS2, Output Buffer is in high impedance state whether $\overline{OE}$ level is "H" or "L".
3. During write cycle time that is controlled by $\overline{WE}$, Output Buffer is high impedance state if $\overline{OE}$ is "H" level.

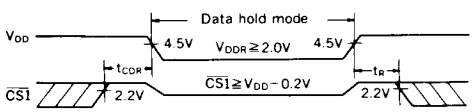
■ DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

(Ta = 0 to 70°C)

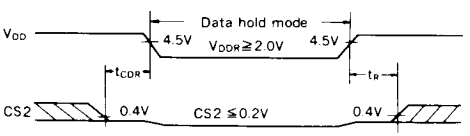
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}		2.0	—	5.5	V
Data retention current	I_{DDR}	V_{DD} = 3V $\overline{CS1}$ = CS2 ≥ V_{DD} − 0.2V or CS2 ≤ 0.2V	—	—	10	μA
Chip select·data hold time	t_{CDR}		0	—	—	ns
Operation recovery time	t_R		t_{RC} *	—	—	ns

* t_{RC} = Read cycle time

Data retention timing ($\overline{CS1}$ Control)



Data retention timing (CS2 Control)



■ FUNCTIONS

● Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	A0 to A12	DATA I/O	Mode	I_{DD}
H	X	—	—	—	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
—	L	—	—	—	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
L	H	X	L	Stable	Input data	Write	I_{DDO}
L	H	L	H	Stable	Output data	Read	I_{DDO}
L	H	H	H	Stable	Hi-Z	Output disable	I_{DDO}

X : "H" or "L", — : "H", "L" or "Hi-Z"

● Reading data

Data is able to be read when the address is setted while holding $\overline{CS1}$ = "L", CS2 = "H", $\overline{OE}$ = "L" and $\overline{WE}$ = "H". Since Data I/O terminals are in high impedance state when $\overline{OE}$ = "H", the data bus line can be used for any other objective, then access time apparently is able to be cut down.

●Writing data

There are the following four ways of writing data into the memory.

(1) Hold $\overline{CS2}$ ="H", $\overline{WE}$="L" set addresses and give "L" pulse to $\overline{CS1}$.

(2) Hold $\overline{CS1}$="L". $\overline{WE}$ ="L", set addresses and give "H" pulse to CS2.

(3) Hold $\overline{CS1}$ = "L", CS2 = "H", set addresses and give "L" pulse to $\overline{WE}$.

(4) After setting addresses, give "L" pulse to $\overline{CS1}$, $\overline{WE}$ and give "H" pulse to CS2.

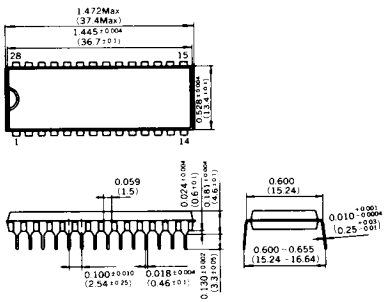
Anyway, data on the Data I/O terminals are latched up into the SRM2264L90/10/12 at the end of the period that $\overline{CS1}$, $\overline{WE}$ are "L" level, and CS2 is "H" level. As Data I/O terminals are in high impedance state when any of $\overline{CS1}$, $\overline{OE}$ = "H", or CS2 = "L", the contention on the data bus can be avoided.

●Standby mode

When $\overline{CS1}$ is "H" or CS2 is "L" level, the SRM2264L90/10/12 is in the standby mode which has retaining date operation. In this case Data I/O terminals are Hi-Z, and all inputs of addresses, $\overline{WE}$ and data can be any "H" or "L". When $\overline{CS1}$ and CS2 level are in the range over V_{DD}-0.2V, or CS2 level is in the range under 0.2V, in the SRM2264L10/12 there is almost no current flow except through the high resistance parts of the memory.

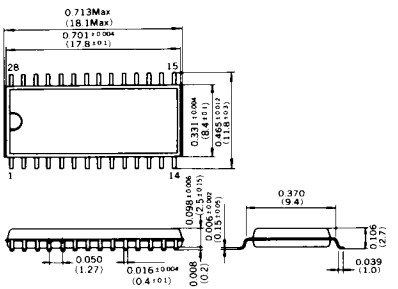
■PACKAGE DIMENSIONS

C28 — 28-pin DIP



unit : inch
(mm)

M28-2 *1 — 28-pin SOP



unit : inch
(mm)

*1 SRM2264LM90/10/12 has the same characteristics as SRM2264LC90/10/12.

■CHARACTERISTICS CURVES