Samsung is a pioneer in the DSP core approach, which is a high performing and flexible family of DSP core based ASDSP(Application Specifics Digital Signal Processor). The DSP core architecture and instruction set are designed simplicity and flexibility. The DSP core contains only the most essential DSP function blocks. Because all internal buses are accessible externally. The ASDSP is an application specifics integrated circuit that incorporates a programmable digital signal processor core. The ASDSP approach allows the system designer to integrate a programmable dsp core, interface logic, peripheral, extra memory into a single integrated circuit. Typically, the custom circuitry on a ASDSP is implemented either in standard cell or gate array. All methods used samsung process by 0.8um double metal CMOS technology.

The SSP1601 uses 0.8um CMOS technology(CSP4H) and can perform up to 25 MHz at 5V. The SSP1601 DSP cores have the following on-chip functions: two independent high-speed RAM banks, a 16 x 16 multiply unit, an 32-bit ALU , RAM address pointers, a status register, a program control unit, and an external bus control unit. The DSP core can address up to 64K-word of external ROM over an external data bus. The actual size of the external ROM area used depends upon the requirements of the individual application. The SSP1601 has five 16-bit buses and one 32-bit bus; program address (PA) bus, program data (PD) bus, multiplier (M) bus, external (EXT) bus, subsidiary (S) bus, data (D) bus, mpya instructions (add, load, multiply, and modify RAM address pointer) are executed efficiently within one machine cycle.The condition flags in the status register (ST) are set or cleared by the corresponding ALU operations. Values for the status register control bits are loaded by application software or through the I/O pins USR0, USR1, ST5, and ST6.
The system stack has six hardware levels and operates using Push and Pop operations. The pins EA[2:0], ESB, and R/WB are used to control the EXT bus, and the RESB, INT0, INT1, INT2, and SS pins are used to control system functions.

Key Features

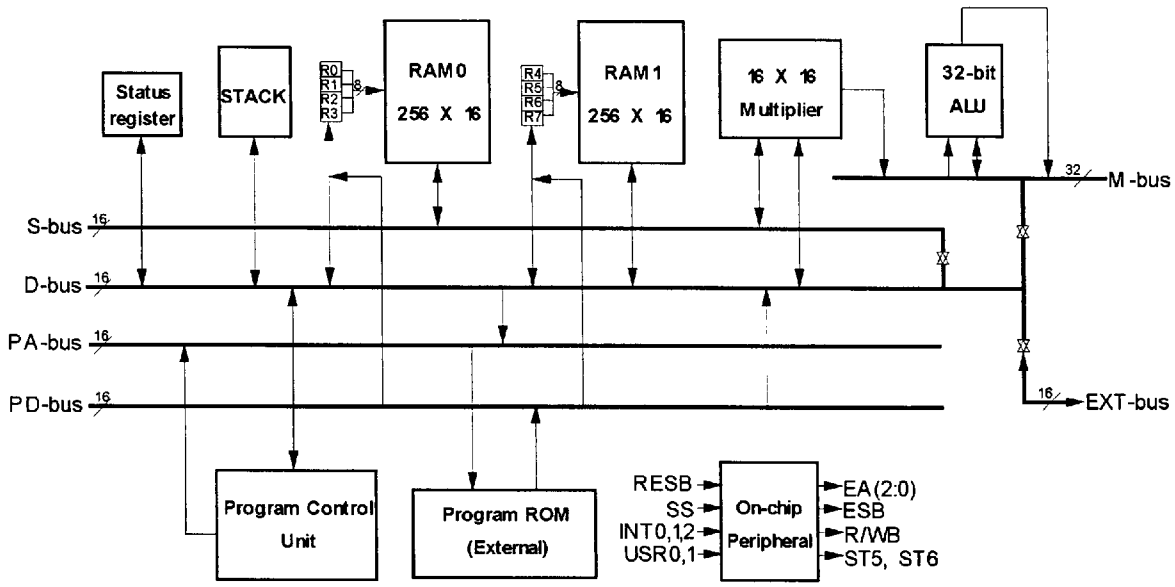
- 16-bit fixed point arithmetic
- ACC + A x B -> ACC; MAC operation in 40 ns using pipelined multiplier
- 16x16-bit pipelined multiply with 32-bit output
- 32-bit ALU operation
- 512-word data RAM ; RAM0, RAM1
- Eight 8-bit RAM point register are existed,
  R0 ~ R3 are for RAM0,
  R4 ~ R7 are for RAM1.
- RAM pointer registers for easy circular buffer operation
- Simple instruction set
- User defined I/Os
- Up to 64K word Program Memory which can be readable and writable
- SSP1601 EVA Chip has two 256-word SRAM for each RAM banks
- 25 MIPS @ 5.0 Volt
- 68 - pin PLCC (evaluation version)
- 0.8um double metal CMOS (CSP4H)
- Excepted core size (except PAD, Data RAM): 3600um x 2400um

Design Tools

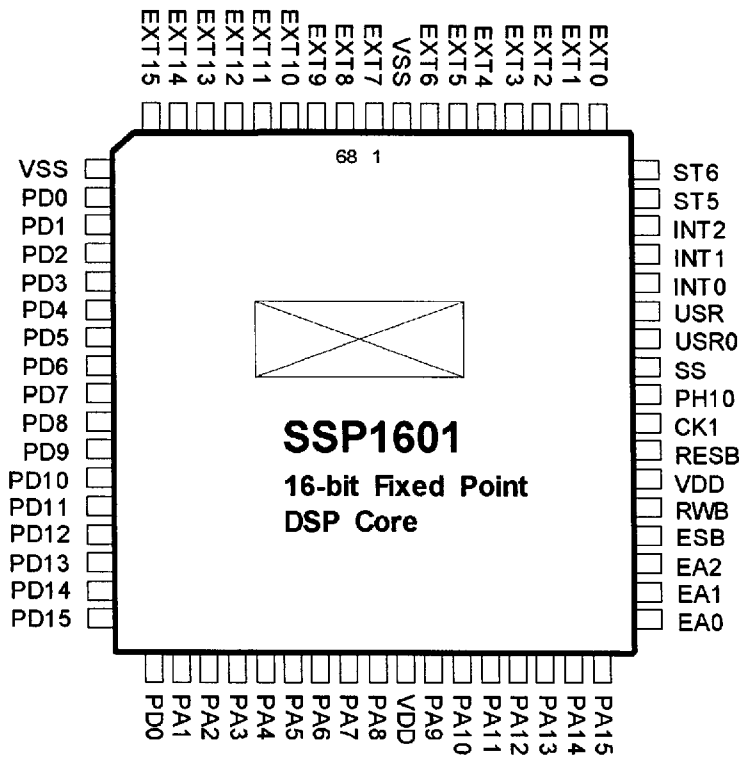
As part of its total support commitment, SASUNG backs up the SSP1601 with a set of high level software and hardware tools.

- Software Tools : running on PC
  - Macro-assembler (MASM1601)
  - Linker (LNK1601)
  - ROM Splitter (RSP1601)
  - Simulator (SIM1601)
- Hardware Tools : running on PC
  - Real-time Emulator (SDE1601)
  - Algorithm Development Board (SDAP1601)
- Design Tools : running on SUN (Unix)
  - Verilog model
  - Macrocells dedicated to the DSP core to build user's applications.
  - Standard cell library, I/O library and Data path generator
  - Memory Generator (ROM, RAM)

Block Diagram



Pin Layout



Pin Descriptions

Name	Number	I/O	Description
CK1	51	I	Clock
PH10B	52	O	Internal clock output Inverted output of PH1 generated from CK1
RESB	50	I	Asynchronous step Effective when CK1 is rising
SS	53	I	Asynchronous single step Effective when CK1 of a cycle is rising
INT0 INT1 INT2	56 57 58	I	Interrupt request 0 Interrupt request 1 Interrupt request 2
PA0-PA15	27-35 & 37-43	O	Program address
PAD0-PD15	11-26	I/O	Program data
EXT0-EXT15	1-9 & 61-68	I/O	External data bus
EA0-EA2	44-46	O	External register address
ESB	47	O	External data strobe
R/WB	48	O	Read/write timing signal for EXT bus
USR0 USR1	54 55	I	User input 0 User input 1
VDD	36,49	I	+ 5 Volt
VSS	10-69	I	GND
ST5 ST6	59 60	O	User output 0 User output 1

Electrical Characteristics

Absolute Maximum Ratings

Characteristics	Symbol	Value	Unit
V_{DD} to V_{SS}	V_{DD}	0.7	V
Input voltage	V_I	V_{DD} + 0.5 to - 0.5	V
Output voltage	V_O	V_{DD} + 0.5 to - 0.5	V
Storage temperature	T_{STG}	-65 to + 150	℃
Lead temperature(Soldering)	T_L	Less than 300	℃

DC Characteristics

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Operating current	I_{DD}	CK = 25 MHz		40		mA
Input voltage high	V_{IH}		$0.9V_{DD}$			V
Output voltage low	V_{IL}				$0.1V_{DD}$	V
Input Leakage current	I_I			1		μA
Output voltage high	V_{OH}	I_{OH} = -100 μA	V_{DD}=0.2			V
Output voltage low	V_{OL}	I_{OL} = 0.5 mA			0.5	V
Output current in high impedance state	I_{OZ}				5	μA

AC Characteristics

AC Characteristics	Symbol	Min	Typ	Max	Unit
Clock cycle time	T_{CY}	1000	40		ns
Clock pulse width	P_{WW}	16			
EA,R/WB delay from CK1	E_{AD}		8		
EXT pre-charge delay from CK1	T_{1P}		10		
EXT floating delay from CK1	T_{1F}		10		
EXT data output delay from CK1	T_{RD}		14		
EXT data output hold from CK1	T_{XH}	6			
EXT data input setup time	T_{XRS}	4			
EXT data input hold time	T_{XRH}	6			
ESB delay time	T_{EWRD}		6		
PA delay from CK1	T_{PAD}		6		
PD input setup time	T_{PDS}		4		
PD input hold time	T_{PDH}	6			
SS setup time	T_{CTLS}	2.5			
SS hold time	T_{CTLH}	6			