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FAIRCHILD SEMICONDUCTOR®

November 2001

SSR2N60B / SSU2N60B

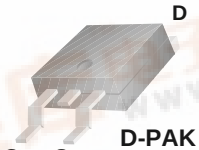
600V N-Channel MOSFET

General Description

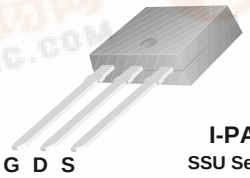
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.

Features

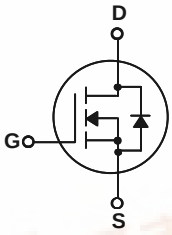
- 1.8A, 600V, $R_{DS(on)}$ = 5.0Ω @V_{GS} = 10 V
- Low gate charge (typical 12.5 nC)
- Low Crss (typical 7.6 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



D-PAK
SSR Series



I-PAK
SSU Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		SSR2N60B / SSU2N60B	Units
V_{DSS}	Drain-Source Voltage		600	V
I_D	Drain Current - Continuous (T_C = 25°C)		1.8	A
	- Continuous (T_C = 100°C)		1.1	A
I_{DM}	Drain Current - Pulsed	(Note 1)	6.0	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	120	mJ
I_{AR}	Avalanche Current	(Note 1)	1.8	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	4.4	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	5.5	V/ns
P_D	Power Dissipation (T_A = 25°C) *		2.5	W
	Power Dissipation (T_C = 25°C)		44	W
	- Derate above 25°C		0.35	W/°C
T_J, T_{stg}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.87	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

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Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	600	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	--	0.65	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	--	--	10	µA
		V_{DS} = 480 V, T_C = 125°C	--	--	100	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 0.9 A	--	3.8	5.0	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 0.9 A (Note 4)	--	1.85	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	380	490	pF
C_{oss}	Output Capacitance		--	35	46	pF
C_{rss}	Reverse Transfer Capacitance		--	7.6	9.9	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 300 V, I_D = 2.0 A, R_G = 25 Ω (Note 4, 5)	--	16	40	ns
t_r	Turn-On Rise Time		--	50	110	ns
$t_{d(off)}$	Turn-Off Delay Time		--	40	90	ns
t_f	Turn-Off Fall Time		--	40	90	ns
Q_g	Total Gate Charge	V_{DS} = 480 V, I_D = 2.0 A, V_{GS} = 10 V (Note 4, 5)	--	12.5	17	nC
Q_{gs}	Gate-Source Charge		--	2.2	--	nC
Q_{gd}	Gate-Drain Charge		--	5.4	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	1.8	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	6.0	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.8 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 2.0 A, dI_F / dt = 100 A/µs (Note 4)	--	250	--	ns
Q_{rr}	Reverse Recovery Charge		--	1.31	--	µC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 68mH, I_{AS} = 2.0A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. $I_{SD} \leq$ 2.0A, di/dt $\leq$ 300A/µs, $V_{DD} \leq BV_{DSS}$, Starting T_J = 25°C
4. Pulse Test : Pulse width $\leq$ 300µs, Duty cycle $\leq$ 2%
5. Essentially independent of operating temperature

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Typical Characteristics

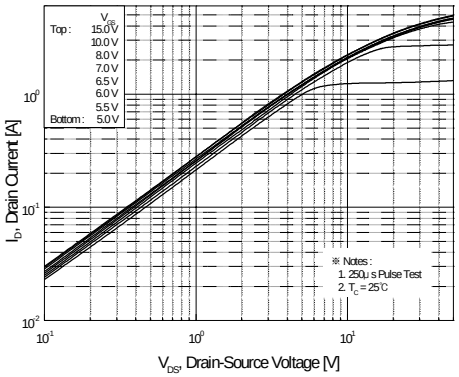

Figure 1. On-Region Characteristics

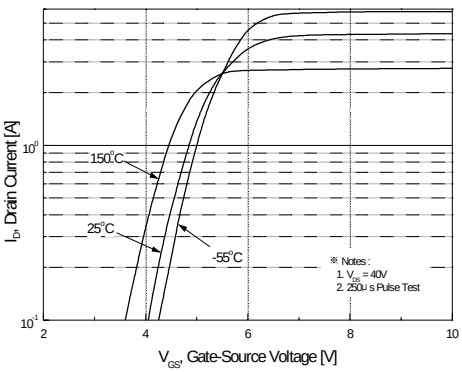

Figure 2. Transfer Characteristics

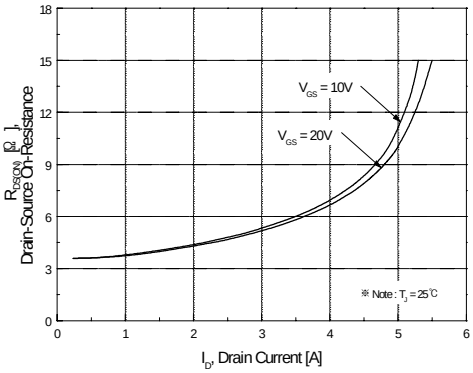

Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

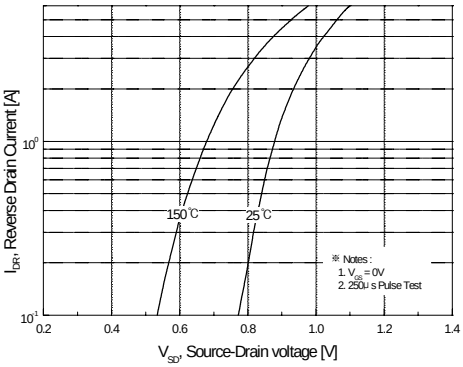

Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

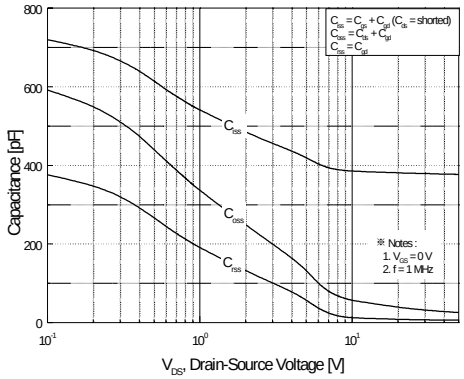

Figure 5. Capacitance Characteristics

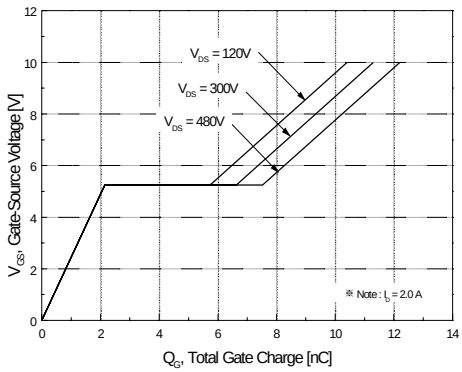

Figure 6. Gate Charge Characteristics

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Typical Characteristics (Continued)

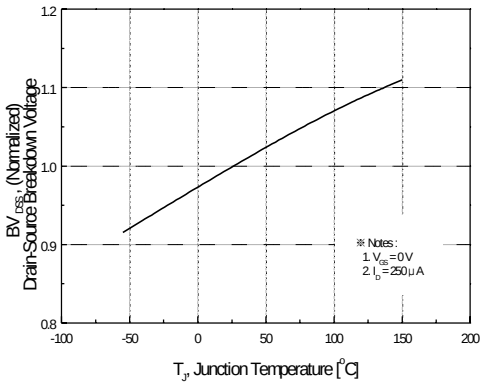


Figure 7. Breakdown Voltage Variation vs Temperature

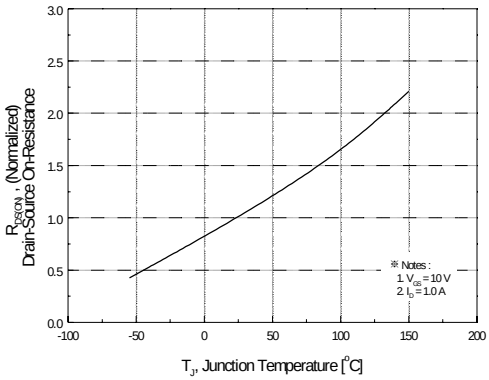


Figure 8. On-Resistance Variation vs Temperature

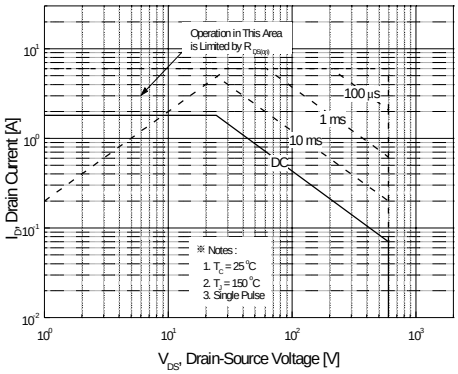


Figure 9. Maximum Safe Operating Area

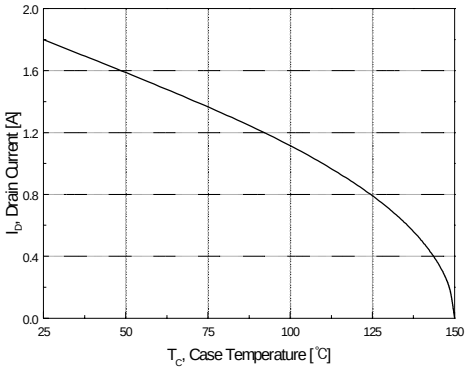


Figure 10. Maximum Drain Current vs Case Temperature

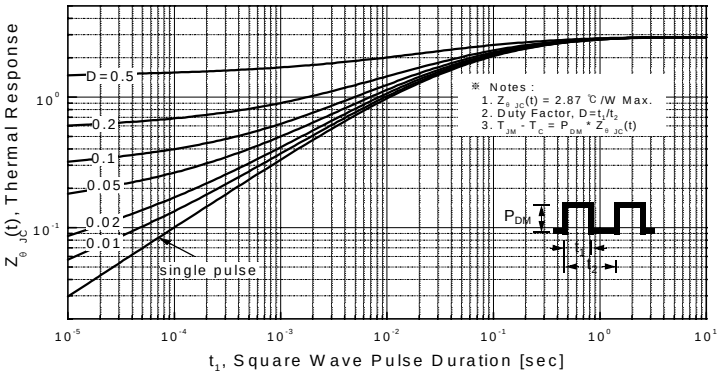
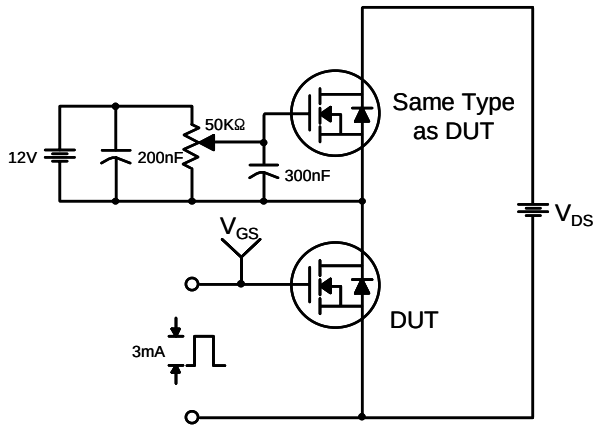
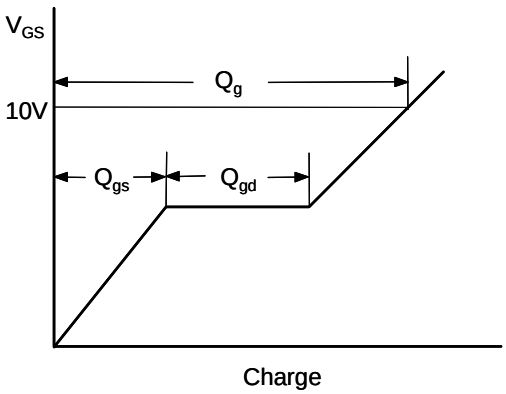


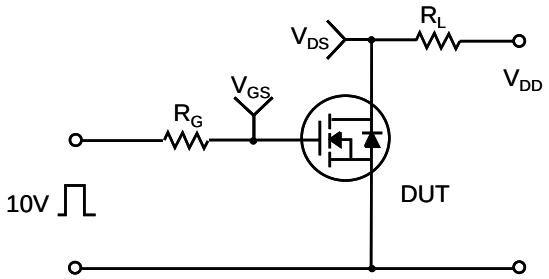
Figure 11. Transient Thermal Response Curve

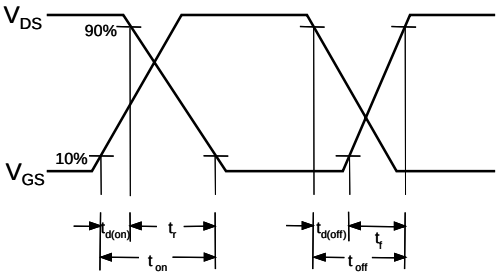
Gate Charge Test Circuit & Waveform



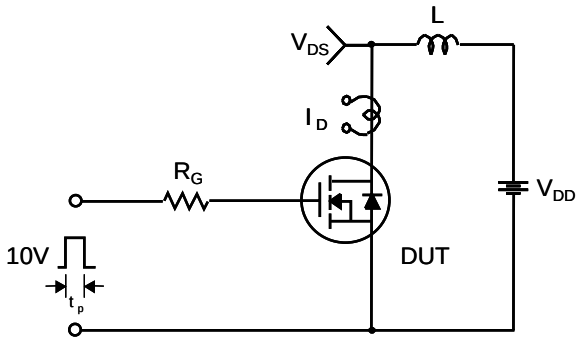


Resistive Switching Test Circuit & Waveforms

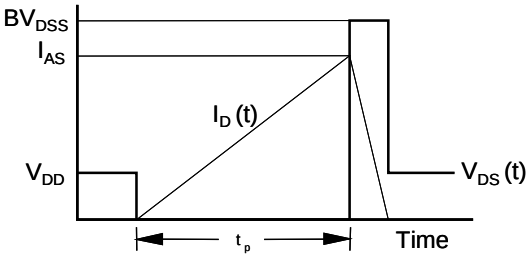




Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



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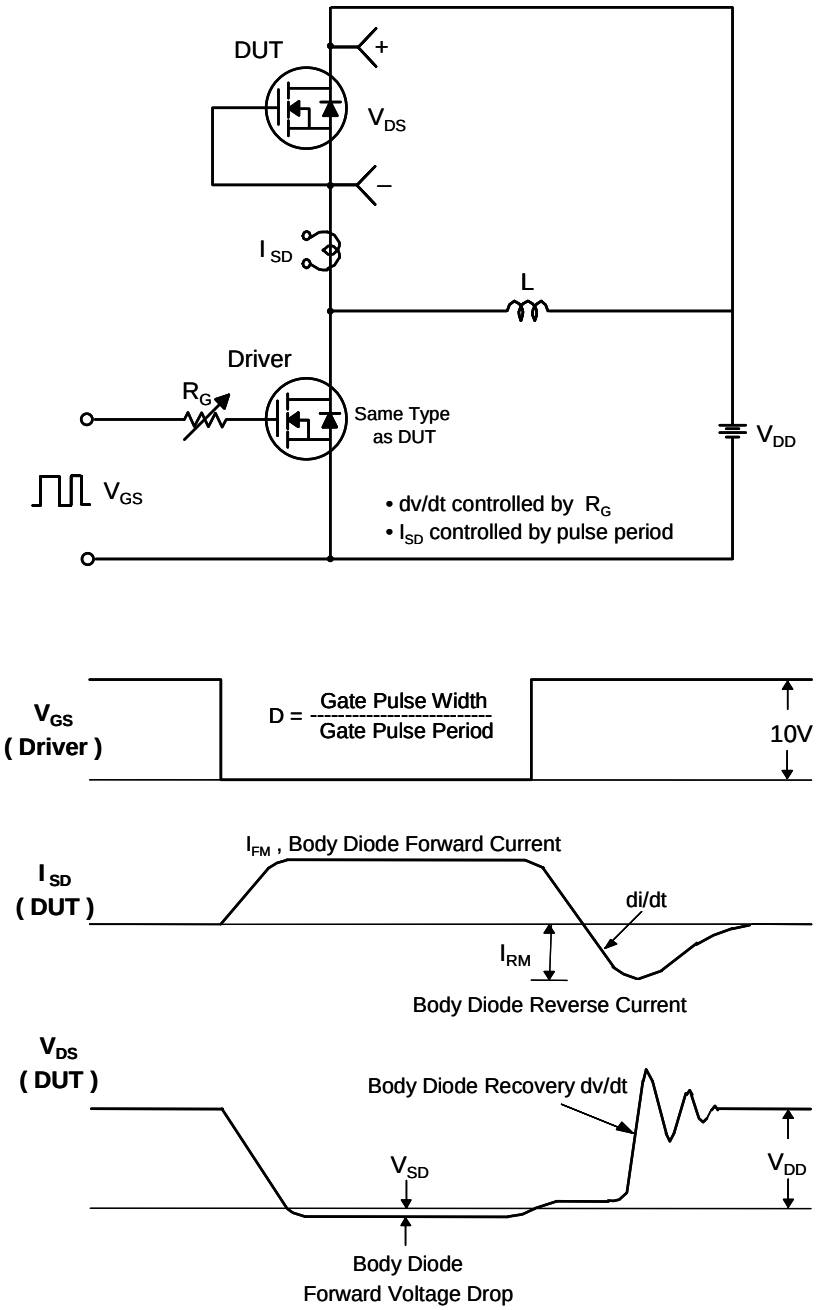
Peak Diode Recovery dv/dt Test Circuit & Waveforms



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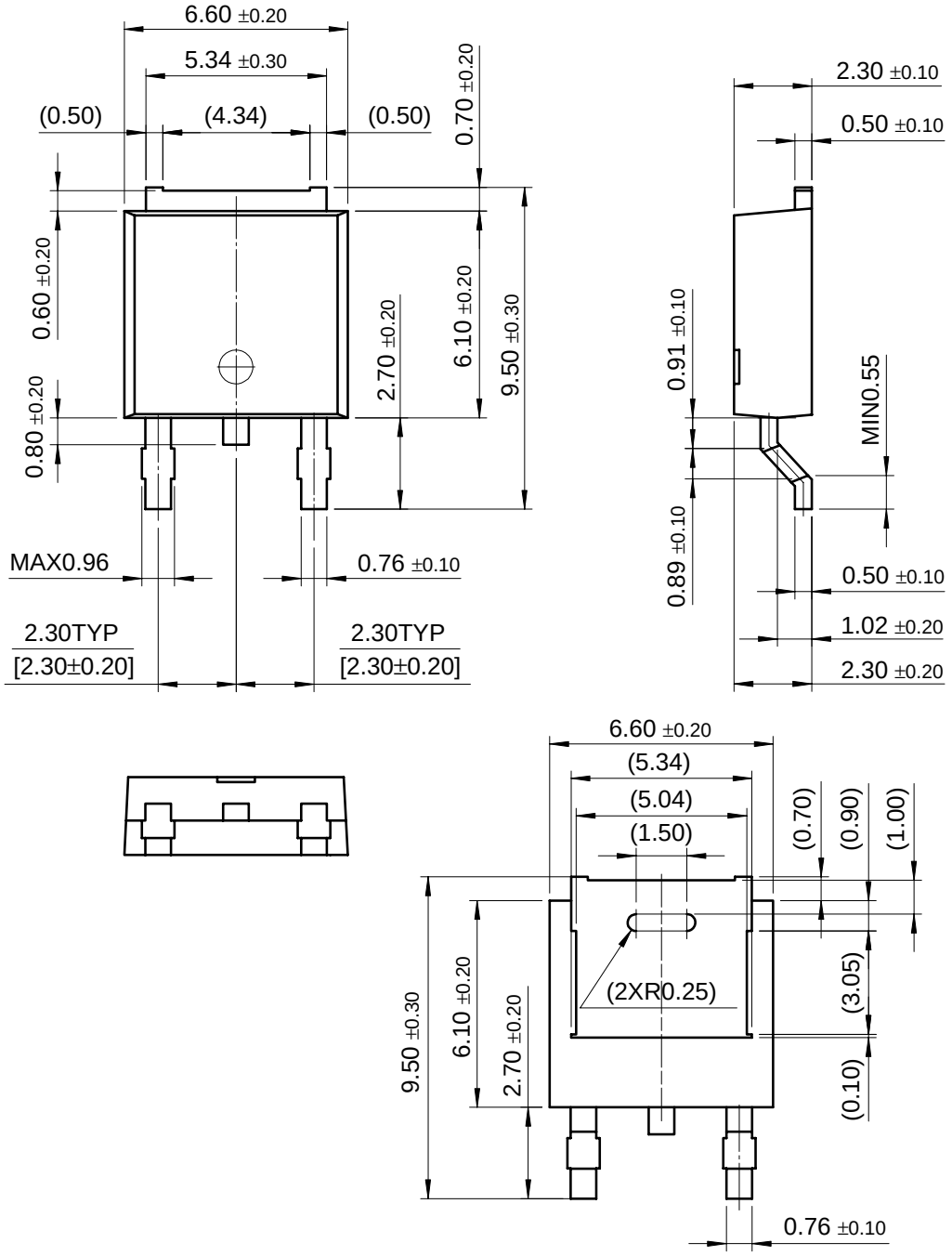
Package Dimensions

D-PAK



Dimensions in Millimeters

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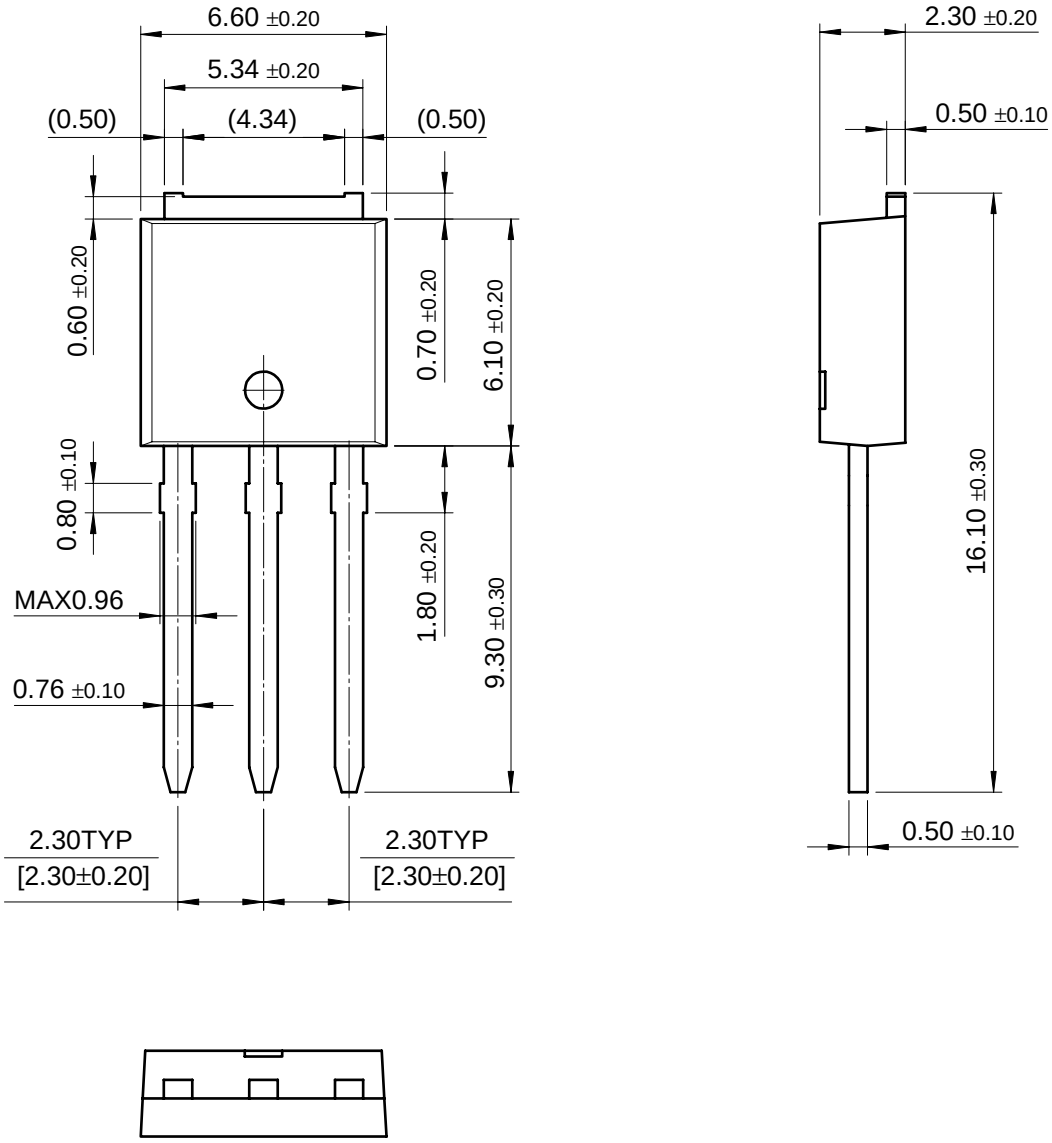
Package Dimensions (Continued)

I-PAK



Dimensions in Millimeters

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