

International IOR Rectifier

ST110S SERIES

PHASE CONTROL THYRISTORS

Stud Version

Features

- Center gate
- Hermetic metal case with ceramic insulator
(Also available with glass-metal seal up to 1200V)
- International standard case TO-209AC (TO-94)
- Threaded studs UNF 1/2 - 20UNF2A
- Compression Bonded Encapsulation for heavy duty operations such as severe thermal cycling

110A

Typical Applications

- DC motor controls
- Controlled DC power supplies
- AC controllers

Major Ratings and Characteristics

Parameters	ST110S	Units
$I_{T(AV)}$	110	A
@ T_c	90	°C
$I_{T(RMS)}$	175	A
I_{TSM} @ 50Hz	2700	A
@ 60Hz	2830	A
I^2t @ 50Hz	36.4	KA ² s
@ 60Hz	33.2	KA ² s
V_{DRM}/V_{RRM}	400 to 1600	V
t_q typical	100	μs
T_J	- 40 to 125	°C



case style
TO-209AC (TO-94)



ST110S Series

ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	Voltage Code	V_{DRM}/V_{RRM} max. repetitive peak and off-state voltage V	V_{RSM} , maximum non-repetitive peak voltage V	I_{DRM}/I_{RRM} max. @ $T_J = T_J$ max mA
ST110S	04	400	500	20
	08	800	900	
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	

On-state Conduction

Parameter	ST110S	Units	Conditions
$I_{T(AV)}$ Max. average on-state current @ Case temperature	110 90	A °C	180° conduction, half sine wave
$I_{T(RMS)}$ Max. RMS on-state current	175	A	DC @ 85°C case temperature
I_{TSM} Max. peak, one-cycle non-repetitive surge current	2700 2830 2270 2380	A	t = 10ms t = 8.3ms t = 10ms t = 8.3ms No voltage reappplied 100% V_{RRM} reappplied Sinusoidal half wave, Initial $T_J = T_J$ max.
I^2t Maximum I^2t for fusing	36.4 33.2 25.8 23.5	KA ² s	t = 10ms t = 8.3ms t = 10ms t = 8.3ms No voltage reappplied 100% V_{RRM} reappplied
$I^2\sqrt{t}$ Maximum $I^2\sqrt{t}$ for fusing	364	KA ² √s	t = 0.1 to 10ms, no voltage reappplied
$V_{T(TO)1}$ Low level value of threshold voltage	0.90	V	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J$ max.
$V_{T(TO)2}$ High level value of threshold voltage	0.92	V	$(I > \pi \times I_{T(AV)})$, $T_J = T_J$ max.
r_{t1} Low level value of on-state slope resistance	1.79	mΩ	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J$ max.
r_{t2} High level value of on-state slope resistance	1.81	mΩ	$(I > \pi \times I_{T(AV)})$, $T_J = T_J$ max.
V_{TM} Max. on-state voltage	1.52	V	$I_{pk} = 350A$, $T_J = T_J$ max, $t_p = 10ms$ sine pulse
I_H Maximum holding current	600	mA	$T_J = 25^\circ C$, anode supply 12V resistive load
I_L Typical latching current	1000		

Switching

Parameter	ST110S	Units	Conditions
di/dt Max. non-repetitive rate of rise of turned-on current	500	A/μs	Gate drive 20V, 20Ω, $t_f \leq 1\mu s$ $T_J = T_J$ max, anode voltage $\leq 80\% V_{DRM}$
t_d Typical delay time	2.0	μs	Gate current 1A, $di_g/dt = 1A/\mu s$ $V_d = 0.67\% V_{DRM}$, $T_J = 25^\circ C$
t_q Typical turn-off time	100		$I_{TM} = 100A$, $T_J = T_J$ max, $di/dt = 10A/\mu s$, $V_R = 50V$ $dv/dt = 20V/\mu s$, Gate 0V 100Ω, $t_f = 500\mu s$

ST110S Series

Blocking

Parameter	ST110S	Units	Conditions
dv/dt Maximum critical rate of rise of	500 off-state voltage	V/μs	$T_J = T_J \text{ max. linear to } 80\% \text{ rated } V_{\text{DRM}}$
I_{RRM} I_{DRM} Max. peak reverse and off-state leakage current	20	mA	$T_J = T_J \text{ max, rated } V_{\text{DRM}}/V_{\text{RRM}}$ applied

Triggering

Parameter	ST110S		Units	Conditions
P_{GM} Maximum peak gate power	5		W	$T_J = T_J \text{ max, } t_p \leq 5\text{ms}$
$P_{\text{G(AV)}}$ Maximum average gate power	1			$T_J = T_J \text{ max, } f = 50\text{Hz, } d\% = 50$
I_{GM} Max. peak positive gate current	2.0		A	$T_J = T_J \text{ max, } t_p \leq 5\text{ms}$
$+V_{\text{GM}}$ Maximum peak positive gate voltage	20		V	$T_J = T_J \text{ max, } t_p \leq 5\text{ms}$
$-V_{\text{GM}}$ Maximum peak negative gate voltage	5.0			
I_{GT} DC gate current required to trigger	TYP.	MAX.	mA	$T_J = -40^\circ\text{C}$ $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ Max. required gate trigger/ current/ voltage are the lowest value which will trigger all units 12V anode-to-cathode applied
	180	-		
	90	150		
	40	-		
V_{GT} DC gate voltage required to trigger	2.9	-	V	$T_J = -40^\circ\text{C}$ $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$
	1.8	3.0		
	1.2	-		
I_{GD} DC gate current not to trigger	10		mA	$T_J = T_J \text{ max}$ Max. gate current/ voltage not to trigger is the max. value which will not trigger any unit with rated V_{DRM} anode-to-cathode applied
V_{GD} DC gate voltage not to trigger	0.25		V	

Thermal and Mechanical Specification

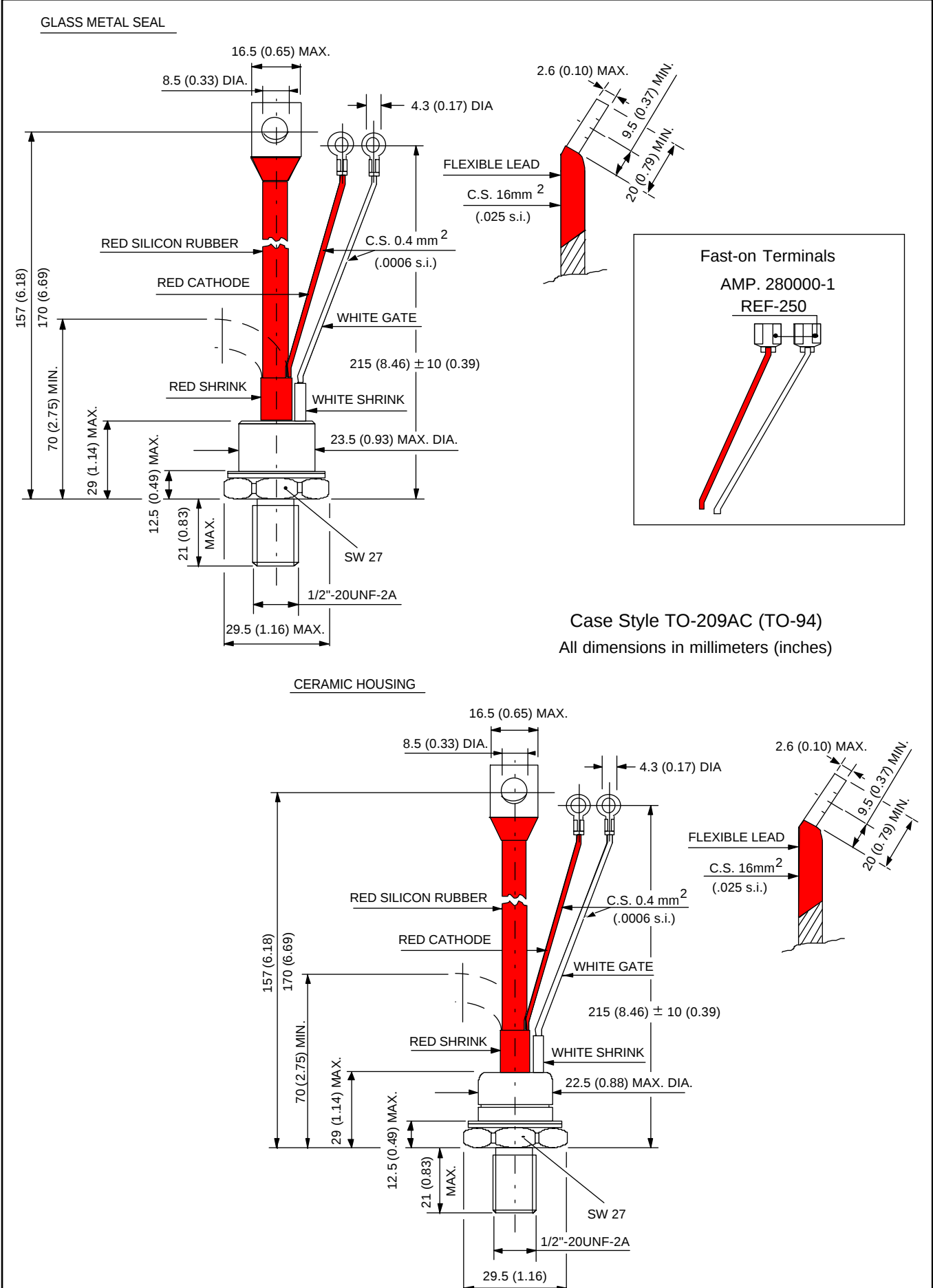
Parameter	ST110S	Units	Conditions
T_J Max. operating temperature range	-40 to 125	$^\circ\text{C}$	
T_{stg} Max. storage temperature range	-40 to 150		
R_{thJC} Max. thermal resistance, junction to case	0.195	K/W	DC operation
R_{thCS} Max. thermal resistance, case to heatsink	0.08		Mounting surface, smooth, flat and greased
T Mounting torque, $\pm 10\%$	15.5	Nm (lbf-in)	Non lubricated threads
	(137)		
	14 (120)		Lubricated threads
wt Approximate weight	130	g	
Case style	TO - 209AC (TO-94)		See Outline Table

Device Code

ST	11	0	S	16	P	0	V	
1	2	3	4	5	6	7	8	9

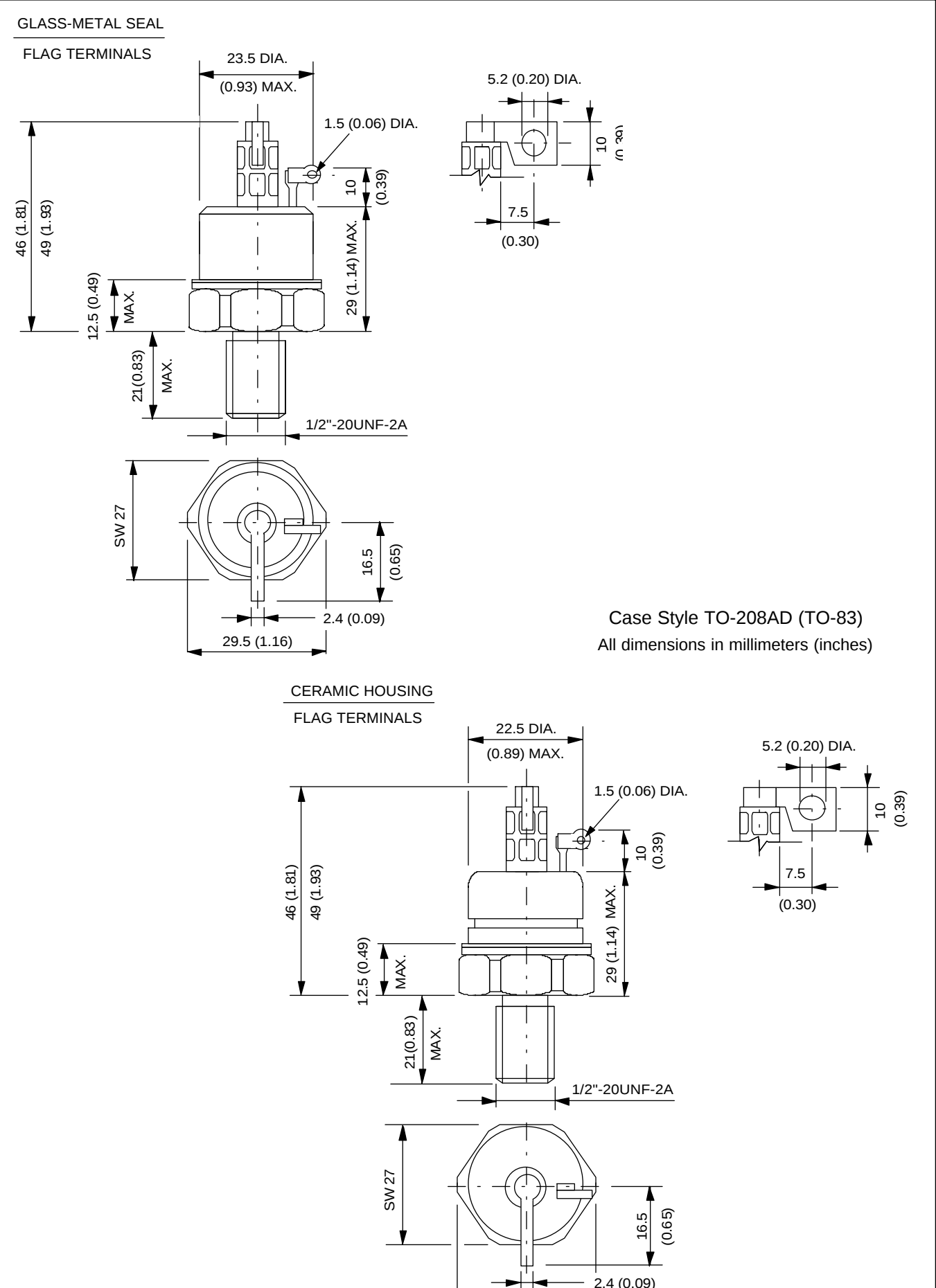
- 1** - Thyristor
- 2** - Essential part number
- 3** - 0 = Converter grade
- 4** - S = Compression bonding Stud
- 5** - Voltage code: Code x 100 = V_{RRM} (See Voltage Rating Table)
- 6** - P = Stud base 20UNF threads
- 7** - 0 = Eyelet terminals (Gate and Auxiliary Cathode Leads)
1 = Fast - on terminals (Gate and Auxiliary Cathode Leads)
2 = Flag terminals (For Cathode and Gate Terminals)
- 8** - V = Glass-metal seal (only up to 1200V)
None = Ceramic housing (over 1200V)
- 9** - Critical dv/dt: None = 500V/ μ sec (Standard value)
L = 1000V/ μ sec (Special selection)

Outline Table



ST110S Series

Outline Table



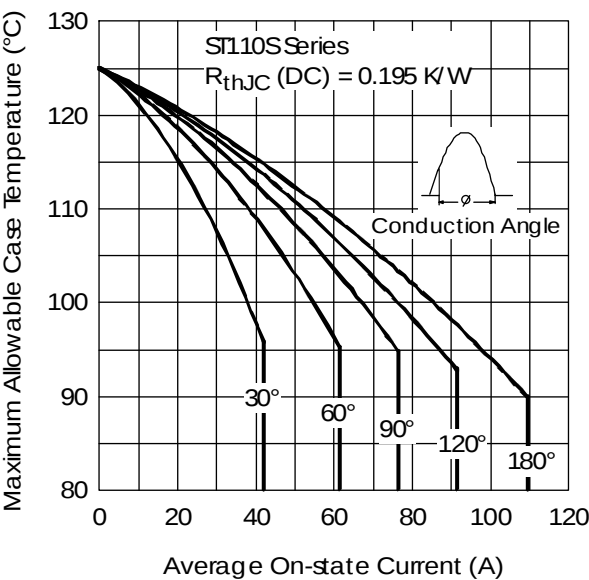


Fig. 1 - Current Ratings Characteristics

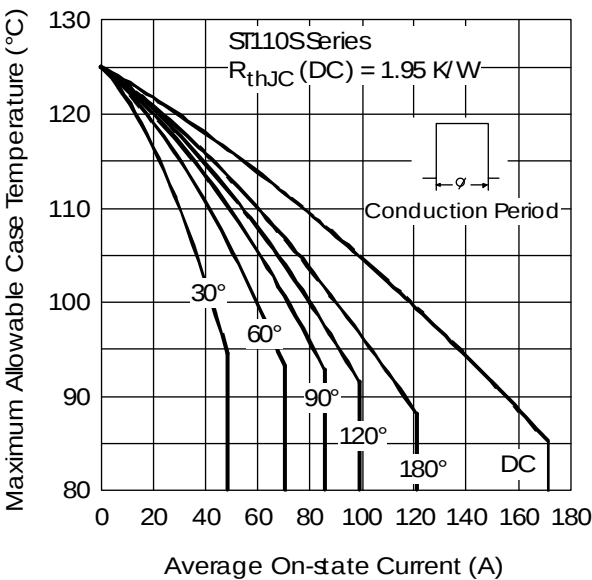


Fig. 2 - Current Ratings Characteristics

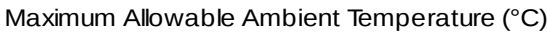
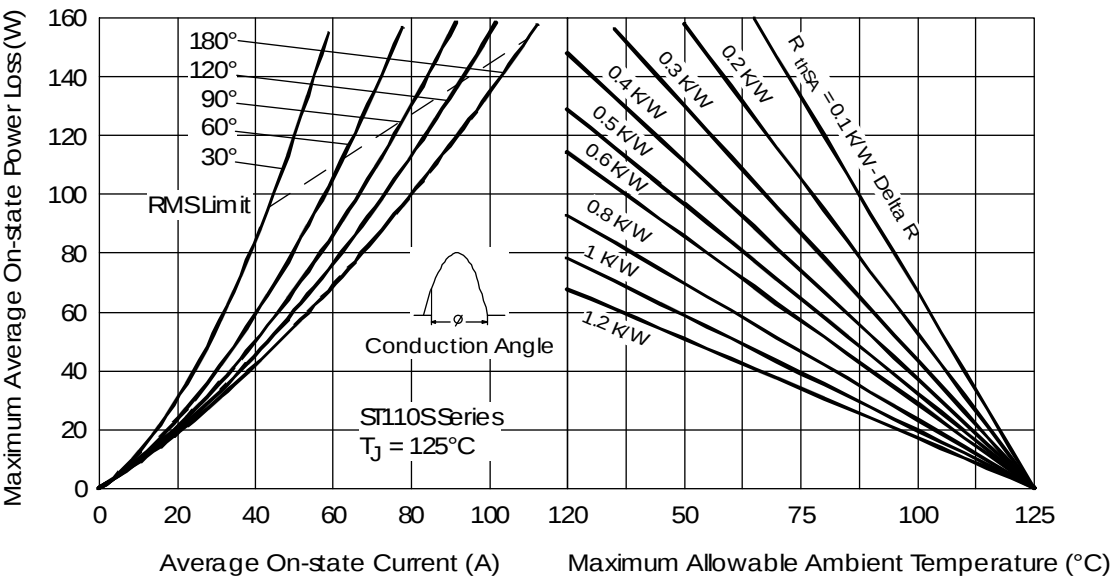
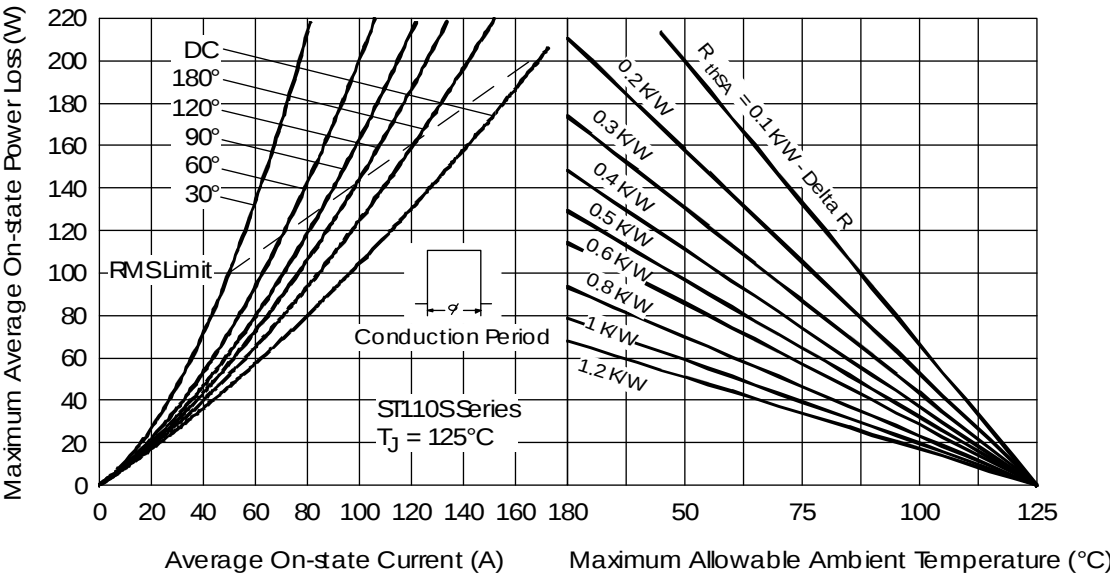


Fig. 3 - On-state Power Loss Characteristics



ST110S Series

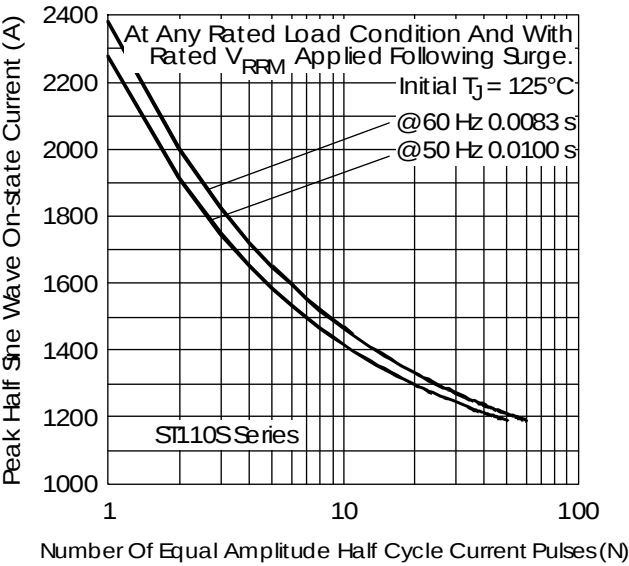


Fig. 5 - Maximum Non-Repetitive Surge Current

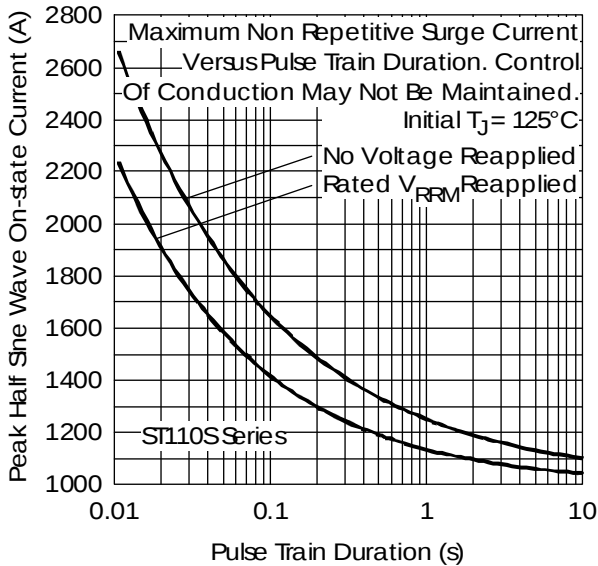


Fig. 6 - Maximum Non-Repetitive Surge Current

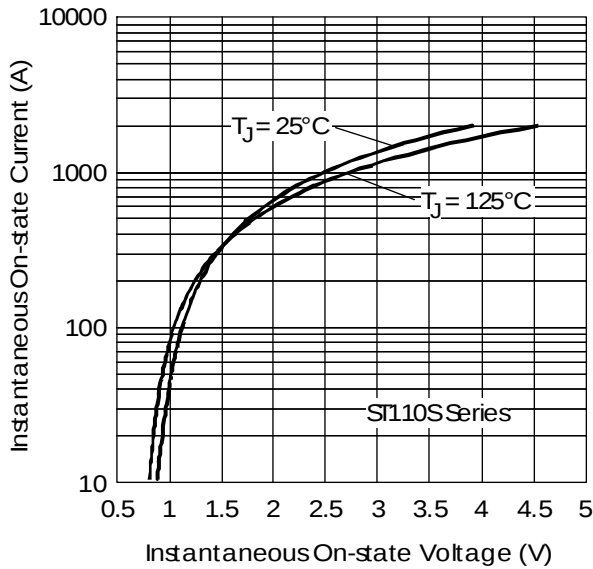
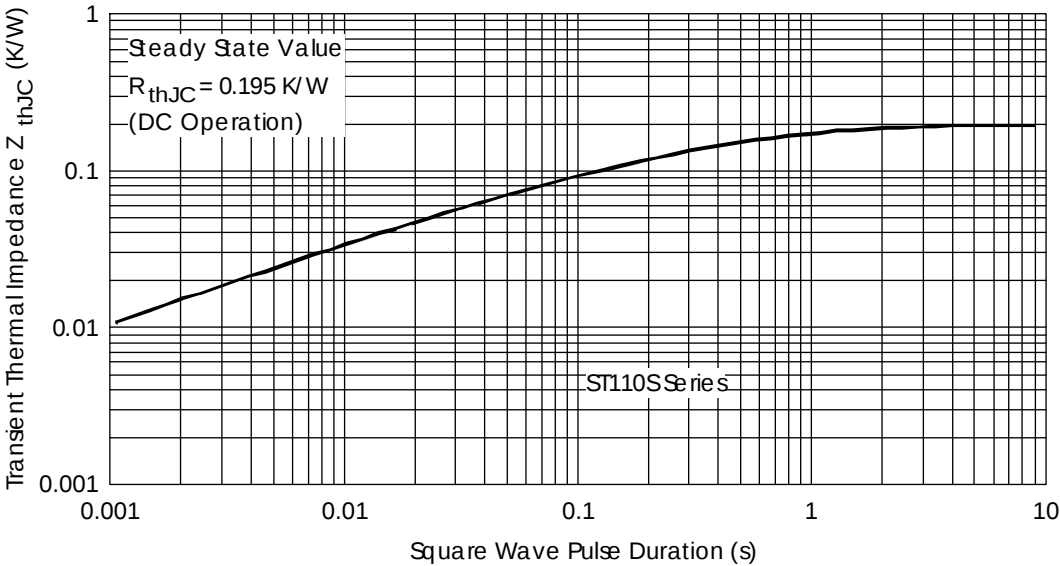


Fig. 7 - On-state Voltage Drop Characteristics



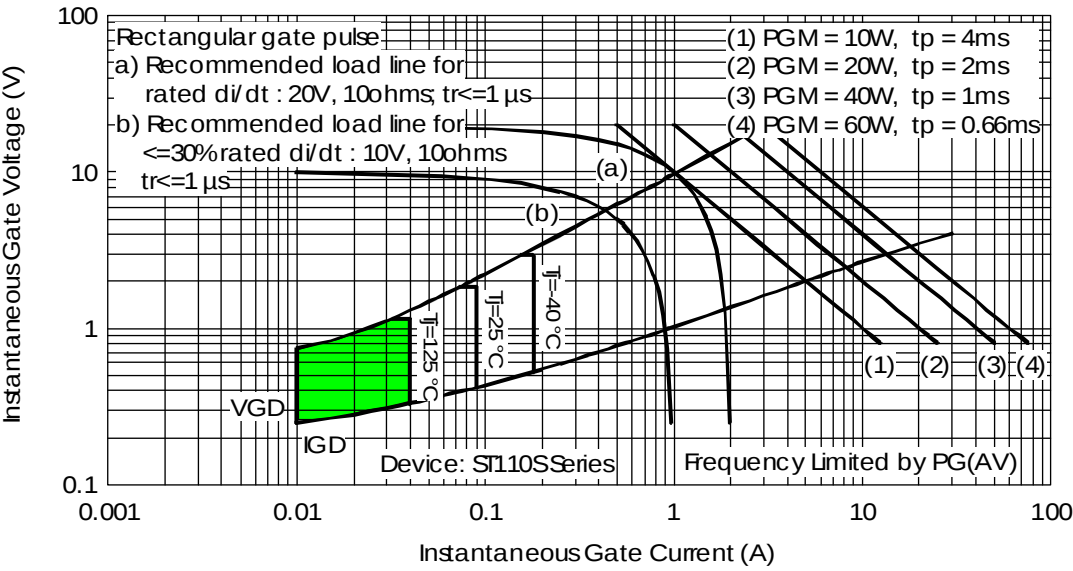


Fig. 9 - Gate Characteristics