



A.S.D.™

ST1284-xxA8/T8

PARALLEL PORT SINGLE TERMINATION NETWORK WITH ±15kV ESD PROTECTION

MAIN APPLICATIONS

ECP/EPP Parallel Port termination on:

- Desktops
- Notebooks
- Workstations
- Servers
- PC Peripherals
- Set Top Box

FEATURES

- One device for parallel port termination
- Compliant with IEEE1284 standard
- EMI / RFI noise filtering
- Highly integrated solution in 28 pin QSOP and TSSOP packages
- One single device provides the proper termination for 8 datalines, 1 strobe line, 4 control lines and 4 status lines
- In system ESD protection of ±15 kV (air discharge) as per IEC61000-4-2 level 4

DESCRIPTION

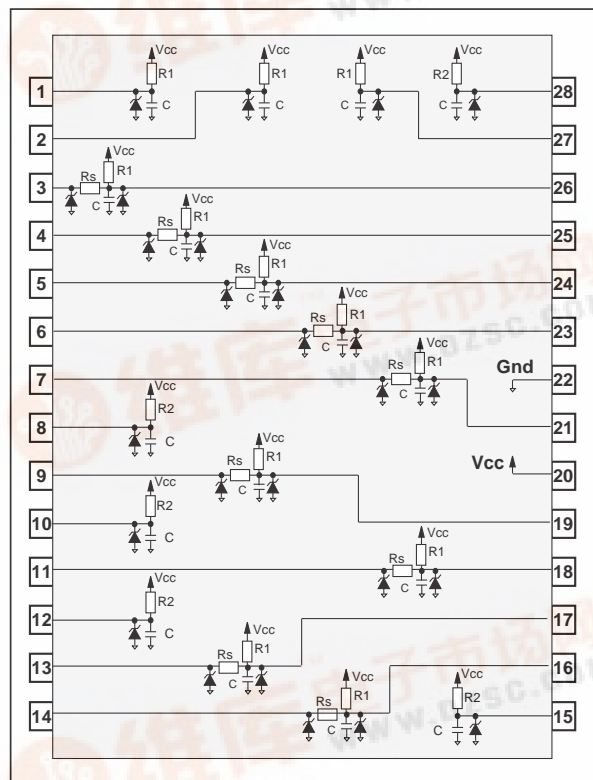
The ST1284-xxA8/T8 is a highly integrated termination for enhanced high speed parallel ports. The integrated termination complies to the IEEE1284 Standard recommendations and government EMC compatibility requirements. It is built around two basic cells. The first one (Cell 1) provides line termination, EMI filtering and ESD protection for the Strobe and Datalines while the second one (Cell 2) provides EMI filtering and ESD protection for the Control and Status lines. In addition, ST1284-xxA8 provides extra protection against ESD. When tested according to IEC61000-4-2, they withstand ±8kV contact discharges and ±15kV air-discharges, thereby providing to the system the necessary robustness to meet up to level 4 of IEC61000-4-2, without the need for additional ESD protection components. Cells 1 and 2 are described in more detail in figures 1 and 2.

COMPLIES WITH THE FOLLOWING ESD STANDARDS :

- IEC61000-4-2 ±15kV (air discharge)
± 8kV (contact discharge)
- MIL STD 883E - Method 3015-7 : Class 3 (human body model).



SCHEMATIC DIAGRAM



	R1	R2	Rs	C
Code 01	4.7kΩ	4.7kΩ	33Ω	180pF
Code 02	2.2kΩ	2.2kΩ	33Ω	220pF
Code 03	1kΩ	5.1kΩ	39Ω	150pF
Tolerance	± 10%	± 10%	± 10%	± 20%

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25°C)

Symbol	Parameter	Value	Unit
V _{PP}	ESD discharge IEC61000-4-2, air discharge	±16	kV
	ESD discharge IEC61000-4-2, contact discharge	±9	kV
	ESD discharge - MIL STD 883E - Method 3015-7	±25	kV
V _{CC}	Supply voltage	5.5	V
P _r	Power rating per resistor	100	mW
P _P	Package Power rating	1	W
T _{op}	Operating temperature range	0 to +70	°C
T _{stg}	Storage temperature range	-55 to +150	°C
T _j	Maximum operating junction temperature	125	°C

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I _R	Leakage current	V _{CC} = 5.0V			10	µA
V _{BR}	Breakdown voltage	I _R = 1mA	6			V
V _F	Forward voltage drop	I _F = 50mA		0.9		V

BASIC CELL CONFIGURATIONS

The ST1284-xxA8/T8 is built around the two basic cells described below which integrate the recommended IEEE1284 network and the ESD protection compatible with IEC61000-4-2 level 4

Fig. 1: Cell 1 for line termination, EMI filtering and ESD protection for the Datalines and Strobe signals. There are 9 of these cells inside the ST1284-xxA8/T8

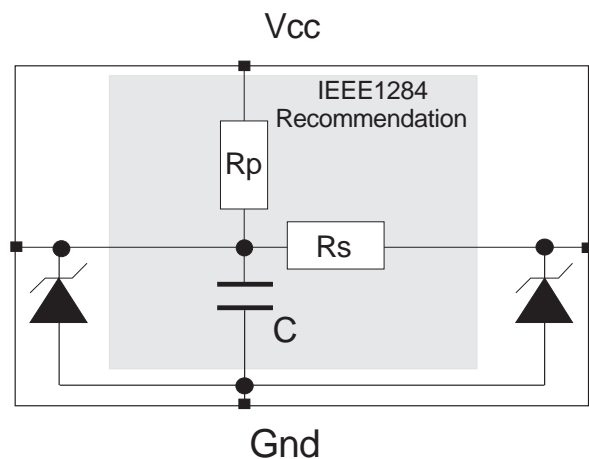
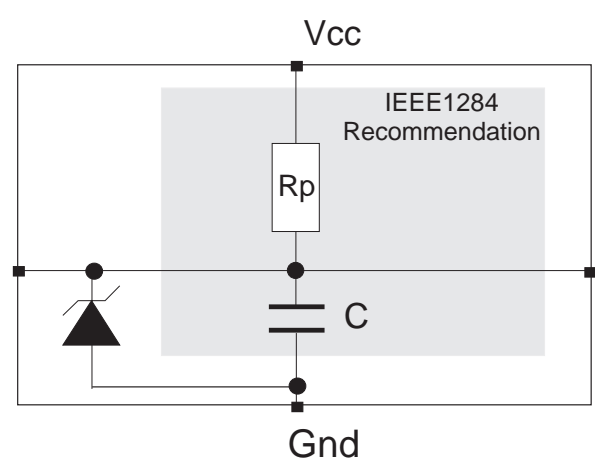
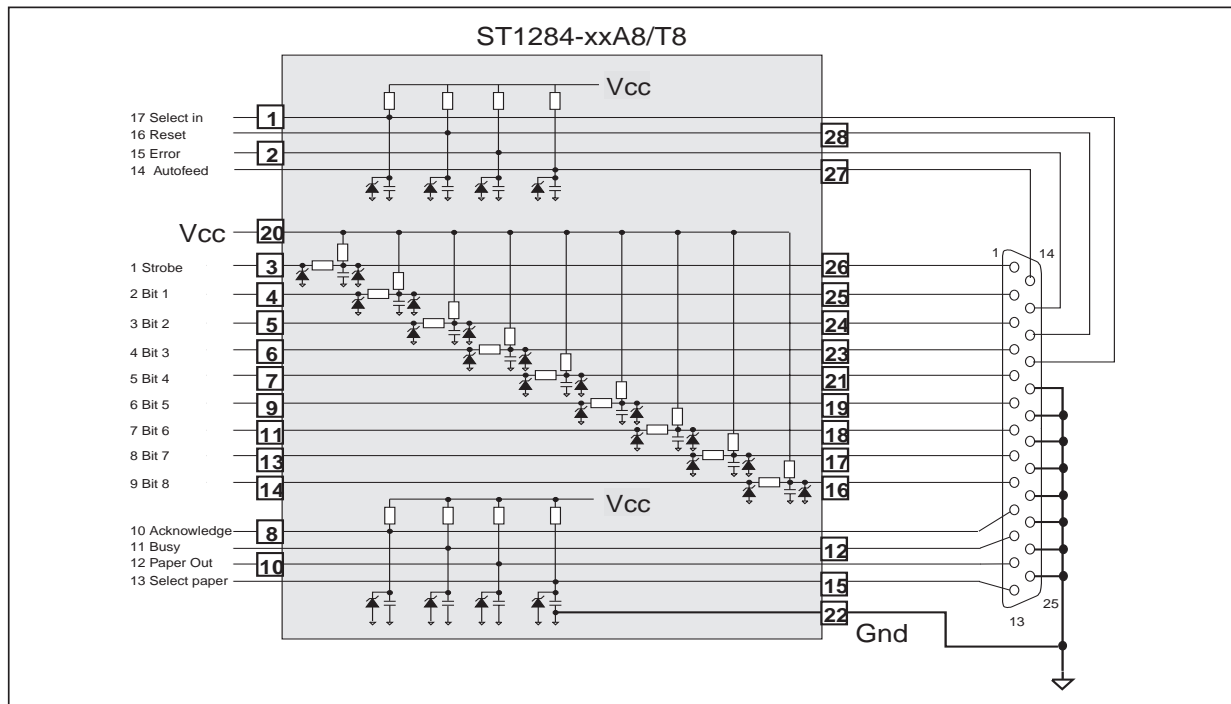


Fig. 2: Cell 2 for EMI filtering and ESD protection of the Control and Status signals. There are 8 of these cells inside the ST1284-xxA8/T8



FUNCTIONAL DIAGRAM



APPLICATION INFORMATION

The functional diagram here above presents a IEEE1284-A connector pinout and show how to connect the ST1284-xxA8/T8 in order to correctly terminate and filter the 17 signal lines. The IEEE1284-A connector is the PC standard for the host connection.

Control and status lines (from 10 to 17) only require a pull-up resistor (R_p) and a filter capacitor (C).

The data lines (from 2 to 9) and the STROBE (pin 1) also require a termination series resistor (R_s) in addition to the pull-up resistor and a filter capacitor. The Vcc is connected to pin 20 and the ground to pin 22.

The ST1284-xxA8/T8 can be used with all 3 types of connectors defined in the IEEE1284 standard:

- IEEE1284-A is a 25DB connector which is the PC standard for the host connection.
- IEEE1284-B is a 36 pin, 0.085 inch centerline connector used on the peripheral device.
- IEEE1284-C is a new 36 pin, 0.050 inch centerline connector which can be used for both host and peripherals.

TECHNICAL INFORMATION

FREQUENCY BEHAVIOR OF DATA AND STROBE SIGNALS

Fig. A1: Measurement conditions

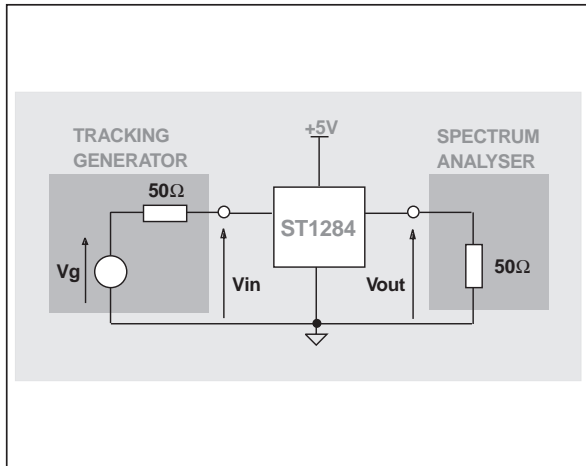
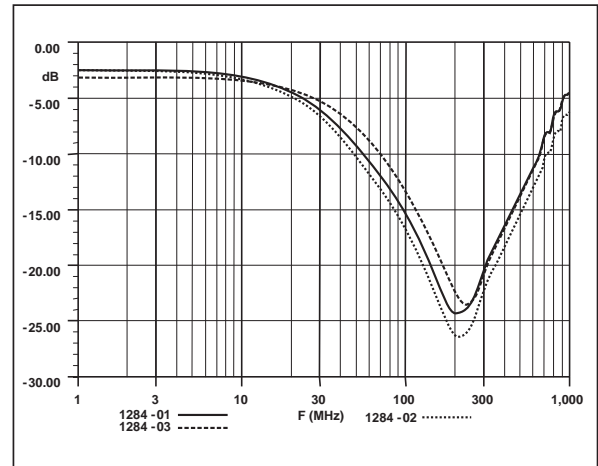


Fig. A2: Typical frequency response curve for data and strobe signals.



ESD PROTECTION

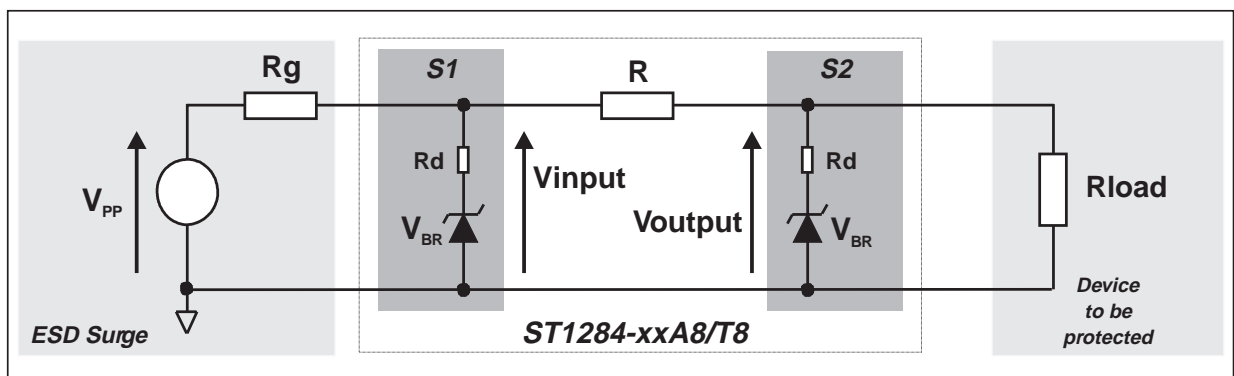
In addition to the requirements of termination and EMC compatibility, computing devices are required to be tested for ESD susceptibility. This test is described in the IEC61000-4-2 and is already in place in Europe. This test requires that a device tolerates ESD events and remain operational without user intervention.

The ST1284-xxA8/T8 is particularly optimized to perform ESD protection. ESD protection is based on the use of device which clamps at :

$$V_{output} = V_{BR} + R_d \cdot I_{PP}$$

This protection function is splitted in 2 stages. As shown in figure A3, the ESD strikes are clamped by the first stage S1 and then its remaining overvoltage is applied to the second stage through the resistor R. Such a configuration makes the voltage very low at the output.

Fig. A3: ST1284 ESD clamping behavior



To have a good approximation of the remaining voltages at both Vin and Vout stages, we give the typical dynamical resistance value Rd. By taking into account these following hypothesis : $R_t > R_d$, $R_g > R_d$ and $R_{load} > R_d$, it gives these formulas:

$$V_{input} = \frac{R_g \cdot V_{BR} + R_d \cdot V_{PP}}{R_g}$$

$$V_{output} = \frac{R_t \cdot V_{BR} + R_d \cdot V_{input}}{R_t}$$

The results of the calculation done for $V_{PP}=8kV$, $R_g=330\Omega$ (IEC61000-4-2 standard), $V_{BR}=7V$ (typ.) and $R_d = 1\Omega$ (typ.) give:

$$V_{input} = 31.2 V$$

$$V_{output} = 7.95 V$$

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be few tenths of volts during few ns at the input side. This parasitic effect is not present at the output side due the low current involved after the resistance R.

The measurements done here after show very clearly (Fig. A5) the high efficiency of the ESD protection :

- no influence of the parasitic inductances on Vout stage
- Voutput clamping voltage very close to V_{BR} (positive strike) and $-V_F$ (negative strike)

Fig. A4: Measurement conditions

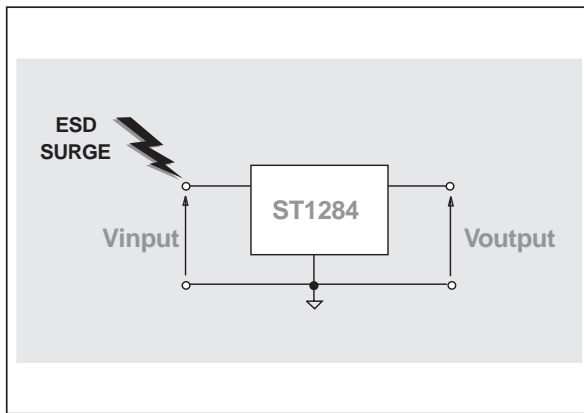
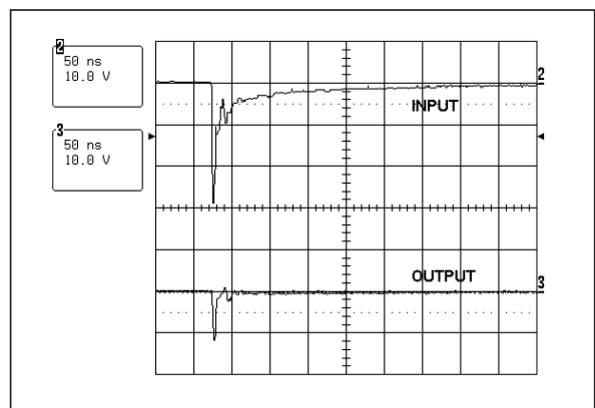
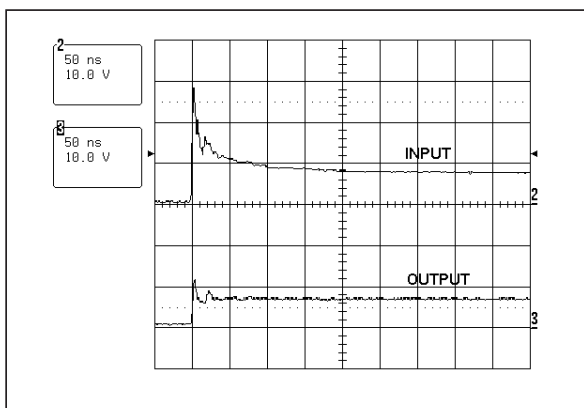


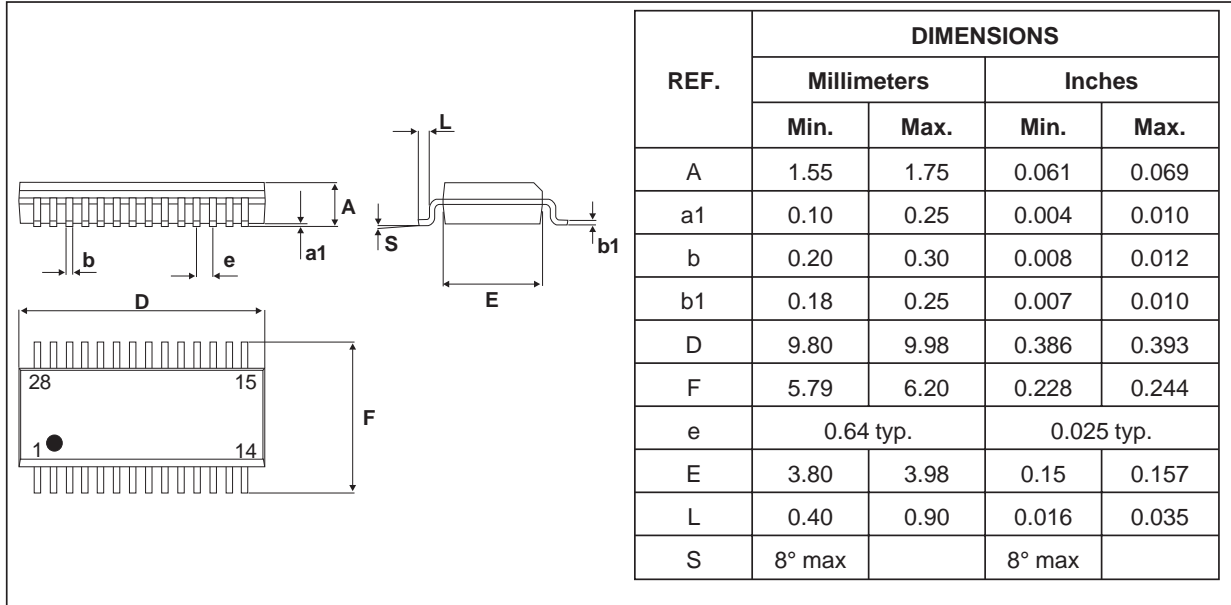
Fig. A5: Remaining voltage at the input and output of the device during a $\pm 16kV$ ESD surge (IEC61000-4-2).



ST1284-xxA8/T8

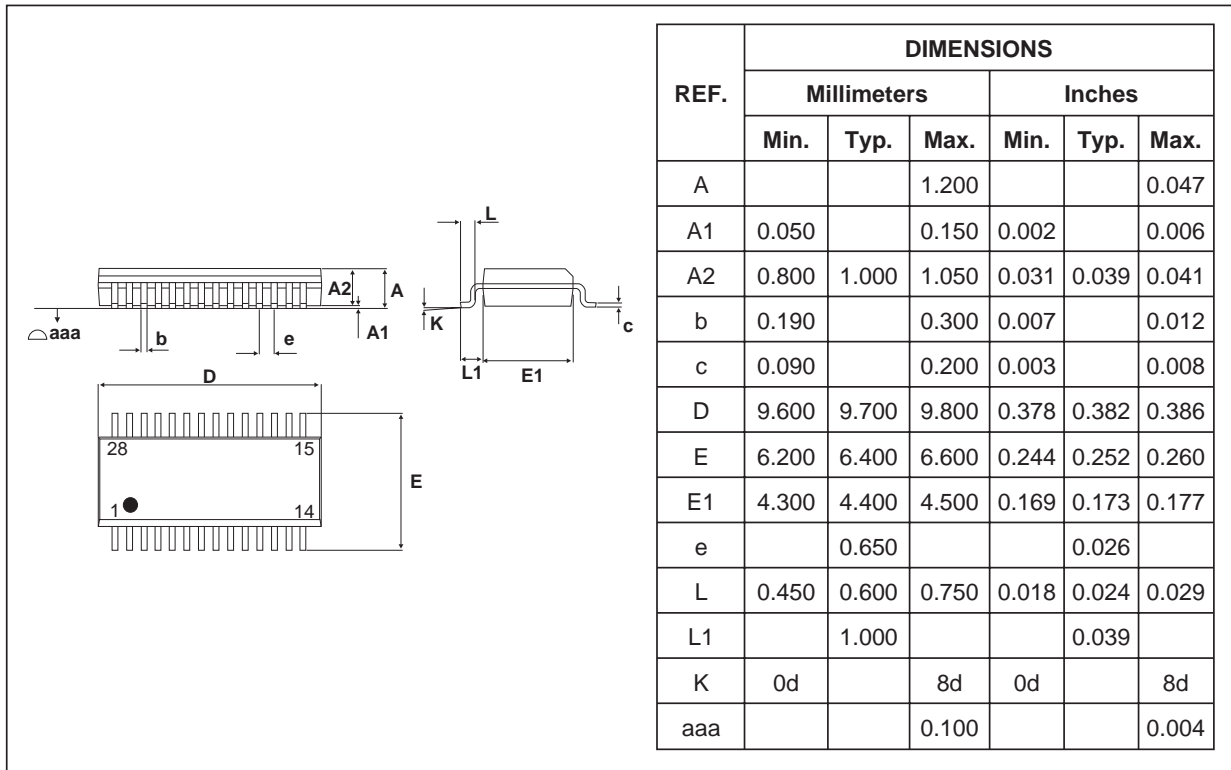
PACKAGE MECHANICAL DATA

QSOP28 (Plastic)

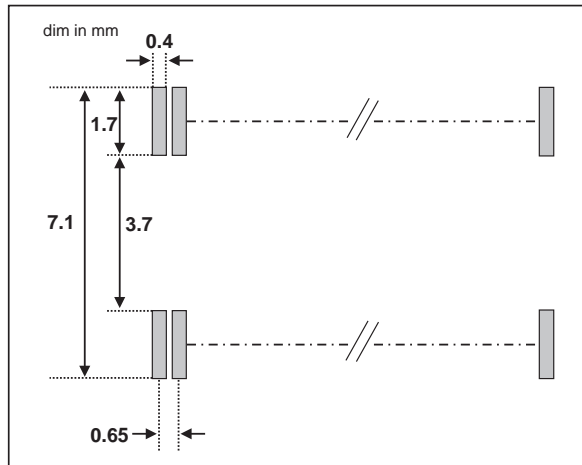


PACKAGE MECHANICAL DATA

TSSOP28 (Plastic)



FOOTPRINT (QSOP28 / TSSOP28)



Package General Specifications	
Lead Plating	Tin-Lead
Lead Plating Thickness	7 μ m Min 20 μ m Max
Lead Material	Copper Alloy
Lead Coplanarity	0.102 mm (0.004")
Body Material	Molded Epoxy
Resine	Meets UL94V.0 standard

Order code	Marking	Package	Weight	Delivery mode	Base qty
ST1284-01A8	ST1284-01	QSOP28	0.147 g	Tube	48
ST1284-01A8RL	ST1284-01	QSOP28	0.147 g	Tape & Reel	2500
ST1284-02A8	ST1284-02	QSOP28	0.147 g	Tube	48
ST1284-02A8RL	ST1284-02	QSOP28	0.147 g	Tape & Reel	2500
ST1284-03A8RL	ST1284-03	QSOP28	0.147 g	Tape & Reel	2500
ST1284-01T8RL	ST1284-01	TSSOP28	0.104 g	Tape & Reel	2500
ST1284-02T8RL	ST1284-02	TSSOP28	0.104 g	Tape & Reel	2500
ST1284-03T8RL	ST1284-03	TSSOP28	0.104 g	Tape & Reel	2500

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