STA400A

XMRADIO® SDARS CHANNEL DECODER

FRONT END INTERFACE

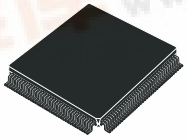
- TWO INTERNAL 10 BIT A/D CONVERTERS
- TWO QPSK DEMODULATORS FOR SATELLITE BRANCH
- ONE MULTICARRIER DEMODULATOR FOR TERRESTRIAL BRANCH
- SATELLITE SYMBOL FREQUENCY: 1.64 MBAUD
- TERRESTRIAL SYMBOL FREQUENCY: 2.99 MBAUD
- DIGITAL ROOT RAISED COSINE NYQUIST FILTER: 15% ROLL-OFF
- FFT LENGTH: 768 SUB-CARRIERS
- FULL DIGITAL CARRIER AND FREQUENCY RECOVERY AND TRACKING LOOPS
- FREQUENCY INVERSION COMPENSATION FOR HIGH-SIDE/LOW-SIDE MIXER INJECTION
- LOCK DETECTORS, C/N INDICATOR, ON CHIP BER ESTIMATORS
- TWO DIGITAL AGCs: INTERNAL SIGNAL POWER ESTIMATION AND FILTERING
- 1 BIT PDM AGCs CONTROL SIGNAL OUTPUTS

TDM DECODING AND MANAGEMENT

- SATELLITE AND TERRESTRIAL FRAME SYNCHRONIZATION
- SATELLITE PHASE AMBIGUITY RESOLUTION
- TDM DEMULTIPLEXING
- PRIME RATE CHANNEL (PRC) DEMULTIPLEXING
- EXTERNAL MEMORY CONTROLLING

FORWARD ERROR CORRECTION

- VITERBI DECODER: K=7, R=1/3
- SATELLITE DEPUNCTURING: RATE 3/4
- TERRESTRIAL DEPUNCTURING: RATE 3/5
- CONVOLUTIONAL TIME DEINTERLEAVER OVER 4.7 SEC
- BLOCK DEINTERLEAVER OVER 2 RS BLOCKS
- REED-SOLOMON DECODER: (255,223). UP TO 16 BYTES CORRECTION CAPABILITY.



TQFP144
ORDERING NUMBER: STA400A

THIS DEVICE CAN BE SOLD ONLY TO CUSTOMERS THAT HAVE SIGNED A LICENSE AGREEMENT WITH XM SATELLITE RADIO.

- ENERGY DISPERSAL DESCRAMBLER
- SAT-SAT AND TERR-SAT DIVERSITY COMBINING

BACK END INTERFACE

- TWO PAYLOAD CHANNEL BITSTREAM INTERFACES
- PAYLOAD CHANNEL SELECTION LOGIC
- DESIGNED TO WORK WITH THE STA450A SERVICE AND SOURCE DECODER

LOW POWER TECHNOLOGY

- 1.8V, 0.18µm TECHNOLOGY
- 3.3V CAPABLE I/Os

CONTROL

- IIC-BUS SLAVE CONTROL INTERFACE
- DEVICE ADDRESS: 1101010

DESCRIPTION

The SDARS is a satellite transmission system based on two geostationary satellites on the East and West coasts of the Continental United States (CONUS). In the urban areas, where the line of sight reception of the satellites is difficult or not possible, the service is covered by terrestrial repeaters adopting a MultiCarrier Modulation scheme.
Designed for digital radio receivers compatible with the XMRadio SDARS System, the STA400A Channel Decoder integrates all the functions to demodu-

late and decode the incoming satellite and terrestrial signals after the RF Front-End down-convertions: Analog-to-Digital conversions, satellite and terrestrial demodulations, AGCs, frame synchronization and demultiplexing, Viterbi decoding, time and spatial diversity combining, Reed-Solomon decoding and deinterleaving, Prime Rate Channel (PRC) demultiplexing, Payload Channel (PC) selection.
At the end of the demodulation and decoding processes a configurable serial data stream is made available to STA450A, the Service/Source Decoder, via the PC BitStream interface.

Figure 1. Channel Decoder Block Diagram

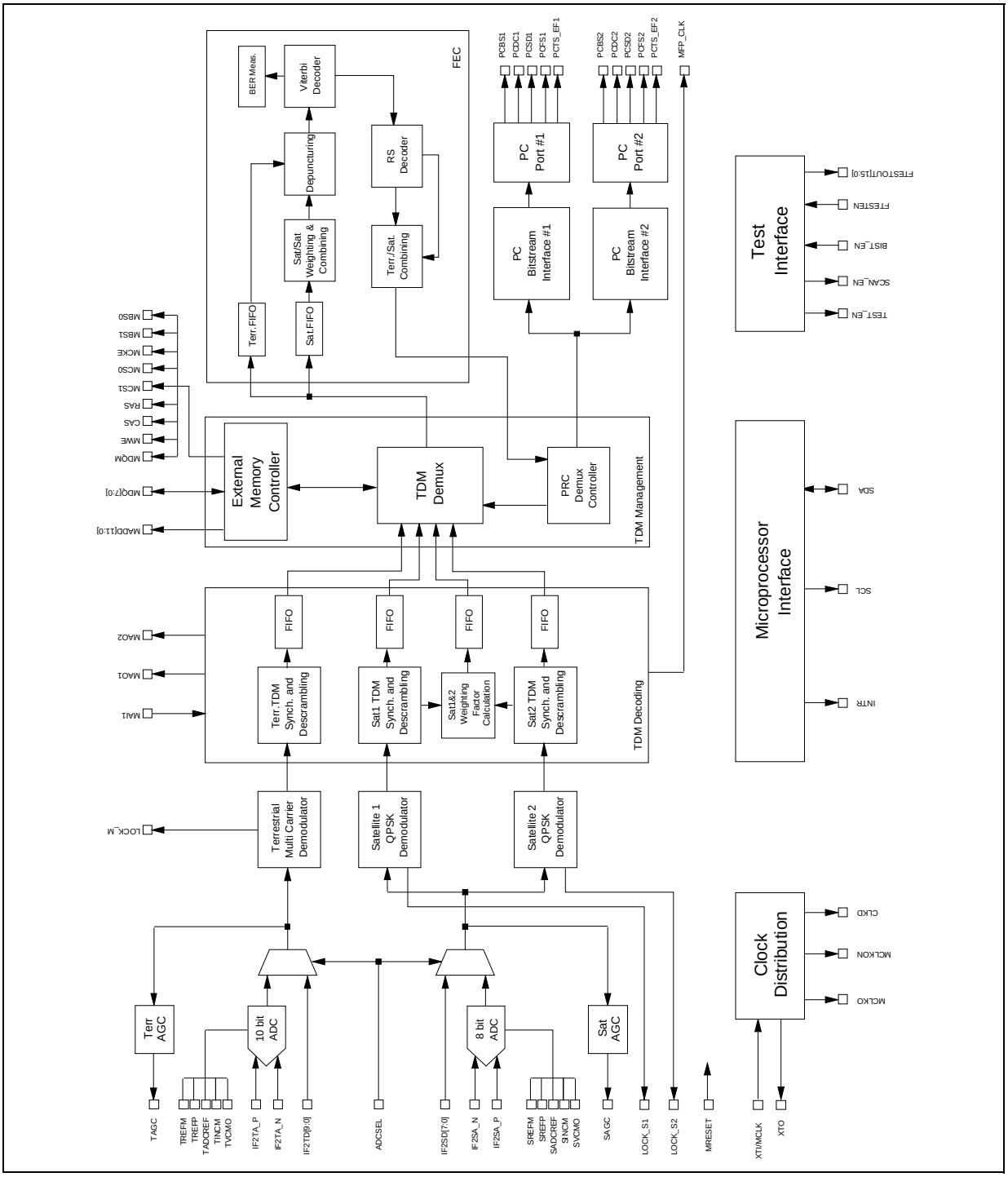
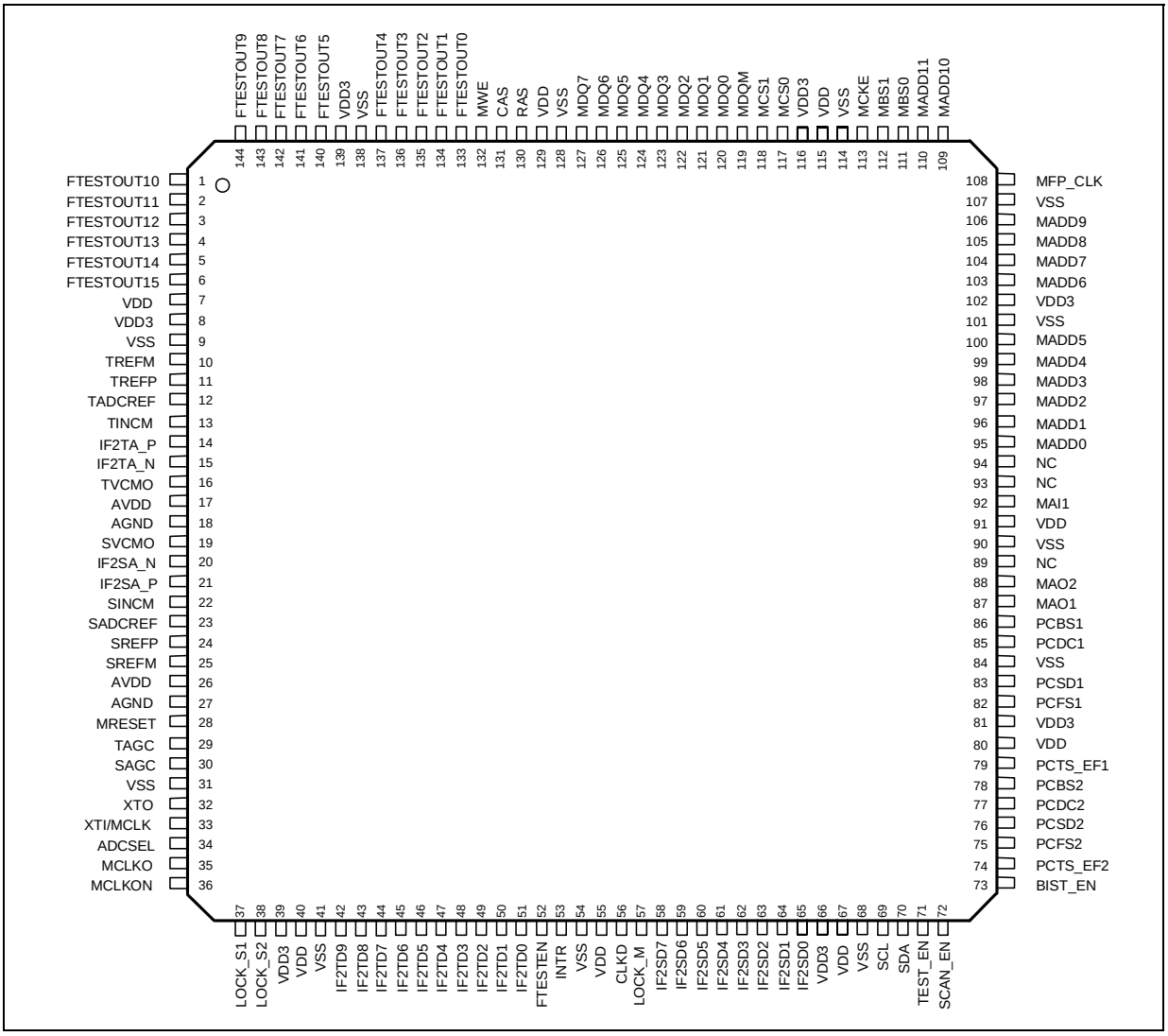


Figure 2. Pin Connection (Top view)



PIN DESCRIPTION

Pin N°	Pin Name	Type	Function	PAD Description
[1:6]	FTESTOUT[10:15]	O	Configurable Functional Test Output	2mA Output Driver
7,40,55, 67,80,91, 115,129,	VDD	PWR	1.8V Positive Supply Voltage	
8,39,66, 81,102, 116,139	VDD3	PWR	3.3V Positive Supply Voltage	
9,31,41, 54,68,84, 90,101,107 ,114,128, 138	VSS	GND	Digital Ground	

PIN DESCRIPTION (Continued)

Pin N°	Pin Name	Type	Function	PAD Description
10	TREFM	Analog Vref	Terr. ADC Reference Negative Voltage. Bottom of the reference ladder (driven or filtered).	Analog Pad Buffer (1)
11	TREFP	Analog Vref	Terr. ADC Reference Positive Voltage. Top of the reference ladder (driven or filtered).	Analog Pad Buffer (1)
12	TADCREF	Analog Terminal	Terr. ADC Reference Adjust (external resistor to determine Ipol)	Analog Pad Buffer (1)
13	TINCM	Analog Output	Terr. ADC Internal Common-Mode output for bypassing	Analog Pad Buffer (1)
14	IF2TA_P	Analog Input	Terr. 2nd IF Differential Input - Positive	Analog Pad Buffer (1)
15	IF2TA_N	Analog Input	Terr. 2nd IF Differential Input - Negative	Analog Pad Buffer (1)
16	TVCMO	Analog Terminal	Terr. ADC Internal Common Mode (filtered)	Analog Pad Buffer (1)
17,26	AVDD	PWR	Analog Positive Supply Voltage (1.8V)	
18,27	AGND	GND	Analog Ground	
19	SVCMO	Analog Terminal	Sat. ADC Internal Common Mode (filtered)	Analog Pad Buffer (1)
20	IF2SA_N	Analog Input	Sat. 2nd IF Differential Input - Negative	Analog Pad Buffer (1)
21	IF2SA_P	Analog Input	Sat. 2nd IF Differential Input - Positive	Analog Pad Buffer (1)
22	SINCM	Analog Output	Sat. ADC Internal Common-Mode output for bypassing	Analog Pad Buffer (1)
23	SADCREF	Analog Terminal	Sat. ADC Reference Adjust (external resistor to determine Ipol)	Analog Pad Buffer (1)
24	SREFP	Analog Vref	Sat. ADC Reference Positive Voltage. Top of the reference ladder (driven or filtered).	Analog Pad Buffer (1)
25	SREFM	Analog Vref	Sat. ADC Reference Negative Voltage. Bottom of the reference ladder (driven or filtered).	Analog Pad Buffer (1)
28	MRESET	I	Master Reset	Schmitt Trigger Buffer
29	TAGC	O	Terr. AGC Control Signal	2mA Output Driver
30	SAGC	O	Sat. AGC Control Signal	2mA Output Driver
32	XTO	O	XTAL Output	Oscillator Buffer
33	XTI/MCLK	I	XTAL Input or Master Clock Input	Analog Pad Buffer (2)
34	ADCSEL	I	Selection between Internal or External ADC 0=Internal	Buffer with Pull-Down

PIN DESCRIPTION (Continued)

Pin N°	Pin Name	Type	Function	PAD Description
35	MCLKO	O	Master Clock Output	4mA Output Driver
36	MCLKON	O	Inverted Master Clock Output	4mA Output Driver
37	LOCK_S1	O	Satellite Dem1 Lock Indicator	2mA Output Driver
38	LOCK_S2	O	Satellite Dem2 Lock Indicator	2mA Output Driver
[42:51]	IF2TD[9:0]	I	Terr. 2nd IF Digital Input	Input Pad Buffer. High Drive.
52	FTESTEN	I	Functional Test Enable (1=enable)	Buffer with Pull-Down
53	INTR	O	Interrupt	2mA Output Driver
56	CLKD	O	Divided Master Clock	2mA Output Driver
57	LOCK_M	O	Terrestrial Demodulator Lock Indicator	2mA Output Driver
[58:65]	IF2SD[7:0]	I	Sat. 2nd IF Digital Input	Input Pad Buffer. High Drive
69	SCL	I	IIC-bus Serial Clock	Schmitt Trigger Buffer
70	SDA	I/O	IIC-bus Serial Data	Schmitt Trigger BiDir Buffer. 4mA Driver
71	TEST_EN	I	ATPG Test Enable (1=Enabled)	Buffer with Pull-Down
72	SCAN_EN	I	Scan Enable (1=Enabled)	Buffer with Pull-Down
73	BIST_EN	I	RAM Bilt In Self Test Enable (1=Enabled)	Buffer with Pull-Down
74	PCTS_EF2	O	Payload Channel TSCC Sync2/ErrorFlag 2 (432 msec)	2mA Output Driver
75	PCFS2	O	Payload Channel PRC Frame Sync 2	2mA Output Driver
76	PCSD2	O	Payload Channel Serial Data 2	2mA Output Driver
77	PCDC2	O	Payload Channel Data Clock 2	2mA Output Driver
78	PCBS2	O	Payload Channel Byte Sync2 (RS Symbol)	2mA Output Driver
79	PCTS_EF1	O	Payload Channel TSCC Sync1/ ErrorFlag1 (432 msec)	2mA Output Driver
82	PCFS1	O	Payload Channel PRC Frame Sync1	2mA Output Driver
83	PCSD1	O	Payload Channel Serial Data 1	2mA Output Driver
85	PCDC1	O	Payload Channel Data Clock 1	2mA Output Driver
86	PCBS1	O	Payload Channel Byte Sync1 (RS Symbol)	2mA Output Driver
87	MAO1	O	Mobile Adapter Output #1	2mA Output Driver
88	MAO2	O	Mobile Adapter Output #2	2mA Output Driver
89,93,94	NC		Not Connected.	
92	MAI1	I	Mobile Adapter Input	Buffer with Pull-Down

PIN DESCRIPTION (Continued)

Pin N°	Pin Name	Type	Function	PAD Description
[95:100]	MADD[0:5]	O	External Memory Address	2mA Output Driver
[103:106]	MADD[6:9]	O	External Memory Address	2mA Output Driver
108	MFP_CLK	O	TDM Master Frame Clock	2mA Output Driver
[109:110]	MADD[10:11]	O	External Memory Address	2mA Output Driver
[111:112]	MBS[0:1]	O	External Memory Block Selection	2mA Output Driver
113	MCKE	O	External Memory Clock Enable	2mA Output Driver
[117:118]	MCS[0:1]	O	External Memory Chip Select	2mA Output Driver
119	MDQM	O	External Memory Data Mask	2mA Output Driver
[120:127]	MDQ[0:7]	I/O	External Memory Data Input Output	BiDir Buffer. 2mA Driver
130	RAS	O	External Memory Row Address Strobe	2mA Output Driver
131	CAS	O	External Memory Column Address Strobe	2mA Output Driver
132	MWE	O	External Memory Write Enable	2mA Output Driver
[133:137]	FTESTOUT[0:4]	O	Configurable Functional Test Output	2mA Output Driver
[140:144]	FTESTOUT[5:9]	O	Configurable Functional Test Output	2mA Output Driver

1. Direct connection to core
2. Connected to the internal oscillator buffer via 460 Ohm series resistor

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}, AV_{DD}	1.8V Power supply Voltage	-0.5 to 2.5	V
V_{DD3}	3.3V Power Supply Voltage	-0.5 to 4	V
V_i	Voltage on input pin	-0.5 to (Vdd3 + 0.5)	V
V_o	Voltage on output pin	-0.5 to (Vdd3 + 0.5)	V
V_{ia}	Voltage on analog input pin	-0.8 to (AVdd + 0.8)	V
V_{oa}	Voltage on analog output pin	-0.8 to (AVdd + 0.8)	V
T_{stg}	Storage Temperature	-55 to +150	°C
T_{oper}	Operative Ambient Temperature	-40 to +85	°C
T_j	Operative Junction Temperature	-40 to +125	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{j\text{-}amb}$	Thermal Resistence junction to ambient(1)	40	ºC/W

Notes: 1. according to JEDEC specification on a 4 layers board

DC ELECTRICAL CHARACTERISTCS: (T_{amb} = -40 to +85°C, V_{DD} = AV_{DD} = 1.65 to 1.95V, V_{DD3} = 3.0 to 3.6V unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	1.8V Supply Voltage		1.65	1.8	1.95	V
V_{DD3}	3.3V Supply Voltage		3.0	3.3	3.6	V
AV_{DD}	1.8V Analog Supply Voltage		1.65	1.8	1.95	V
I_{DD}	V_{DD} Power Supply Current	MCLK = 23.92MHz; sat1, sat2 & terr arms active; V_{DD}=1.95V		130	160	mA
I_{DD3}	V_{DD3} Power Supply Current	MCLK = 23.92MHz; sat1, sat2 & terr arms active; V_{DD3}=3.6V		45	90	mA
$I_{AVDDsat}$	AV_{Ddsat} Power Supply Current	MCLK = 23.92MHz; V_{IN}=0.75Vpp; f_{IN}=6.095MHz; AV_{Ddsat}=1.95V		16	20	mA
$I_{AVDDterr}$	AV_{Ddterr} Power Supply Current	MCLK = 23.92MHz; V_{IN}=0.75Vpp; f_{IN}=2.99MHz; AV_{Ddterr} =1.95V		16	20	mA
P_d	Power Dissipation	MCLK = 23.92MHz; V_{DD} = 1.8V; V_{DD3} = 3.3V		350		mW
I_{il}	Low level input leakage current 1)	Vi = 0V			1	µA
I_{ih}	High level input leakage current 1)	Vi = V_{DD3}			1	µA
I_{OZ}	Tristare output leakage current 2)	Vo = 0V or V_{DD3}			1	µA
I_{pd}	Pull-down current	Vi = V_{DD3}	30		110	µA
R_{pu}	Equivalent pull-up resistance 7)	Vi = 0V		50		KΩ
R_{pd}	Equivalent pull-down resistance 7)	Vi = V_{DD3}		50		kΩ
V_{il}	Low level input voltage				0.8	V
V_{ih}	High level input voltage		2			V
V_{ilhyst}	Low level threshold input falling		0.8		1.35	V
V_{ihhyst}	High level threshold input rising		1.3		2	V
V_{hyst}	Schmitt trigger hysteresis3)		0.3		0.8	V
V_{ol}	Low level output voltage 4,5)	Iol = XmA			0.2	V
V_{oh}	High level output voltage 4,5)	Ioh = XmA	2.8			V
C_{in}	Input capacitance 3)				1.2	pF
C_{out}	Output Capacitance 3)				1.9	pF
C_{io}	I/O (bi-directional) capacitance 3)				2.1	pF
$I_{latchup}$	I/O Latch-up current		200			mA
V_{ESD}	Electrostatic Protection 6)	Leakage<1µA	4000			V

Note 1: Performed on all the input pins excluded the pull-down ones
Note 2: Performed on the I/O pins in tristate mode
Note 3: Guaranteed by Design
Note 4: take into account 200mV voltage drop in supply lines and Input/Output levels for frequency > 20MHz.
Note 5. X is the source/sink current under worst case conditions (X = 2 to 4 mA)
Note 6: Human body Model
Note 7. Guaranteed by Ipd measurements

ADC ELECTRICAL CHARACTERISTCS: (T_{amb} = -40 to +85°C, V_{DD} =1.8V, AV_{DD} = 1.65 to 1.95V, V_{DD3} = 3.3V unless otherwise specified

ADC Analog Input

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IF2xA_P, IF2xA_N	Voltage Range			0.75		Vpp
XINCM	Internal Common Mode		0.375		0.625	V
R_{in} (1)	Input Resistance 2)	@75MHz		35		kΩ
C_{in}	Input Capacitance 2)			800		fF
BW	Analog Bandwidth 2)			200		MHz

ADC Reference Voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
XREFP	Top internal voltage reference			0.75 ±50mV		V
XREFM	Bottom internal voltage reference			0		V

ADC Accuracy

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DNL	Differential Non-Linearity	Tamb = 25°C ; AV_{DD} = 1.8V	-1.5	±0.9	1.5	LSB
INL	Integral Non-Linearity	Tamb = 25°C; AV_{DD} = 1.8V	-2.0	±1.5	2.0	LSB

ADC Dynamic Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SNR	Signal to Noise Ratio 2)	Fs = 75Msps, Fin = 15MHz; AV_{DD} = 1.8V		57		dB
SINAD	Signal to Noise and Distortion Ratio 2)	Fs = 75Msps, Fin = 15MHz AV_{DD} = 1.8V		56		dB
THD	Total Harmonic Distortion 2)	Fs = 75Msps, Fin = 15MHz AV_{DD} = 1.8V		57		dB
ENOB	Effective number of bit 2)	Fs = 10Msps, Fin = 10MHz AV_{DD} = 1.8V		9.5		bit

Note1: Input resistance from conversion frequency f_C: $R_{IN} = (35K\Omega \times 75MHz)/f_C$
Note2: Guaranteed by Design

MASTER CLOCK INPUT ELECTRICAL CHARACTERISTCS: (T_{amb} = -40 to +85°C, V_{DD} =1.65 to 1.95V, AV_{DD} = 1.65 to 1.95V, V_{DD3} = 3.0 to 3.6V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{MCLK}	Master clock input voltage swing		0.8	1	1.2	Vpp
$V_{MCLKOFS}$	Master clock input Voltage offset			Vdd/2		V

OSCILLATOR BUFFER ELECTRICAL CHARACTERISTICS

The Oscillator Pad Buffer is a single stage oscillator with an inverter working as an amplifier biased by an internal resistor (>1 MOhm). With an external PI network consisting of a crystal and two capacitors it works as oscillator, without the external crystal component it acts as input trigger.
Pin XTI (analog pad buffer) is the input for the external clock source or for the quartz component, XTO is the oscillator buffer output pin to be connected to the external quartz.

Oscillator Mode Specification (Guaranteed by Design)

Condition: 27 MHz oscillation - PI quartz network connected to XTI and XTO ($C_A = C_B = 16pF$).

Symbol	Parameter	Min	Typ	Max	Unit
Ci	Current Consumption			450	µA
Cp	Power Consumption			810	µW
DC	Duty Cycle	49.07	49.60	49.86	%
$t_{start-up}$	Start-up Time		3		ms

Symbol	Parameters	VL	VH	Hysteresis	Unit
Hys	Hysteresis	0.631	1.123	0.492	V

Input Trigger Mode Specification (no crystal connected) (Guaranteed by Design)

Condition: 27 MHz sine wave (0.5V amplitude, VDD/2 offset) applied to XTI.

Symbol	Parameters	Min	Typ	Max	Unit
Ci	Current Consumption		133		µA
Cp	Power Consumption		240		µW
DC	Duty Cycle		49.45		%

The external analog signal to be applied to the XTI input must be a sinusoid or a impulse wave centered at Vdd/ with 1V peak-to-peak amplitude.

Minimum Oscillator Transconductance (Guaranteed by Design)

Symbol	Patrameters	Min	Typ	Max	Unit
	gmcrit		1236		µA/V

The oscillator pad buffer can work with different crystal frequencies. To check if a given quartz can be used with this oscillator, the needed amplifier transconductance must be evaluated by the following formula:

$$gm_{crit} = R_m \cdot \omega^2 \cdot \frac{(C_A \cdot C_B + C_A \cdot C_O + C_B \cdot C_O)^2}{C_A \cdot C_B}$$

if

$$C_A = C_B = C$$

the equation simplifies to:

$$gm_{crit} = R_m \cdot \omega^2 \cdot (C + 2C_O)^2$$

where R_m is the quartz equivalent series resistance, C_A and C_B the PI network capacitances and C_O the quartz shunt capacitance.

The transconductance of the oscillator pad given in the table above must be 8/9 times the transconductance calculated with the formula.

1 FUNCTIONAL DESCRIPTION

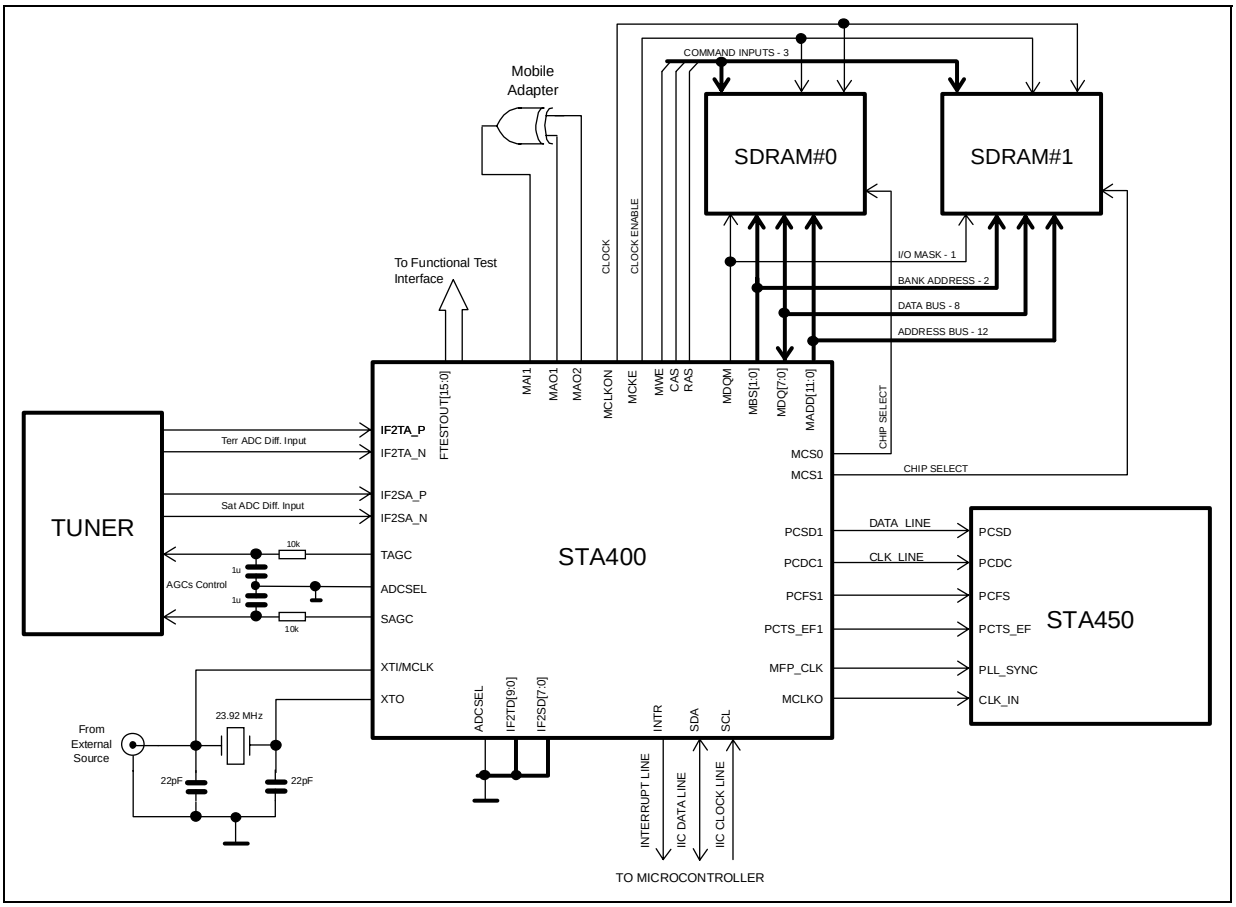
The main inputs of the STA400A Channel Decoder are the 2nd IF analog signals centered at 6.095 MHz for the satellite and at 2.99 MHz for the terrestrial branch. The final down-convertion to baseband of the three signals is digitally performed inside the chip. After the demodulation process, the three TDM data streams are available and stored into the external memory for further digital processing including TDM decoding and demultiplexing, time and spatial diversity combining, FEC processing and data stream generation for the external source decoding.

The external memory and the PRC-based packed structure of the service layer allow the use of one Viterbi decoder and RS decoder for the FEC processing of both the combined satellite and terrestrial frames.

The STA400A is designed to work with the STA450A Service/Source Decoder, an external RF Tuner and a 128Mbit Synchronous DRAM. Figure 3 depicts the connection block diagram of the STA400A Channel Decoder and the external components. The 128Mbit SDRAM may be selected as a single 4Mx8Bitx4Banks or as a dual 2Mx8Bitx4Banks Memory. In the latter case the MCS0 pin must be connected to the chip select input of the memory and the XMEM_TYPE register (address 0x0630) must be programmed with "0x01" (see section 2.8).

STA400A is fully configurable via the I2C-bus interface.

Figure 3. STA400A Connection Diagram



The 23.92 MHz system clock applied to XTI/MCLK input (pin 33) can be generated by the built-in clock buffer and an XTAL pi-network as showed in fig.3 or may come from an external source. In both cases the quartz or the external source must be compliant with the specifications given in the I/O Cell Description (section 3).

In fig.3 the two embedded 10 bits ADCs are used to sample and convert to digital the satellite and terrestrial IF signals from the tuner. An internal mux, controlled by the ADCSEL input (pin 34), may be used to by-pass the

two embedded ADCs. This functionality gives the possibility to use two external ADCs connected to the satellite digital input (IF2SD[7:0]) and to the terrestrial digital input (IF2TD[9:0]) respectively. The digital inputs must be tied to ground when not used.

The FTESTOUT[15:0] pins are available for testing purpose and for measuring system performance.

1.1 IF SAMPLING AND CONTROL INTERFACE

This block comprises the embedded ADCs, the satellite and terrestrial AGCs and CDEC CONTROL registers. It receives from the RF Front-End the two QPSK modulated satellite signals centered at 6.095 MHz and the MultiCarrier Modulated terrestrial signal centered at 2.99 MHz (2nd IF frequencies). These signals are over sampled by the 23.92 MHz master clock (MCLK) and converted to digital on 8 bits for the satellite composite signal and on 10 bits for the terrestrial signal (see fig.1).

The programmable registers of the IF Sampling block are described in section 2.6.

Embedded ADCs

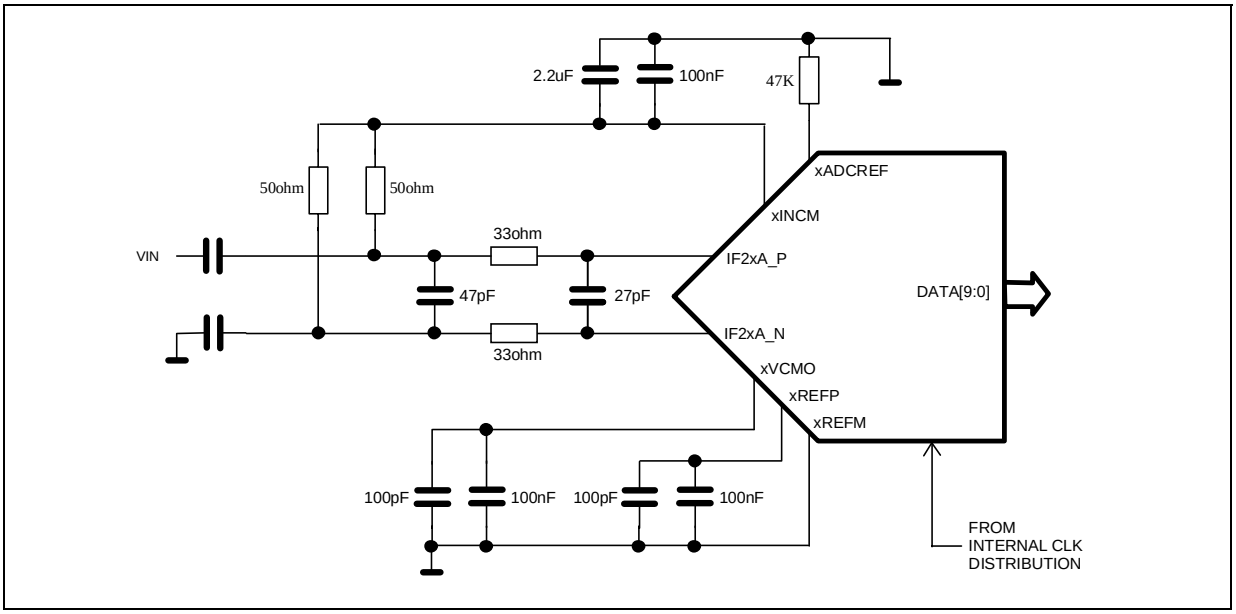
The two embedded ADCs are 10 bit high speed A/D converters designed for high sampling rate (up to 50 MHz) and low power consumption (1mW/MHz) with a full differential pipeline conversion architecture that needs 6 clock periods for one conversion.

A voltage reference is integrated in the circuit for external components minimization but it is possible to use an external reference.

The ADCs provide also a reduced input capacitance, a low reference capability and a wide input bandwidth (50MHz).

Pins IF2xA_P IF2xA_N can be connected as full-differential inputs or as pseudo-differential input. In fig.4 the latter configuration is showed (x=S for Satellite and x=T for Terrestrial branch).

Figure 4. ADC Pseudo-Differental Configuration



The two pins xREFM (Bottom of the reference ladder) and xREFP (Top of the reference ladder) are decoupling nodes for conversion dynamic adjustment; when the internal reference is used these pins must be connected as showed in figure 4. Pin xADCREF is connected with an external resistor (typical value 47 Kohm) to trim the internal bias current, xINCM is the output common mode used to centre the external input network and xVCMO is the internal common mode that can be externally filtered by a capacitor.

IF AGC

To maintain constant the signal levels at the A/D converters input, two 1-bit Pulse Density Modulated (PDM) signals (SAGC for satellite and TAGC for terrestrial branch) are generated to drive an external IF AGC.

The difference between the user programmable reference level and the power of the input samples is integrated by the programmable gain loop filter and then sent to a 1-bit modulator to generate the output control signal. The sense of this signal is programmable to adapt it to a positive or negative slope of the variable gain amplifier.

The SAGC and TAGC outputs can be filtered by an external low pass filter to close the AGC loop (see fig.3); in this way the mean power of the ADCs input signal is forced to the reference.

The AGC loop gain is given by: $\beta_{AGC} = 2^{xAGCBETA}$. The parameter xAGCBETA can take values from 0 to 6. When xAGCBETA="111" the loop gain is zero. The AGC loop may be opened by programming "111" in the x AGCBETA parameter and writing "00000000" in the xAGCINTG register. In this condition the control signal is a 50% duty-cycle square wave with a frequency of MCLK/2 (23.92MHz/2=11.96MHz).

The 8 MSBs of the integrator register may be read at any time in the xAGCINTG register. This value is the level of the AGC outputs after low pass filtering; it gives an image of the input signal power at the terrestrial and satellite branch respectively.

The reference level can be set by the xAGCREF register, the loop gain and the sense of the control pins (TAGC and SAGC) are set by the AGC_CTRL1 register described in section 2.6.

CONTROL Registers

The IF_CTRL, CONTROL and STATUS1 are the control registers of the IF Sampling interface (see section 2.6).

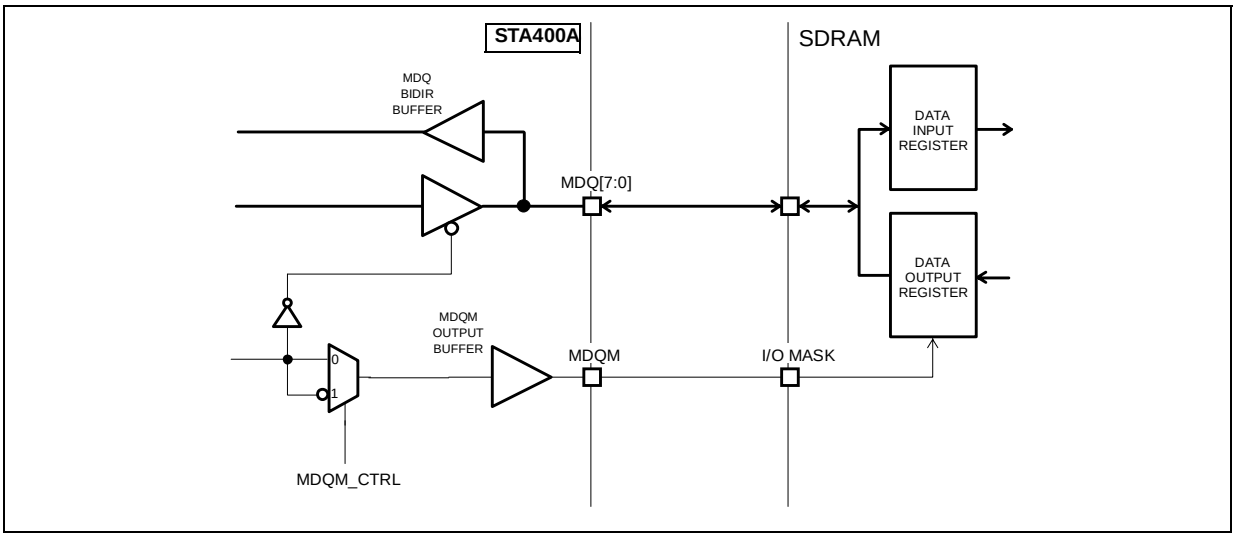
To have a more stable reading of the xAGCINTG register a moving average filter over 2048 samples is used. This filter can be enabled or disabled by the bit7 of the IF_CTRL register.

The data bit from the external ADCs (if used) may have a two's complement or offset binary format. Bit1 of the IF_CTRL register sets the binary format for the digital IF inputs.

The CONTROL register configures the master clock outputs (MCLKO and MCLKON) and the external memory mode access of the bi-directional bus (MDQ[7:0]). When the master clock output buffers are disabled the output levels are fixed to ground resulting in no activity on these pins; this aproach minimizes the interferences when these signals are not used.

The bi-directional buffers of the STA400A and the input/output mask of the external SDRAM are controlled by the MDQM pin. The STA400A has a low level active bi-directional buffers (high level on the enable drives the buffers to Hi-Z). The input/output mask operation of the external SDRAM may be selected active HIGH or active LOW (see figure 5) setting the MDQM_CTRL parameter of the CONTROL register (bit5).

Figure 5. Input/Output Mask Configuration

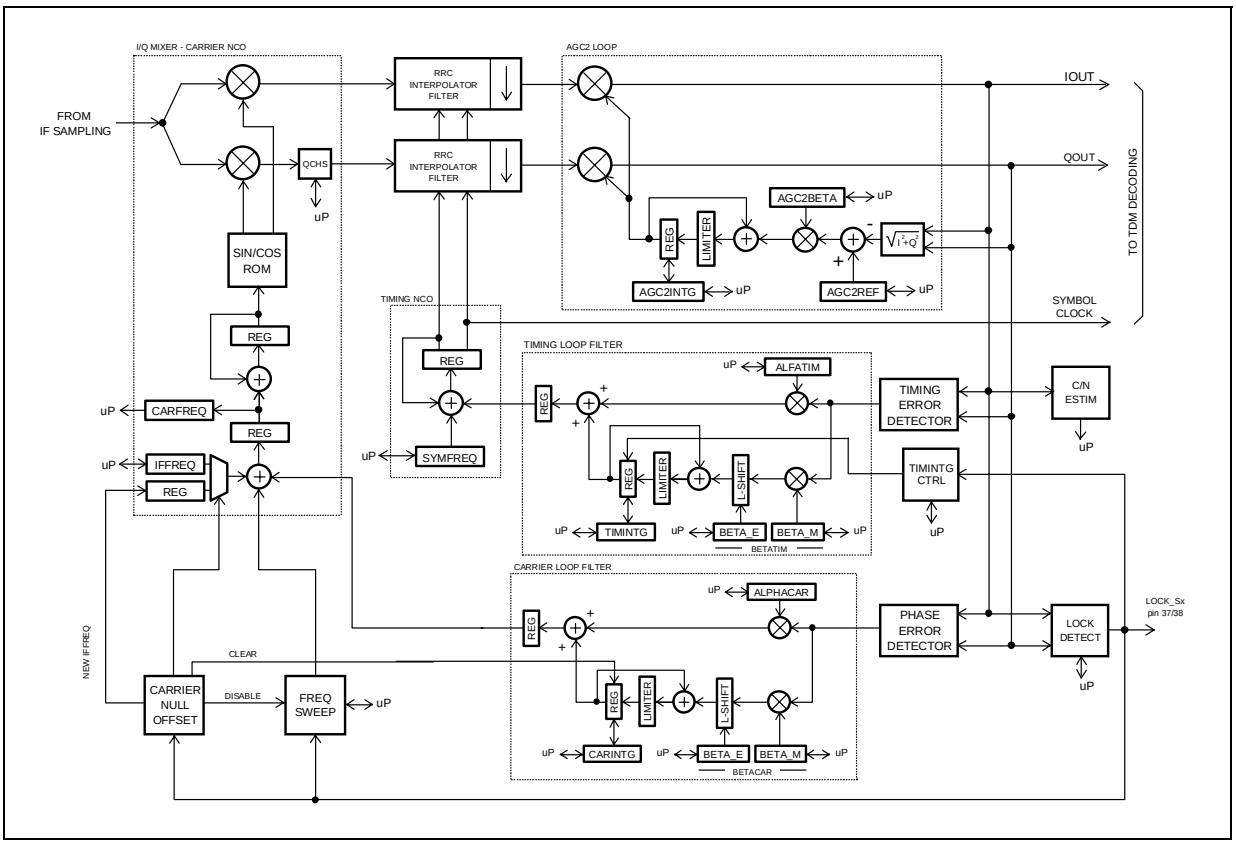


The carrier lock indication of the satellite and the terrestrial demodulators, and the status of the FEC Terrestrial-Satellite combining may be read in the STATUS1 register described in section 2.6.

1.2 SATELLITE DEMODULATION

The satellite signals are demodulated by two QPSK demodulators, one tuned to the East satellite and the other to the West satellite. The two QPSK demodulators are identical and include quadrature demodulation, carrier and timing recovery and tracking, frequency sweep generation, Nyquist Root Raised Cosine filtering with 15% roll-off, digital AGC, lock indication and carrier to noise estimation.

Figure 6. Satellite Demodulator Block Diagram



The architecture of one QPSK demodulator is depicted in fig.6. The input signal, sampled at 23.92 MHz and quantized on 8 bits, is multiplied by the sine an cosine functions to obtain the In-phase and the Quadrature component of the transmitted symbols. The demodulated QPSK signal is affected by the phase and frequency error due to oscillator inaccuracies and frequency shift. These errors are removed by the carrier tracking loop by means of a Phase/Frequency Detector, a loop filter and an NCO. The symbol tracking loop removes the phase and frequency uncertainties in the symbols: instead of controlling the sampling clock phase, the timing error detector adjusts, using the timing NCO, the impulse response phase of the two interpolator filters.

To enhance the performace of the demodulator in presence of a signal dropout, the carrier and symbol loops are controlled by the CarrierNullOffset and the TimingCtrl blocks. The first operates on the Carrier NCO and Carrier Loop Filter, the latter on the Timing Loop Filter.

An internal ramp generator (FreqSweep) is used to help the carrier loop during the acquisition phase. The frequency sweep is stopped by the lock detector output whenever a lock condition is reached.

The phase ambiguity introduced by the demodulation process and the frame synchronization are resolved in the TDM Decoding block using the Master Frame Preamble (MFP) and the Fast Syncronization Preamble (FSP).

The second IF composite satellite signal, available at the IF2SA inputs, has the spectrum schematically shown in Fig.7. The base band convertion of the selected satellite signal is done by programming the carrier NCO (acting as local oscillator) of the demodulator. For demodulating the S1-Early Satellite signal the carrier NCO frequency of the Early QPSK Demodulator must be equal to 6.095 + 0.92 = 7.015 MHz; for the S2-Late Satellite signal the frequency at the carrier NCO output of the Late QPSK Demodulator must be 6.095 - 0.92 = 5.175 MHz.

The register map of the QPSK demodulators is described in section 2.2.

I/Q Mixer - Carrier NCO

The final downconvertion to baseband of the 2nd IF satellite signal is performed by a mixer and a local oscillator implemented with an NCO and a Sin/Cos Look-up table (see figure 6). The signal coming from the IF Sampling block is multiplied by the output of the quadrature NCO to produce the I and Q components of the baseband signal. The NCO output are the sine and cosine functions obtained with a look-up table driven by a 28 bit phase accumulator.

The IFFREQ register sets the frequency of the carrier NCO as given in the following:

$F_c = F_{MCLK} \times (IFFREQ)/2^{28}$,

where F_{MCLK} is the clock frequency and IFFREQ is the 28 bit integer value loaded in the register.

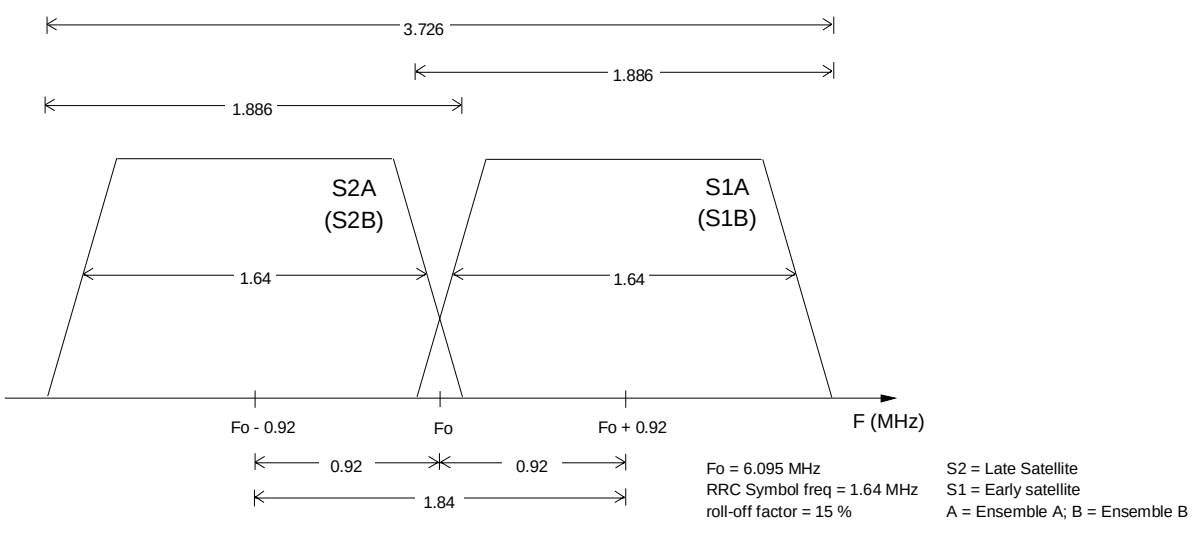
For example, to program the S1-NCO to 7.015 MHz the IFFREQ register must be loaded with 04B13B14 (Hex) equivalent to 78723860 (Dec).

The sine/cosine output frequency of the NCO is given by $F_o = (F_c + F_{sw} + PH_{err}) \times F_{MCLK}/2^{28}$ where Fc is the nominal center frequency, F_{sw} is the output of the frequency sweep generator, PHerr is the filtered phase error from the carrier loop filter output and $F_{MCLK}/2^{28}$ is the NCO frequency resolution.

The CARFREQ read only register gives the value of the actual carrier frequency after the lock condition has been reached. This register can be used to measure the frequency offset between the local oscillator and the incoming carrier.

The QCHS block of the I/Q mixer changes the sign of the Quadrature component in order to adapt the demodulation process to a different rotation sense of the QPSK mapping.

Figure 7. Second IF Satellite Signal Spectrum



High-Side/Low-Side Injenction Control

In a superetherodyne tuner (using two downconversions to produce the second IF signal at the Channel Decoder satellite input) is possible that one LO may use an High-Side injection of the carrier and the other LO may use a Low-Side injection.

In this case a data polarity convertion is required in the Channed Decoder. To accomodate this function two methods are available: the first method requires a polarity change in the QCHS and CARCHS bits of the QPSK_CTRL register, with the second method the IFFREQ register of the carrier NCO must be programmed with the image frequency using the following formula:

$$F_{MCLK} - F_c = F_{MCLK} \times (IFFREQ)/2^{28}$$

For example, to set the image frequency of the 7.015 MHz the value FB4EC4EC (Hex) must be loaded in the IFFREQ register.

Matched/Interpolator Filters

The STA400A provides two matched/interpolator filters. These filters perform the Nyquist filter function (matched with the one in the transmission side) with a Root Raised Cosine (RRC) shape and a roll-off factor of 15% and the interpolation function to evaluate the optimum sampling instant of the output symbol. The filters, based on a poliphase structure (12 taps with 32 coefficients/ tap), receive at their inputs the separate I and Q streams at F_{MCLK}/F_{SYM} samples/symbols and produce the separate I and Q output streams at one sample per symbol. The frequency responce of one filter is given in fig.8 and fig.9.

AGC2

The AGC2 loop is designed to maintain a fixed signal level at the input of the Soft Decision Slicer. As shown in fig.6, the AGC2 loop consists of an error detector, a loop filter and a gain multiplier. The modulus of the complex symbols is compared to a programmable reference level (AGC2REF register) and then scaled by the AGC2BETA coefficient and integrated. The filtered error drives two multipliers at the output of the Matched filters to maintain constant the level at the demodulator output.

The AGC2 loop gain is given by: $\beta_{AGC2} = 2^{AGC2BETA}$. The parameter AGC2BETA can take values from 0 to 6. When AGC2BETA="111" the loop gain is null and the AGC2 amplifier gain keeps the last value. The AGC loop may be opened by programming "111" in the AGC2BETA parameter and writing "0x00" in the AGC2INTG register.
The reference level set in the AGC2REF register impacts on the carrier and timing loop equations and on the operation of the Soft Decision Slicer.

Figure 8. RRC Filter Frequency Responce

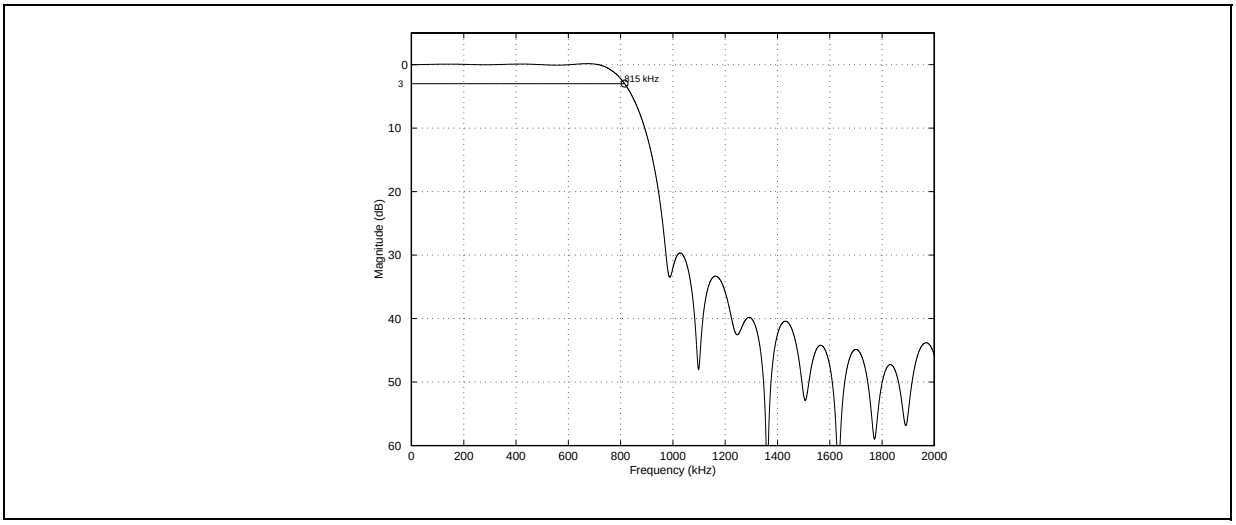
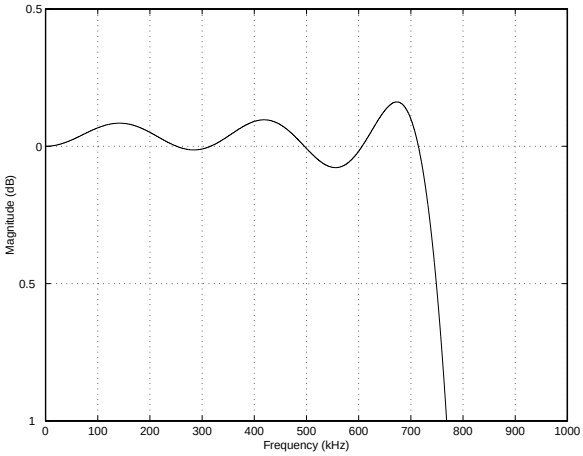


Figure 9. RRC Filter Passband Ripple



Carrier Phase/Frequency Error Detector

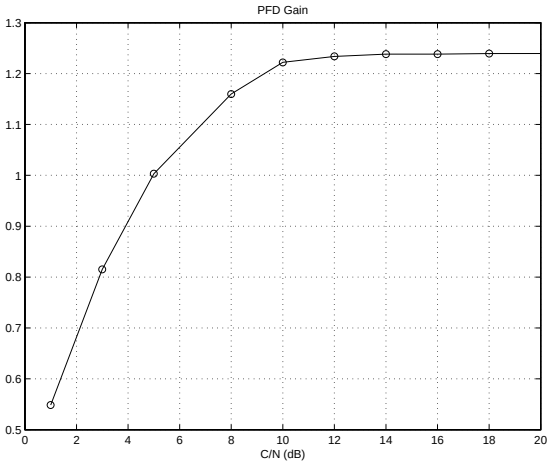
The carrier Phase/Frequency Error Detector (PFD) measures the error between the sampled symbols and the quadrant bisector. The error is calculated by the following formula : PH_{err} = I x Sgn(Q) - Q x Sgn(I), where Sgn(.) is the sign function.

This value is computed at symbol rate if the actual I and Q components are greater than a programmed threshold otherwise the previous value is maintained. In this way the detector outputs a DC value proportional to the frequency offset between the incoming signal and the local oscillator. In the steady state, when the carrier loop is locked (and, therefore, the phase error is small), the circuit behaves like a pure phase detector while during the acquisition phase it behaves like a PFD.

The threshold value may be programmed by the PFDTHR register. The signal level after the AGC2 loop must be taken into account when setting the threshold. The default preset for this parameter is about the 20% of the AGC2 reference value (see AGC2REF register).

The carrier Phase and Frequency Detector Gain (K_d) characteristic as a function of the Carrier to Noise ratio is given in fig.10. K_d = 1.24 is the value for a noise free input signal and may be reduce up to 50% of its maximum value in a low C/N condition.

Figure 10. Carrier Phase/Frequency Detector Gain



Carrier Loop Filter

The carrier loop filter is a first order IIR filter with two programmable parameters, one for the proportional and the other for the integral correction, as shown in fig. 6. The output of the integrator, that produces a frequency control term, is summed with the weighted phase error in the proportional path and then sent to the Carrier NCO to close the carrier tracking loop.

The proportional gain alpha and the integral gain beta of the filter are configured by the registers ALFACAR and BETACAR respectively. The integral gain is set by a mantissa and exponent as given by:

$beta = beta\_m \times 2^{(beta\_e)}$

where beta_m, the mantissa, is a 5-bit integer value set in the five LSBs of the BETACAR register (beta_m=BETACAR[4:0]) and beta_e, the exponent, is a 3-bit integer set in the three MSBs of the BETACAR register (beta_e=BETACAR[7:5]).

The proportional gain is an integer value set in the ALFACAR register with a range from 0 to 255 (alpha=ALFACAR[7:0]). The CARINTG register collects the 8 MSBs of the filter integrator and may be read or written at any time by the system controller. When the register is written, the integrator LSBs are reset. The filter integrator is saturated to 21-bit by the LIMITER block resulting in a maximum peak-to-peak frequency range of 373KHz (with F_{MCLK} = 23.92MHz).

Carrier Loop Equations

The carrier loop is fully digital and comprises two blocks working at symbol rate: the Phase/Frequency Error Detector and the Loop Filter, and two blocks working at clock rate: the Carrier NCO and the I/Q Mixer (see fig.6).

The loop is parametrised by the coefficients alpha and beta given in the registers ALFACAR and BETACAR respectively. The carrier loop is a second order loop whose natural frequency f_n and damping factor ξ may be calculated applying the following formulas:

$$f_n = 26.96\sqrt{mK_d beta} \quad [Hz] \qquad \zeta = 0.01322\ alpha\ \sqrt{\frac{mk_d}{beta}}$$

where alpha is set in the ALFACAR register and beta in the BETACAR register, K_d is the PFD gain as shown in fig.10 and m is the reference level of the AGC2 loop (see AGC2REF register).

For example, to set the loop natural frequency to 1.3KHz with the default value for m=AGC2REF (90dec, 5Ahex) and K_d = 1.24 (noise free value), the above equation solved for beta gives:

$$beta = \frac{f_n^2}{726.84mK_d} = 20.83$$

alpha can be chosen to have a damping factor equal to 0.7:

$$alpha = \frac{\zeta}{0.01322}\sqrt{\frac{beta}{mK_d}} = 22.87$$

The register ALFACAR can be programmed with 23 (Dec) and the register BETACAR can be programmed with the parameter BETA_E=0 and BETA_M=21 (Dec).

Frequency Sweep

When the frequency offset is greater than the pull-in range of the carrier loop or in presence of low signal to noise ratio the tracking performance of the loop itself may became rather slow. To help the loop in tracking this frequency offset an internal frequency sweep generator can be enabled via IIC-bus. The output of this block is summed to the frequency register of the I/Q Mixer and operates only during the carrier acquisition. The sweep is stopped by the lock detector when the carrier lock condition is reached (see fig.6).

The sweep rate is given by the following formula:

$$\frac{dF}{dt} = \frac{2^{SWSTEP}}{STEPPER + 1}\frac{F_{MCLK}^2}{2^{28}} \quad [Hz/s]$$

The frequency sweep operation is controlled by the RAMPCTRL register. The parameter SWSTEP can take 0 or 1 values and STEPPER can be programmed in the range 0 to 15 decimal.

The maximum peak-to-peak frequency sweep range is 373.75KHz. The sweep direction can be positive or negative depending on the bit-6 of the RAMPCTRL register. The sweep always starts from the zero value; when the upper limit is reached, the sweep continues with the lower one if the positive slope is set and viceversa when the negative slope is selected.

This frequency sweep block can be switched on or off setting the SWON parameter to 1 or 0 respectively. When SWON=0 the output value of the ramp is null.

Carrier Lock Detector

The lock detector consists of an up/down counter with saturation driven by a dedicated logic. This circuit monitors the QPSK symbol constellation to decid the counter direction. If the actual symbol is inside the region delimited by the equations $2 \times I - Q \geq 0$ and $2 \times Q - I \geq 0$ (the lock region) the counter counts up otherwise counts down. If the demodulator is locked, the number of symbols inside the lock region is greater than the number of symbols outside and the the counter is driven in the up direction toward the saturation limit. When the counter output is above a programmable threshold, the lock indicator is set to '0' declaring the lock condition of the carrier tracking loop. This threshold is set by the LOCKTHR register.

The lock detector controls the frequency sweep generator, the Carrier Null Offset and TIMING_CTRL circuits.

Timing NCO

The timing NCO is the timing generator for the two interpolator filters (see fig.6). To correct the symbol error, the impulse response of the interpolator is shifted by an amount of time depending on the phase accumulated in the timing NCO. It consists of a 25-bit modulo-1 accumulator driven by the output of the timing loop filter. The 5LSBs of the accumulator give the fractional part of the sampling clock used by the interpolator filter to select the coefficients of the impulse response that cancel the timing error. The integer part, given by the carry bit of the accumulator, is used to decimate to symbol rate the output of the interpolator/matched filter.

The nominal symbol frequency is set by the SYMFREQ register. The timing loop adjusts this nominal value to find the optimal symbol phase (maximum open eye condition) and to track the residual symbol frequency offset. The output of the timing generator is given by

$$F_o = (F_{sym} + TED_{err}) \times F_{MCLK}/2^{25}$$

where F_{sym} = 1.64MHz is the nominal symbol frequency, TED_{err} is the filtered timing error detector output and $F_{MCLK}/2^{25}$ is the NCO resolution.

For example, to set the symbol frequency to 1.64MHz the SYMFREQ register must be loaded with the value 00231A8B (Hex) equivalent to 2300555 (Dec).

Timing Error Detector

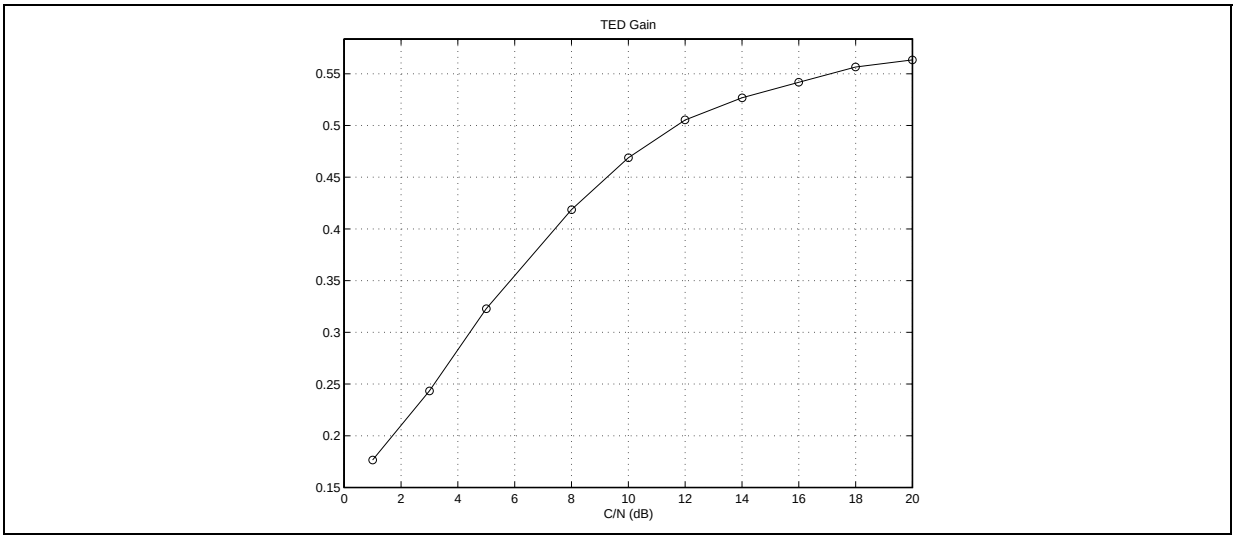
The timing error detector (TED) is based on a one sample per symbol algorithm to compute the timing error between the demodulated symbol at the matched filter output and the optimum sampling instant. The output of the detector is given by the following equation:

$$TED_{err} = I_n \times Sgn(I_{n-1}) - I_{n-1} \times Sgn(I_n) + Q_n \times Sgn(Q_{n-1}) - Q_{n-1} \times Sgn(Q_n)$$

This signal is filtered by the timing loop filter and then sent to the timing NCO to close the tracking loop.

The TED Gain (K_d) characteristic as a function of the Carrier to Noise ratio is given in fig.11. K_d = 0.56 is the value for a noise free input signal and may be reduce up to 40% of its maximum value in a low C/N condition.

Figure 11. Timing Error Detector Gain



Timing Loop Filter

The timing loop filter is a first order IIR filter with two programmable parameters, one for the proportional and the other for the integral correction, as shown in fig.6. The output of the integrator, that produces a frequency control term, is summed with the weighted timing error in the proportional path and then sent to the timing NCO to close the timing tracking loop.

The proportional gain alpha and the integral gain beta of the filter are programmable by the registers ALFATIM and BETATIM respectively. The integral gain is set by a mantissa and exponent as given by:

$$beta = beta\_m \times 2^{(beta\_e)}$$

where beta_m, the mantissa, is a 5-bit integer value set in the five LSBs of the BETATIM register (beta_m=BETATIM[4:0]) and beta_e, the exponent, is a 3-bit integer set in the three MSBs of the BETATIM register (beta_e=BETATIM[7:5]).

The proportional gain is an integer value set in the ALFATIM register with a range from 0 to 255 (alpha=ALFATIM[7:0]). The TIMINTG register collects the 8 MSBs of the filter integrator and may be read or written at any time by the system controller. When the register is written the integrator LSBs are reset.

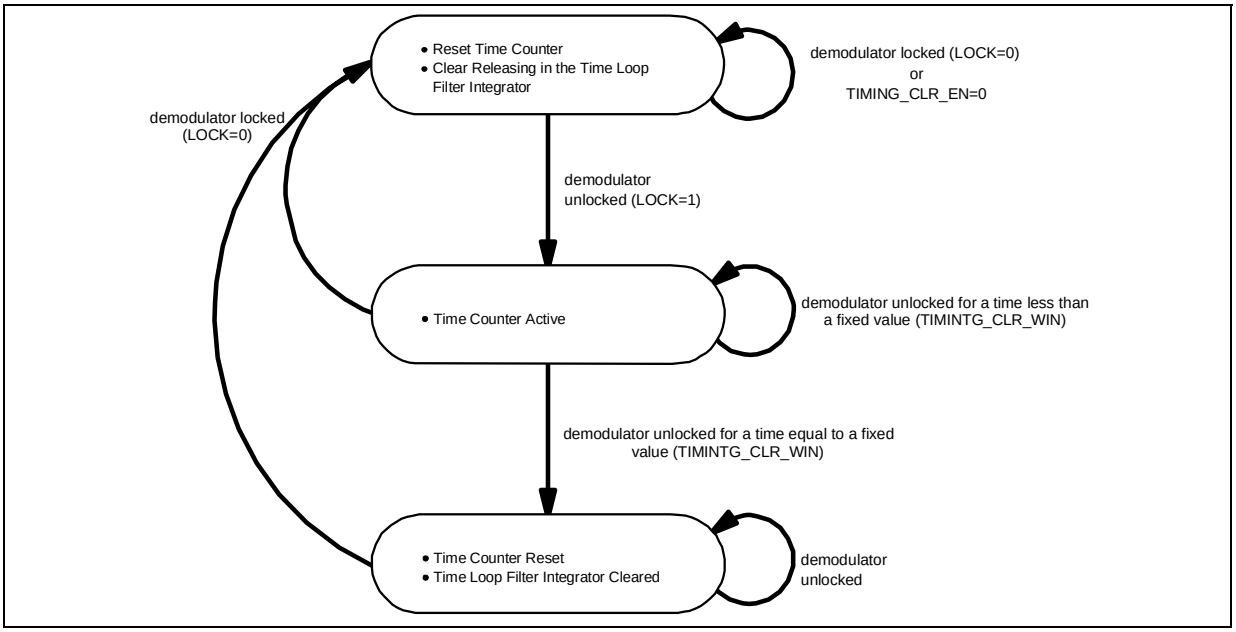
A limiter is provided on the filter integrator to limit the frequency sweep of the timing NCO. After a drop-out or during the unlock condition, the frequency uncertainty of the timing NCO (that produces a symbol slip on the demodulated data) can be controlled setting the maximum number of bit in the timing integrator. This value is set in the LIMITER block by the TIMLPF_LENGTH parameter (see TIMLPF_CTRL register). The limiter peak-to-peak range can take 8 values from 8-bits to 20-bits corresponding to a frequency shift from 182Hz to 7.5KHz respectively.

Timing Integrator Control

This block operates on the timing loop integrator. During a very long drop-out or when no signal is applied to the demodulator input, the timing loop integrator may drift up to the saturation value. As the signal is applied again or after the drop-out event, it is possible that the integrator remains in saturation for a long period causing a very slow symbol re-acquisition time. The TimintgCtrl block recognizes this event and sends a reset to the integrator register to speed-up the re-acquisition phase.

The flow diagram of the TimintgCtrl block Finite State Machine (FSM) is depicted in fig.12. The FSM parameters and the block enable/disable command are set in the TIMLPF_CTRL register

Figure 12. TimingCtrl FSM Flow Diagram



Timing Loop Equations

The timing recovery is fully digital and comprises two blocks working at symbol rate: the Timing Error Detector and the Loop Filter and two blocks working at clock rate: the Timing NCO and the Nyquist/Interpolator filters (see fig.6).

The loop is parametrised by the coefficients alpha and beta given in the registers ALFATIM and BETATIM respectively. The timing loop is a second order loop whose natural frequency f_n and damping factor ξ may be calculated by the following formulas:

$$f_n = 4.76\sqrt{mK_d beta} \quad [Hz] \qquad \zeta = 0.075\ alpha\ \sqrt{\frac{mK_d}{beta}}$$

where alpha is set in the ALFATIM register and beta in the BETATIM register, K_d is the TED gain as shown in fig.11 and m is the reference level of the AGC2 loop (see AGC2REF register).

For example, to set the loop natural frequency to 126Hz with the default value for m=AGC2REF (90dec, 5Ahex) and K_d = 0.56 (noise free value), the above equation solved for beta gives:

$$beta = \frac{f_n^2}{22.6576 mK_d} = 13.90$$

alpha can be chosen to have a damping factor equal to 0.7:

$$alpha = \frac{\zeta}{0.075}\sqrt{\frac{beta}{mK_d}} = 4.9$$

The register ALFACAR can be programmed with 5 (Dec) and the register BETACAR can be programmed with the parameter BETA_E=0 and BETA_M=14 (Dec).

C/N Estimator

This block gives the signal to noise ratio at the Nyquist filter output. It computes the statistic (mean and variance) of a single component of the demodulated complex signal and writes the estimated C/N value in dB in the CN register.

This register has a fixed point format. The integer part of the number is stored in the six MSBs (bit7-2) and the fractional part in the two LSBs (bit1-0). The C/N estimation is correct only when the QPSK demodulator is locked.

Carrier Null Offset

This block is used to enhance the acquisition performance of the carrier loop. It may be enabled/disabled setting bit-6 of the QPSK_CTRL register. The block consists of a FSM that is activated when the carrier loop has reached the lock condition (low level on at the Lock Detector output). The FSM checks if the lock detector output is low for a programmable period (see NULOFS_WIN register) and then it writes the locked carrier frequency value (read from the CARFREQ register) into the Carrier NCO. It resets also the carrier loop filter integrator and disables the frequency sweep (see fig.6).

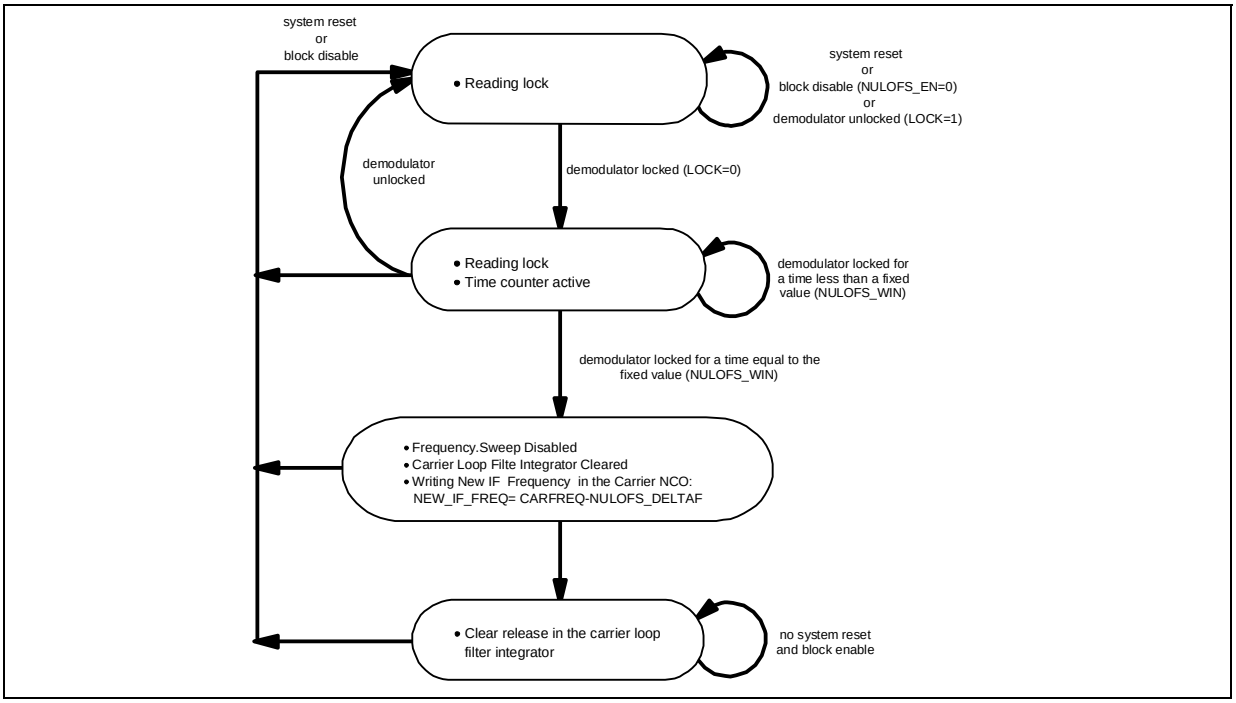
In this way the demodulator works with a null carrier offset resulting in a faster re-acquisition time of the carrier in case of a signal drop-out. The NULOFS_DELTAF register gives the possibility to subtract a programmed frequency from the locked carrier before writing the new value in the carrier NCO.

The flow diagram of the CarrierNullOffset FSM is showed in fig.13

Flag Register

A flag register is provided in the QPSK demodulator. This is a read only register containing specific status bits of the demodulator. It gives information on the lock staus and on the operation of the CarrierNullOffset and TimintgCtrl blocks.

Figure 13. CarrierNullOffset FSM Flow Diagram



1.3 TERRESTRIAL DEMODULATION (To Be Completed)

The MultiCarrier Modulated (MCM) terrestrial signal is sampled at 23.92 MHz and converted to 10-bit. The terrestrial demodulator processes these samples at four time the MCM symbol rate (4*2.99 MHz = 11.96 MHz) and includes the final down-convertion and I/Q symbol generation, low-pass filtering and down-sampling to MCM symbol rate (2.99 MHz). The MCM demodulation is performed by an FFT over 768 samples. The MultiCarrier Demodulator also includes frequency and symbol synchronization, Amplitude-Modulated Synchronisation Symbol (AMSS) detection for frame synchronisation, guard interval removal, differential decoding, demapping and metric generation.

All the MCM demodulator functionality are programmable by the microcontroller; the Register Map is listed in sections 2.3 and 2.9.

1.4 TDM DECODING (To Be Completed)

There are two different TDM structures within the DARS system, the satellite TDM and the Terrestrial TDM, carrying the same Payload Channels (PC), which are included in a 432 msec framed packet consisting of one or more Prime Rate Channel (PRC) with Reed-Solomon protection (outer encoding).

The combined satellite transmission includes a punctured rate 3/8 convolutional inner encoder (from a mother code of rate 1/3 and "1 out of 9" punctured scheme) and a convolutional interleaved with 4.698 sec. delay.

Each satellite transports one half of the punctured and interleaved PC resulting in an effective inner encoder rate of 3/4. Up to 256 PRCs are multiplexed together into a Time Division Multiplex (TDM) structure. The Time Slot Control Channel (TSCC), containing information of the TDM structure, is added at the begin of the fully FEC protected PCs. After the insertion of 1 Master Frame Preamble (MFP), 205 Fast Synchronization Preamble (FSP) and the padding field (PAD) the complete satellite Master Frame (MF) contains 1416960 bits over 432 msec, resulting in a satellite TDM bit-rate of 3.28 Mbits/sec.

The terrestrial bit-stream is a repeater signal from the satellite transmission. The inner encoder has a convolutional code rate of 3/5 (from a mother code of rate 1/3 and "4 out of 9" punctured scheme) and does not include convolutional interleaving. The terrestrial MF structure contains only 3 fields: MFP, Data Field (TSCC/PCs) and PAD resulting in a 1755360 bits over 432 msec. for a bit-rate of 4.063333 Mbits/sec.

The TDM decoder receives the demodulated symbol streams from the two satellite and the terrestrial demodulators.

The TDM processing includes Sat-Sat combining, frame synchronization, external memory management and PRC demultiplexing.

The frame synchronization is based on the MFP detection. The MFP and FSP are also used for the phase ambiguity resolution of the satellite demodulated data and for fast synchronization after a short dropout and cycle-slip.

The PRC demultiplexer processes the TSCW (Time Slot Control Word) from the TSCC field to extract all the information needed for the allocation of the PRCs to the selected PCs. Up to 50 PRCs (48 PRCs plus 2 TSCC) can be demultiplexed resulting in a maximum PC bit stream rate of 414.8 Kbit/s (384Kbit/s of useful data).

The programmable register for the TDM Decoding are explained in sections 2.4 and 2.8.

1.5 FEC (To Be Completed)

The PRC and the TSCC data from the external memory are decoded by the FEC (Viterbi Decoder, Reed-Solomon Decoder and Block Deinterleaver) and sent to the PC-BitStream Interface.

The PRC-based packet structure of the Service Layer and the external memory allow the use of one Viterbi Decoder and one RS Decoder for both the combined-satellite and terrestrial TDM frame.

The first operation of the FEC block is a data pre-processing for buffering, reordering and demultiplexing of the data streams coming from the external memory and containing both the satellite and terrestrial TDM. In this phase the depuncturing process is also performed.

The depunctured R=1/3 coded data stream (equal for combined-satellite and terrestrial) is decoded by the Viterbi Decoder using 6 bit of quantization (1 hard bit and 5 soft bits). The outer decoding process, the block deinterleaving and the satellite/terrestrial selective combining is performed by the RS decoder circuit. Additional feature of the FEC block is the Bit Error Rate estimation (computed separately for terrestrial and combined satellite) based on the re-encoding of the Viterbi decoded bit-stream.

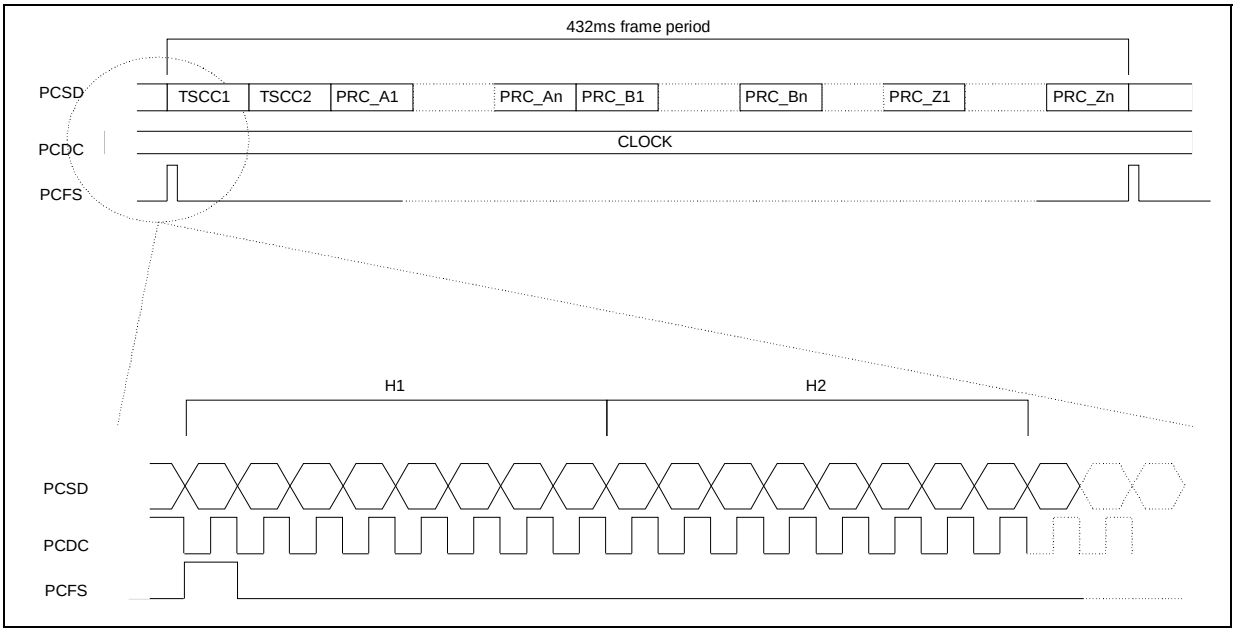
1.6 PC BITSTREAM INTERFACES

After demodulation, TDM processing and FEC decoding the CDEC delivers the TSCC and the selected PRCs to external devices for further processing. To implement this function, STA400A contains two identical Payload Channel (PC) Bitstream Interfaces (see fig.1).

Each PC Interface performs the parallel to serial conversion and the reformatting of the data packets coming from the PRC Demux Control block and provides serial data, clock and synchronization signals to the PC output ports.

The Payload Channel output protocol (showed in fig.14) is configurable, independently for the two interfaces, via the PC interface registers described in section 2.7.

Figure 14. PC Bitstream Output Protocol



The 432ms TDM frame is divided in 50 time intervals with the first two containing the TSCC data. Each time interval contains a burst of 448 bytes (2 header bytes H1 and H2, and 446 bytes of PRC data) transmitted from the PRC Demux to the PC Interface.

The PC output ports are enabled depending on the settings of the register Pcid Data Wr (addr: 0x0651-0x0652).

Each output port provides 5 signals:

- PCSD, Payload Channel Serial Data
- PCDC, Payload Channel Data Clock
- PCFS, Payload Channel PRC Frame Sync
- PCBS, Payload Channel Byte Sync

■ PCTS_EF, Payload Channel TSCC Sync / Reed-Solomon Error Flag

The PCDC frequency can be set from 11.96 MHz to 373.75 kHz via the 5 MSBs of the PCDC_CONF register (PCDC_CONF[6:2]); the clock polarity and the clock configuration (always running or fixed to '1' when the interface is not transmitting data) can be configured via the PCDC_CONF[1] and the PCDC_CONF[0] bits respectively.

The PCSD data format can be set via the PCSD_CONF register; PCSD_CONF[0] and PCSD_CONF[1] define if data are transmitted MSB or LSB first and if a parity bit is appended or not to each data byte respectively

The calculated parity can be even or odd depending on the content of PCSD_CONF[2] bit.

PCFS is the PRC packet synchronization; the default setting is one pulse at the beginning of each burst of 448 bytes. PCBS is a byte synchronization signal with one pulse at the beginning of each decoded data byte (default configuration).

PCTS_EF can be configured as the TSCC synchronization signal (default configuration) or as the Reed-Solomon error flag signal. The TSCC synchronization is a pulsed signal having period T=432ms (one pulse every TDM frame).

The width of the synchronization pulses is equal to 1 PCDC cycle. The parameters of these last three signals can be configured via the PCSYNC_CONF register.

1.7 MICROPOCESSOR INTERFACE

Data communication between the microcontroller and the device takes place through the 2 wires (SDA and SCL) IIC-bus interface. The STA400A is always a slave device.

The STA400A Register Map is organized in 8 main pages with a base address given in Table 2.2. After the device address, to read or write a register, the microcontroller must send first the base-address to select one of the 8 pages and a relative-address to select the register inside the page. The STA400A has byte or multibytes registers access with different classes (see table 2.1); the complete list of the registers is given in the Register Map section.

Interrupt Line

The interrupt line of the STA400A (pin 53 - INTR) OR-Wires 8 different interrupt requests from the CDEC that can be individually masked by the registers IRQ1_MASK (address 0x0417).

The interrupt vector is represented by the IRQ1_STATUS register (address 0x0419) described in section 2.6.

After an interrupt request, the INTR pin remains at high level, except for the MFP_CLK interrupt bit5, that is an impulse periodic signal. The IRQ1_STATUS interrupt vector may be automatically reset after the read operation or may be reset by the microcontroller (writing 0x00) depending on the bit0 of the CONTROL register (see section 2.6)

IIC-BUS Specification

The I2C-bus protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the others as the slave. The master will always initiate the transfer and will provide the serial clock for synchronisation.

Data Transition or Change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transitions while the clock is high are used to identify START or STOP condition.

Start Condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is

stable in the high state. A START condition must precede any command for data transfer.

Stop Condition

STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communications between STA400A and the bus master.

Acknowledge Bit

An acknowledge bit is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data.

During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of 8 bits of data.

Some registers do not give acknowledge when the data is not available.

Data Input

During the data input the STA400A samples the SDA signal on the rising edge of the clock SCL. For correct device operation the SDA signal has to be stable during the rising edge of the clock and the data can change only when the SCL line is low.

Device Addressing

To start communication between the master and the STA400A, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8 bits (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifier, corresponding to the I2C bus definition. For the STA400A these are fixed as 1101010.

The 8th bit (LSB) is the read or write operation bit (RW; set to 1 in read mode and to 0 in write mode). After a START condition the STA400A identifies on the bus the device address and, if matched, it will acknowledges the identification on SDA bus during the 9th bit time.

The following 2 bytes after the device identification byte are the internal space address.

Write Operation (see fig. 15)

Following a START condition the master sends a device select code with the RW bit set to 0.

The STA400A gives the acknowledge and waits for the 2 bytes of internal address. The least significant 15 bits of the 2 bytes address provides access to any of the internal registers. The most significant bit means incremental mode (1 = auto incremental enabled, 0 = auto incremental disabled).

The STA400A has an internal byte address counter. Each time a byte is written or read, this counter, according to the autoincremental bit setting, is incremented or not.

After the reception of each of the internal bytes address the STA400A again responds with an acknowledge.

Byte Write

In the byte write mode the master sends one data byte and this is acknowledged by STA400A. The master then terminates the transfer by generating a STOP condition. The Multibyte Write needs the auto incremental mode bit set to '1'.

Multibyte Write

The multibyte write mode can start from any internal address. The master sends the data and each one is acknowledged by the STA400A. The transfer is terminated by the master generating a STOP condition.

Read Operation (see Fig. 16)

Current Byte Address Read

For the current byte address read mode, following a START condition the master sends the device address with the RW bit set to 1.

The STA400A acknowledges this and outputs the byte addressed by the internal byte address counter.

The counter is then incremented or not depending on the auto incremental bit. The master does not acknowledge the received byte, but terminates the transfer with a STOP condition.

Random Byte Address Read

A dummy write is performed to load the byte address into the internal address counter.

This is followed by another START condition from the master and the device address repeated with the RW bit set to 1. The STA400A acknowledges this and outputs the byte addressed by the internal byte address counter already loaded

The master does not acknowledge the received byte, but terminates the transfer with a STOP condition.

Sequential Address Read

This mode can be initiated with either a current address read or a random address read. However in this case the master does acknowledge the data byte output and the STA400A continues to output the next byte in sequence, providing that the auto incremental mode bit be set.

To terminate the stream of bytes the master does not acknowledge the last received byte, but terminates the transfer with a STOP condition.

The output data stream is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output.

Figure 15. Write Mode Sequence

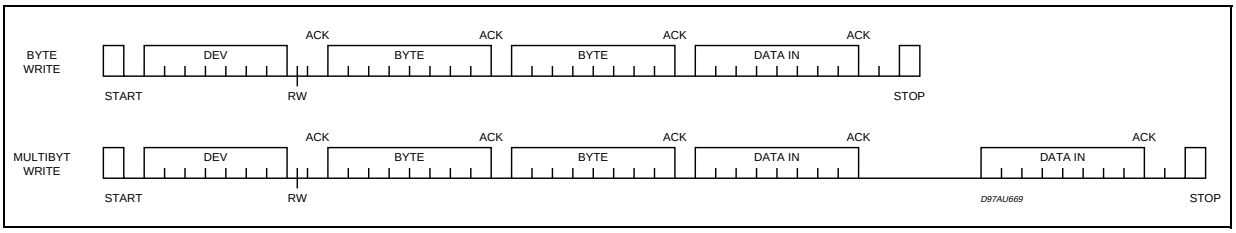
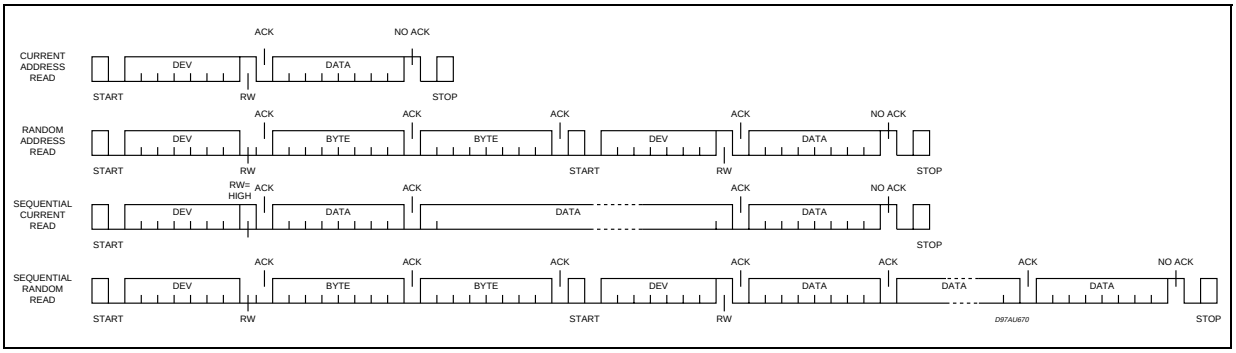


Figure 16. Read Mode Sequence



2 REGISTER MAP

Table 1. Register Classes

Abbreviations	Name of Register Class
wr	write and read
r	read
rt	read plus en-trigger
pr	preset when read
pri	preset when read plus trigger signal
wrt	write and read plus trigger signal
int	interrupt register pair
trt	transparent

pr: Event counter. (increments if input =1 and will be reset after read access to preset value)

pri: Event counter like pr-register, plus trigger output signal if maximum is arrived.

wrt: Write and read register plus trigger output signal when write access.

rt: Read only register plus trigger output signal when read access.

int: This register class always consists out of a status and mask register. The status register stores interrupt signals from CDEC. The mask registers determines if an interrupt signal should generate an irq_out signal or not.

trt: A transparent register does not exists physically in the register map. The register map pipelines the information to the CDEC register. The register operates as a normal write/read register in the register map.

Note: The pr and rt register classes must be read with the random address read mode only. Sequential read mode is not allowed.

Table 2. Base Address List

Base Address (hex)	Block
00	Satellite Demodulators (SatDem1 + SatDem2)
01	Terrestrial Demodulator (Section 1)
02	TDM (Section 1)
03	FEC
04	IF Sampling and Control Interface
05	PC Bitstream Interface
06	TDM (Section 2)
07	Terrestrial Demodulator (Section 2)

2.1 REGISTER MAP OVERVIEW

Table 3. QPSK Demodulator #1 (S1-Early)

Base Address: 00 - Address Range: 59 - 77					
Relative Address (Hex)	**Register Name**	**WL**	**Type**	**Reset Value** (Hex)	**Comment**
59	QPSK_DEMOD_EN	1	wr	01	QPSK Dem Enable Register
5A	QPSK_CTRL	8	wr	47	QPSK Dem Control Register
5B	PFDTHR	6	wr	14	Phase/Freq. Detector Threshold
5C	SYMFREQ0	8	wr	8B	Symbol Frequency (LSB)
5D	SYMFREQ1	8	wr	1A	
5E	SYMFREQ2	8	wr	23	
5F	SYMFREQ3	1	wr	00	Symbol Frequency (MSB)
60	IFFREQ0	8	wr	EC	Intermediate Frequency (LSB)
61	IFFREQ1	8	wr	C4	
62	IFFREQ2	8	wr	4E	
63	IFFREQ3	4	wr	FB	Intermediate Frequency (MSB)
64	ALFACAR	8	wr	17	Carrier Loop Filter Alpha Param.
65	BETACAR	8	wr	15	Carrier Loop Filter Beta Param.
66	ALFATIM	8	wr	07	Timing Loop Filter Alpha Param.
67	BETATIM	8	wr	0E	Timing Loop Filter Beta Param.
68	RAMPCTRL	7	wr	20	Ramp Control Register
69	AGC2BETA	3	wr	03	AGC2 Gain
6A	AGC2REF	8	wr	5A	AGC2 Reference
6B	AGC2INTG	8	wr	00	8MSB of AGC2 Loop Integrator
6C	TIMINTG	8	wr	00	8MSB of Timing Loop Integrator
6D	CARINTG	8	wr	00	8MSB of Carrier Loop Integrator
6E	CARFREQ0	8	r	--	Locked Carrier Frequency (LSB)
6F	CARFREQ1	8	r	--	
70	CARFREQ2	8	r	--	
71	CARFREQ3	4	r	--	Locked Carrier Frequency (MSB)
72	CN	8	r	--	C/N Esteem
73	FLAG	4	r	--	Demodulator Status
74	NULOFS_WIN	4	wr	07	Null Carrier Offset Window
75	NULOFS_DELTAF	8	wr	2B	Null Carrier Offset Delta Frequency
76	TIMLPF_CTRL	8	wr	90	Timing Loop Low Pass Filter Control
77	LOCKTHR	2	wr	02	Lock Detector Threshold

Table 4. QPSK Demodulator #2 (S1-Late)

Base Address: 00 - Address Range: 7F - 9D					
Relative Address (Hex)	**Register Name**	**WL**	**Type**	**Reset Value** (Hex)	**Comment**
7F	QPSK_DEMOD_EN	1	wr	01	QPSK Dem Enable Register
80	QPSK_CTRL	8	wr	47	QPSK Dem Control Register
81	PFDTHR	6	wr	14	Phase/Freq. Detector Threshold
82	SYMFREQ0	8	wr	8B	Symbol Frequency (LSB)
83	SYMFREQ1	8	wr	1A	
84	SYMFREQ2	8	wr	23	
85	SYMFREQ3	1	wr	00	Symbol Frequency (MSB)
86	IFFREQ0	8	wr	9E	Intermediate Frequency (LSB)
87	IFFREQ1	8	wr	D8	
88	IFFREQ2	8	wr	89	
89	IFFREQ3	4	wr	FC	Intermediate Frequency (MSB)
8A	ALFACAR	8	wr	17	Carrier Loop Filter Alpha Param.
8B	BETACAR	8	wr	15	Carrier Loop Filter Beta Param.
8C	ALFATIM	8	wr	07	Timing Loop Filter Alpha Param.
8D	BETATIM	8	wr	0E	Timing Loop Filter Beta Param.
8E	RAMPCTRL	7	wr	20	Ramp Control Register
8F	AGC2BETA	3	wr	03	AGC2 Gain
90	AGC2REF	8	wr	5A	AGC2 Reference
91	AGC2INTG	8	wr	00	8MSB of AGC2 Loop Integrator
92	TIMINTG	8	wr	00	8MSB of Timing Loop Integrator
93	CARINTG	8	wr	00	8MSB of Carrier Loop Integrator
94	CARFREQ0	8	r	--	Locked Carrier Frequency (LSB)
95	CARFREQ1	8	r	--	
96	CARFREQ2	8	r	--	
97	CARFREQ3	4	r	--	Locked Carrier Frequency (MSB)
98	CN	8	r	--	C/N Esteem
99	FLAG	4	r	--	Demodulator Status
9A	NULOFS_WIN	4	wr	07	Null Carrier Offset Window
9B	NULOFS_DELTAF	8	wr	2B	Null Carrier Offset Delta Frequency
9C	TIMLPF_CTRL	8	wr	90	Timing Loop Low Pass Filter Control
9D	LOCKTHR	2	wr	02	Lock Detector Threshold

Table 5. Terrestrial Demodulator (Section 1)

Base Address: 01 - Address Range: 00 - C1					
Relative Address (Hex)	**Register Name**	**WL**	**Type**	**Reset Value** (Hex)	**Comment**
00	Enable_M	8	wr	FF	enable signals for mcm submodules
01	Status1_M	8	r	00	status information of mcm submodules
02	Status2_M	2	r	00	
04	DataOvf_M	8	pr	00	overflow event counter of mcm submodules
06	IQGMode_M	3	wr	02	iq generation mode
07	Clk_devcomp_M	1	wr	01	selects mode of clk deviation compensation
08	AMSSThrL_M	7	wr	37	low threshold of AMSS detection
09	AMSSThrH_M	7	wr	41	high threshold of AMSS detection
0A	AMSSFailed_M	3	wr	07	if not more than *mrm_sync_min_amss_failed* AMSS-not-detected events : pre-sync -> hunt
0B	SyncSearch_M	4	wr	0A	Number of mcm-frames during pre sync state
0C	SyncLoss1_M	8	wr	FF	number of allowed AMSS failed events (sync -> hunt)
0D	SyncLoss2_M	3	wr	03	
0E	FrameLen_M	8	wr	B4	frame window length of AMSS detection
0F	ChannelLen_M	8	wr	B4	channel window length of AMSS detection
10	CycleCnt1_M	8	r	--	actual difference of mcm-frame cycle count to nominal value.
11	CycleCnt2_M	4	r	--	
12	CycleCntRef1_M	8	wrt	00	external setting of actual difference of mcm-frame cycle count to nominal value
13	CycleCntRef2_M	4	wrt	00	
15	AttFactor1_M	8	wr	F0	attenuation factor for correlation results.
16	AttFactor2_M	5	wr	1F	
17	HistLen_M	4	wr	0F	length of history register
19	CN1_M	8	r	--	estimated noise and signal&noise power.
1A	CN2_M	8	r	--	
1B	CN3_M	8	r	--	
1C	FfCtrl_M	6	wr	1E	control of ff internal algorithm
1D	FfBeta_M	8	wr	04	loop filter constant beta
1F	BlkDetect_M	1	wr	00	external setting of blockage condition to fc
20	InitDelay_M	2	wr	00	delay on use of ff output at startup
21	MaxFreq1_M	8	wr	46	maximum allowed difference of ff and cf to detect out-of-range condition of ff.
22	MaxFreq2_M	5	wr	00	
23	MinCf_M	8	wr	90	confidence value for cf estimation

Table 5. Terrestrial Demodulator (Section 1) (continued)

Relative Address (Hex)	Register Name	WL	Type	Reset Value (Hex)	Comment
24	CfRef1_M	8	wrt	00	external setting of cf offset value.
25	CfRef2_M	5	wrt	00	
26	CfValue1_M	8	r	--	actual cf offset value.
27	CfValue2_M	5	r	--	
28	FfScale_M	8	wr	E0	scale factor multiplied with ff value
2A	Ff_OOR_M	8	pr	00	counter for ff_out_of_range events
33	EpocEn_M	1	wr	01	epoc enable
34	DemapCtrl_M	8	wr	E0	control of demapping
35	EpocThr1_M	8	wr	00	control of epoc algorithm
36	EpocThr2_M	6	wr	06	
37	NormShift_M	4	wr	0B	normalization shift for FFT data
38	LinScale_M	8	wr	80	a linear scaling of the FFT output data
39	ShiftOvfl_M	8	pr	00	overflow counter if norm shift 0x37 is too large
3B	LimitOvfl_M	8	pr	00	overflow counter if input data for pp exeeds input range
3C	EpocCarriers1_M	8	r	--	number of carriers used for EPOC correction in current MCM symbol
3D	EpocCarriers2_M	2	r	--	
3E	EpocRotRe_M	8	r	--	EPOC correction phasor (real part)
3F	EpocRotIm_M	8	r	--	EPOC correction phasor (imag part)
40	PSFrameCnt_M	4	r	--	counter of frames during presync state
41	PS_NoAMSSCnt_M	3	r	--	counter of frames without amss detection
42	AMSSFailCnt1_M	8	r	--	counter of sequent frames without amss detection.
43	AMSSFailCnt2_M	8	r	--	
44	OivlAMSSFail1_M	8	r	--	number of failed amss dectection during an interval set by register 0x0195/96.
45	OivlAMSSFail2_M	4	r	--	
47	MaxCorrIw_M	7	rt	--	maximum correlation inside channel window
49	MaxCorrOw_M	7	rt	--	maximum correlation outside channel window
4B	MinCorrIw_M	7	rt	--	minimum correlation inside channel window
4D	MinCorrOw_M	7	rt	--	minimum correlation outside channel window
4F	FrameToggle_M	1	r	--	with each mcm frame register value changes between 0 and 1
50	CorrMaxAkt_M	7	r	--	stores the current weighted maximum correlation value inside channel window
51	CorrMaxPos1_M	8	r	--	stores the current position inside frame window.

Table 5. Terrestrial Demodulator (Section 1) (continued)

Relative Address (Hex)	Register Name	WL	Type	Reset Value (Hex)	Comment
52	CorrMaxPos2_M	3	r	--	
53	PosShift1_M	8	r	--	real shift operation after checking history.
54	PosShift2_M	4	r	--	
55	WinJump1_M	8	r	--	real jump of window.
56	WinJump2	3	r	--	
60	NCOInc1_M	8	r	--	NCO increment.
61	NCOInc2_M	8	r	--	
62	NCOInc3_M	1	r	--	
70	FfEst1_M	8	r	--	actual fine frequency value.
71	FfEst2_M	8	r	--	
72	FfEst3_M	1	r	--	
80	MctlEn_M	1	wr	00	MCM Control
81	MctlMask_M	6	wr	1F	MCM Control masks
82	MctlInit_M	1	wrt	00	MCM Control initialization trigger
83	TdmCntTh_M	8	wr	18	Number of TDM frames in lock for transition to state NO_UPDATE
84	MctlState_M	2	r	00	MCM Control Status
90	MeanAbs_M	8	r	00	Mean of absolute value of MCM output symbols
91	ClipRate_M	8	r	00	MCM output clip rate
95	OivlLenAMSSFail1_M	8	wr	8B	sets length of observation interval of reg 0x0144/45 (139 frames =~ 1 sec).
96	OivlLenAMSSFail2_M	4	wr	0F	
97	WinJpLimit1_M	8	wr	03	sets maximal allowed jump of window.
98	WinJpLimit2_M	3	wr	00	
9A	JpLimitEvt_M	8	pr	00	counts jump limit events
9B	WinJpNoLimit1_M	8	wr	00	actual requested jump of window without limit function.
9C	WinJpNoLimit2_M	3	wr	00	
B0	IQGDataOvf_M	8	pr	00	Overflow event counter of LPF inside IQGEN
B2	NCODataOvf_M	8	pr	00	Overflow event counter of NCO
B4	LPFDataOvf_M	8	pr	00	Overflow event counter of LPF
C0	IrqMask_M	2	int	00	MCM interrupt mask
C1	IrqStatus_M	2	int	00	MCM interrupt status

Table 6. TDM (Section 1)

Base Address: 02 - Address Range: 00 - CB					
Relative Address (Hex)	**Register Name**	**WL**	**Type**	**Reset Value** (Hex)	**Comment**
00	TdmEnable_S	8	wr	FF	satellite TDM decoding block enable
04	TdmSync_S1	5	wr	10	satellite one TDM decoding synchronization data control
05	MfpLength_S1	4	wr	0F	satellite one TDM decoding extended MFP detection window length
06	MfpThr_S1	7	wr	44	satellite one TDM decoding extended MFP detection threshold
07	SyncLength_S1	4	wr	03	satellite one TDM decoding synchronization window length
08	PreSyncThr_S1	4	wr	02	satellite one TDM decoding pre-synchronization lost threshold
09	SyncThr_S1	4	wr	0B	satellite one TDM decoding synchronization lost threshold
0A	FspThr_S1	6	wr	14	satellite one TDM decoding FSP invalid threshold
0B	MetricCtrl_S1	4	wr	00	satellite one TDM decoding QPSK metric generation data control
0C	Scrambler1_S1	8	wr	05	satellite one TDM decoding scrambler polynomial
0D	Scrambler2_S1	4	wr	08	
12	TdmSync_S2	5	wr	10	satellite one TDM decoding synchronization data control
13	MfpLength_S2	4	wr	0F	satellite two TDM decoding extended MFP detection window length
14	MfpThr_S2	7	wr	44	satellite two TDM decoding extended MFP detection threshold
15	SyncLength_S2	4	wr	03	satellite two TDM decoding synchronization window length
16	PreSyncThr_S2	4	wr	02	satellite two TDM decoding pre-synchronization lost threshold
17	SyncThr_S2	4	wr	0B	satellite two TDM decoding synchronization lost threshold
18	FspThr_S2	6	wr	14	satellite two TDM decoding FSP invalid threshold
19	MetricCtrl_S2	4	wr	00	satellite two TDM decoding QPSK metric generation data control
1A	Scrambler1_S2	8	wr	05	satellite two TDM decoding scrambler polynomial
1B	Scrambler2_S2	4	wr	08	
1D	MfpLock_S1	7	r	--	satellite two TDM decoding status
1E	MfpLost_S1	4	r	--	satellite one TDM decoding extended MFP counter
20	MfpW_re_S1	8	r	--	satellite one TDM decoding extended MFP correlation weight, real part
21	MfpW_im_S1	8	r	--	satellite one TDM decoding extended MFP correlation weight, imaginary part
22	FspW_re_S1	7	r	--	satellite one TDM decoding FSP correlation weight, real part

Table 6. TDM (Section 1) (continued)

Relative Address (Hex)	Register Name	WL	Type	Reset Value (Hex)	Comment
23	FspW_im_S1	7	r	--	satellite one TDM decoding FSP correlation weight, imaginary part
24	FspPhase_S1	2	r	--	satellite one TDM decoding phase
25	MfpLock_S2	7	r	--	satellite two TDM decoding status
26	MfpLost_S2	4	r	--	satellite two TDM decoding extended MFP counter
28	MfpW_re_S2	8	r	--	satellite two TDM decoding extended MFP correlation weight, real part
29	MfpW_im_S2	8	r	--	satellite two TDM decoding extended MFP correlation weight, imaginary part
2A	FspW_re_S2	7	r	--	satellite two TDM decoding FSP correlation weight, real part
2B	FspW_im_S2	7	r	--	satellite two TDM decoding FSP correlation weight, imaginary part
2C	FspPhase_S2	2	r	--	satellite two TDM decoding phase
2D	TdmEnable_T	5	wr	1F	terrestrial TDM decoding block enable
2E	MfpLength_T	4	wr	07	terrestrial TDM decoding MFP detection window length
2F	MfpThrPreSync_T	7	wr	2C	terrestrial TDM decoding MFP detection threshold, pre-synchronization
30	MfpThrSync_T	7	wr	28	terrestrial TDM decoding MFP detection threshold, synchronization
31	SyncLength_T	5	wr	03	terrestrial TDM decoding TDM synchronization window length
32	SyncThr_T	4	wr	02	terrestrial TDM decoding TDM synchronization found threshold
33	SyncLost_T	4	wr	0B	terrestrial TDM decoding TDM synchronization lost threshold
34	Scrambler1_T	8	wr	05	terrestrial TDM decoding scrambling polynomial
35	Scrambler2_T	4	wr	08	
36	DataFormat_T	4	wr	00	terrestrial TDM decoding data formatting
37	TdmStatus_T	3	r	--	terrestrial TDM decoding status
39	MfpLost_T	4	r	--	terrestrial TDM decoding MFP correlation lost
3A	MfpW_re_T	8	r	--	terrestrial TDM decoding MFP correlation weight, real part
3B	MfpW_im_T	8	r	--	terrestrial TDM decoding MFP correlation weight, imaginary part
3C	TdmPhase_T	2	r	--	terrestrial TDM decoding TDM phase
3F	TdmSyncCtrl_T	1	wr	01	terrestrial TDM decoding synchronization control
40	SwfgEnable_S	8	wr	FF	satellite weighting factor generation block enable
41	SwfgStatus_S	2	r	--	satellite weighting factor generation status
50	Prc_En	3	wr	00	0: TDM PRC interface block enable; 2:1 TDM PRC interface PRC source

Table 6. TDM (Section 1) (continued)

Relative Address (Hex)	Register Name	WL	Type	Reset Value (Hex)	Comment
51	Prc_Num1	8	wr	00	TDM PRC interface: PRC number. (Range from 1 to 258).
52	Prc_Num2	1	wr	00	
60	DescDataEn	5	wr	00	select signal for multiplexers after descrambler
61	DescData_re_T	8	wr	00	real terrestrial test data
62	DescData_im_T	8	wr	00	imag terrestrial test data
63	DescData_re_S1	4	wr	00	real satellite one test data
64	DescData_im_S1	4	wr	00	imag satellite one test data
65	DescData_re_S2	4	wr	00	real satellite two test data
66	DescData_im_S2	4	wr	00	imag satellite two test data
67	DescData_S1wfg	4	wr	00	SWFG one test data
68	DescData_S2wfg	4	wr	00	SWFG two test data
80	TpmEnable_S	2	wr	00	satellite TDM preamble monitor block enable
81	TpmDataFormat_S1	2	wr	00	satellite one TDM preamble monitor input data format
82	TpmMfpThr_S1	7	wr	28	satellite one TDM preamble monitor MFP detection threshold
83	TpmFspThr_S1	6	wr	14	satellite one TDM preamble monitor FSP detection threshold
84	TpmDataFormat_S2	2	wr	00	satellite two TDM preamble monitor input data format
85	TpmMfpThr_S2	7	wr	28	satellite two TDM preamble monitor MFP detection threshold
86	TpmFspThr_S2	6	wr	14	satellite two TDM preamble monitor FSP detection threshold
90	TpmMfpW_re_S1	8	r	--	satellite one TDM preamble monitor MFP correlation weight, real part
91	TpmMfpW_im_S1	8	r	--	satellite one TDM preamble monitor MFP correlation weight, imaginary part
92	TpmMfpSymSlip1_S1	8	r	--	satellite one TDM preamble monitor MFP symbol slip
93	TpmMfpSymSlip2_S1	4	r	--	
94	TpmFspW_re_S1	7	r	--	satellite one TDM preamble monitor FSP correlation weight, real part
95	TpmFspW_im_S1	7	r	--	satellite one TDM preamble monitor FSP correlation weight, imaginary part
96	TpmFspPosSlip1_S1	8	r	--	satellite one TDM preamble monitor FSP position slip
97	TpmFspPosSlip2_S1	4	r	--	
98	TpmFspTdmPhase_S1	2	r	--	satellite one TDM preamble monitor FSP phase
99	TpmPrDetect_S1	2	r	--	satellite one TDM preamble monitor preamble detection
9A	TpmFspCySlipCnt_S1	8	r	--	satellite one TDM preamble monitor FSP cycle slip counter

Table 6. TDM (Section 1) (continued)

Relative Address (Hex)	Register Name	WL	Type	Reset Value (Hex)	Comment
9B	TpmFspPoSlipCnt_S1	8	r	--	satellite one TDM preamble monitor FSP position slip counter
A0	TpmMfpW_re_S2	8	r	--	satellite two TDM preamble monitor MFP correlation weight, real part
A1	TpmMfpW_im_S2	8	r	--	satellite two TDM preamble monitor MFP correlation weight, imaginary part
A2	TpmMfpSymSlip1_S2	8	r	--	satellite two TDM preamble monitor MFP symbol slip
A3	TpmMfpSymSlip2_S2	4	r	--	
A4	TpmFspW_re_S2	7	r	--	satellite two TDM preamble monitor FSP correlation weight, real part
A5	TpmFspW_im_S2	7	r	--	satellite two TDM preamble monitor FSP correlation weight, imaginary part
A6	TpmFspPosSlip1_S2	8	r	--	satellite two TDM preamble monitor FSP symbol slip
A7	TpmFspPosSlip2_S2	4	r	--	
A8	TpmFspTdmPhase_S2	2	r	--	satellite two TDM preamble monitor FSP phase
A9	TpmPrDetect_S2	2	r	--	satellite two TDM preamble monitor preamble detection
AA	TpmFspCySlipCnt_S2	8	r	--	satellite two TDM preamble monitor FSP cycle slip counter
AB	TpmFspPoSlipCnt_S2	8	r	--	satellite two TDM preamble monitor FSP position slip counter
B0	TdmSySlip1_S1	8	r	--	satellite one TDM decoding symbol slip
B1	TdmSySlip2_S1	4	r	--	
B2	TdmSySlip1_S2	8	r	--	satellite two TDM decoding symbol slip
B3	TdmSySlip2_S2	4	r	--	
B4	TdmSySlip1_T	8	r	--	terrestrial TDM decoding symbol slip
B5	TdmSySlip2_T	2	r	--	
C0	FspStarWinLen_S1	3	wr	02	Satellite one TDM decoding FSP detection start window length
C1	FspHuntWinInc_S1	4	wr	03	Satellite one TDM decoding FSP detection hunt window increment
C2	FspShDropOutLen_S1	5	wr	0F	Satellite one TDM decoding FSP short dropout length
C3	FspSecuAlignThr_S1	3	wr	03	Satellite one TDM decoding FSP secure alignment threshold
C8	FspStarWinLen_S2	3	wr	02	Satellite two TDM decoding FSP detection start window length
C9	FspHuntWinInc_S2	4	wr	03	Satellite two TDM decoding FSP detection hunt window increment
CA	FspShDropOutLen_S2	5	wr	0F	Satellite two TDM decoding FSP short dropout length
CB	FspSecuAlignThr_S2	3	wr	03	Satellite two TDM decoding FSP secure alignment threshold

Table 7. FEC

Base Address: 03 - Address Range: 00 - 51					
Relative Address (Hex)	**Register Name**	**WL**	**Type**	**Reset Value** (Hex)	**Comment**
00	Control_F	6	wr	3F	control vector for FEC and FEC Preprocessing
01	Status_F	4	r	--	status flags of FEC Processing blocks (FEC Preproc, VD, FEC Mgmt, RS input control)
02	ErrorCtrl_F	6	wr	01	FEC error reporting
07	InitState_F	6	wr	2E	initial state of convolutional decoder after training sequence
08	InitLfsr1_F	8	wr	CC	initial state of flush LFSR
09	InitLfsr2_F	4	wr	0C	
0A	InitTerm1_F	8	wr	00	termination sequence after flush operation
0B	InitTerm2_F	8	wr	80	
0C	InitTerm3_F	4	wr	0B	
10	VitBerCtrl_F	4	wr	0F	Viterbi BER Measurement control flags
20	TerrBer1_F	8	r	--	Terrestrial channel error rate
21	TerrBer2_F	4	r	--	
24	Sat1Ber1_F	8	r	--	Sat1 channel error rate
25	Sat1Ber2_F	4	r	--	
28	Sat2Ber1_F	8	r	--	Sat2 channel error rate
29	Sat2Ber1_F	4	r	--	
30	ForceCorr_F	8	wr	1D	forced correction value for PRC preamble (1D hex)
31	RS_Ctrl_F	4	wr	03	RS/RS Input Control configuration bits
32	RS_Cnt_F	1	wrt	01	RS Decoder Error Counter Control
35	RS_ByeCnt1_F	8	r	--	RS byte error counter
36	RS_ByeCnt2_F	6	r	--	
37	RS_FrameCnt1_F	8	r	--	RS frame error counter
38	RS_FrameCnt2_F	2	r	--	
40	InitSeq_F	8	wr	1D	initialization sequence for VD (PRC preamble 1D hex)
42	RS1_TerrByteErr_F	5	r	--	terr. Reed-Solomon block 1 error reporting
43	RS2_TerrByteErr_F	5	r	--	terr. Reed-Solomon block 2 error reporting
44	RS1_SatByteErr_F	5	r	--	sat. Reed-Solomon block 1 error reporting
45	RS2_SatByteErr_F	5	r	--	sat. Reed-Solomon block 2 error reporting
46	RS_Block_decis_F	2	r	--	status of last Reed-Solomon diversity decision
50	IrqMask_F	5	int	00	FEC interrupt mask
51	IrqStatus_F	5	int	00	FEC interrupt status

Table 8. IF Sampling and Control Interface

Base Address: 04 - Address Range: 00 - 20					
Relative Address (Hex)	**Register Name**	**WL**	**Type**	**Reset Value** (Hex)	**Comment**
00	AGC_CTRL1	8	wr	88	Terr. and Sat. AGC Control Register1
01	SAGCREF0	8	wr	90	Satellite Agc Reference (LSB)
02	SAGCREF1	5	wr	01	Satellite Agc Reference (MSB)
03	SAGCINTG	8	wr	00	8MSB of Satellite AGC Integrator
04	TAGCREF0	8	wr	90	Terrestrial Agc Reference (LSB)
05	TAGCREF1	5	wr	01	Terrestrial Agc Reference (MSB)
06	TAGCINTG	8	wr	00	8MSB of Terr. AGC Integrator
07	IF_CTRL	2	wr	00	IF Sampling Control Register
08		8	wr	00	Reserved
09		8	wr	00	Reserved
0A	SELTSTOUT	4	wr	00	Block Functional Test Output Sel.
0B	TSTMUXCTL	4	wr	00	CDEC Functional Test Output Sel.
0C	CLKDIV_CONF	2	wr	03	Master Clock Programmable Divider
0D	QPSK_BER_CTRL		wr	00	Control of the interface for external BER measurement
0E					Reserved for Future Use
0F					Reserved for Future Use
10	CONTROL	8	wr	00	General Purpose Control
11		8	wr	00	Reserved
12		8	r	--	Reserved
13		8	r	--	Reserved
14		8	r	--	Reserved
15		8	r	--	Reserved
17	IRQ1_MASK	8	wr	00	Interrupt #1 Mask
19	IRQ1_STATUS	8	pr	00	Interrupt #1 Status
1B		8	wr	00	Reserved for Future Use
1D		8	pr	00	Reserved for Future Use
1F	STATUS1	8	r	--	General Purpose Status
20		8	r	--	Reserved for Future Use

Table 9. PC Bitstream Interface

Base Address: 05 - Address Range: 00 - 06					
Relative Address (Hex)	**Register Name**	**WL**	**Type**	**Reset Value** (Hex)	**Comment**
00	PCDC_CONF_0	7	wr	00	Clock Configuration for PC Interface #0
01	PCDC_CONF_1	7	wr	00	Clock Configuration for PC Interface #1
02	PCSD_CONF_0	6	wr	00	Output Data Configuration for PC Interface #0
03	PCSD_CONF_1	6	wr	00	Output Data Configuration for PC Interface #1
04	PCSYNC_CONF	8	wr	77	Synchronization Signals Configuration for both Interfaces
05		8	wr	00	Reserved For Future Use
06	PC_ALARM	2	pr	00	Alarm Signals for Interface #0 and #1

Table 10. TDM (Section 2)

Base Address: 06 - Address Range: 10 - F6					
Relative Address (Hex)	**Register Name**	**WL**	**Type**	**Reset Value** (Hex)	**Comment**
10	DeltaRefCyc1_M	8	r	--	delta reference cycles for MCM Frame Sync
11	DeltaRefCyc2_M	5	r	--	
20	MfpSyncMax_S1	8	wr	46	set the rightmost distance of sat1 MFP sync
21	MfpSyncMin_S1	8	wr	2F	set the leftmost distance of sat1 MFP sync
22	MfpSyncMax_S2	8	wr	46	set the rightmost distance of sat2 MFP sync
23	MfpSyncMin_S2	8	wr	2F	set the leftmost distance of sat2 MFP sync
24	MfpSyncMax_T	8	wr	11	set the rightmost distance of terrestrial MFP sync
25	MfpSyncMin_T	8	wr	29	set the leftmost distance of terrestrial MFP sync
30	Xmem_Type	1	wr	00	external memory device type
31	XmemRefCyc1	8	wr	75	external memory refresh cycle period
32	XmemRefCyc2	1	wr	01	
34	XmemMode	2	wr	00	external memory management mode
35	XmemStatus	2	r	--	external memory management status
36	XmemStErrAdr1	8	r	--	external memory management self-test error address
37	XmemStErrAdr2	8	r	--	
38	XmemStErrAdr3	8	r	--	
40	UdCycDelta1_T	8	wr	00	MFP Cycle Number Up Down Delta
41	UdCycDelta2_T	3	wr	00	
42	Cnt_Prio	8	wr	80	MFP Cycles Time Internal Setting
43	Ud_Cycles1	8	wr	9C	MFP Cycle Number Adiustment.
44	Ud_Cycles2	3	wr	00	

Table 10. TDM (Section 2) (continued)

Relative Address (Hex)	Register Name	WL	Type	Reset Value (Hex)	Comment
45	FrameLen1	8	wr	00	TDM frame length
46	FrameLen2	8	wr	AD	
47	FrameLen3	8	wr	9D	
48	DeltaCycles1	8	r	--	MFP Clock Period Monitor
49	DeltaCycles2	3	r	--	
4A	MFC1	8	r	--	Master Frame counter
4B	MFC2	3	r	--	
4C	MFC_lsb	7	r	--	Master Frame counter (LSB)
4D	Tdm2Enable	8	wr	FF	TDM management block enable
4E	XmemFifoLevel	4	r	--	External memory write access buffer filling level
4F	PcidDataRd1	8	r	--	pcid table read register
50	PcidDataRd2	2	r	--	
51	PcidDataWr1	8	wrt	00	pcid number and pcid interface enable
52	PcidDataWr2	2	wrt	00	
53	PcidAddr	5	wr	00	address of the pcid in the table
54	PRC_ti	8	wr	C8	Sets the time interval between the output of two PRCs.
55	Tscw_Err	2	wr	00	Sets what is done if the TSCW has uncorrected errors
56	Tscw_AddrRd	8	wrt	00	start address of register of TSCW table, which shall to be read
57	Tscw_Data	8	rt	--	contents of addressed TSCW word (enables autoincrement function of address when read access)
58	StatusErr_T	2	r	--	read management enable and error flag
59	MgmtCtrl_T	4	wr	03	control vector for TDM management
5B	Tscw_AddrCurr	8	r	--	address of current register of TSCW table, which is read
61-F0	BK1-BK144	8	trt	FF	TDM management bookkeeping matrix
F5	IrqMask_T	3	int	00	TDM interrupt mask
F6	IrqStatus_T	3	int	00	TDM interrupt status

Table 11. Terrestrial Demodulator (Section 2)

Base Address: 07 - Address Range: 10 - 81					
Relative Address (Hex)	**Register Name**	**WL**	**Type**	**Reset Value** (Hex)	**Comment**
10	CfCntGood1_M	8	pr	00	counter for Coarse Frequency Good events
11	CfCntGood2_M	8	pr	00	

Table 11. Terrestrial Demodulator (Section 2)

15	CfCntBad1_M	8	pr	00	counter for Coarse Frequency Bad events
16	CfCntBad2_M	8	pr	00	
18	CfCtrl_M	1	wr	00	control of cf algorithm
20	Cf_MinKexpLow_M	8	wr	90	control of confidence threshold calculation for cf estimation
21	Cf_DiffKexpMaxLow_M	8	wr	08	control of confidence threshold calculation for cf estimation
22	Cf_Delta_KexpLow_M	8	wr	01	control of confidence threshold calculation for cf estimation
23	Cf_DeltaCntLow1_M	8	wr	20	control of confidence threshold calculation for cf estimation
24	Cf_DeltaCntLow2_M	2	wr	00	
26	Cf_MaxKexpHigh_M	8	wr	FF	control of confidence threshold calculation for cf estimation
27	Cf_DiffKexpMaxHigh_M	8	wr	06	control of confidence threshold calculation for cf estimation
28	Cf_DeltaKexpHigh_M	8	wr	01	control of confidence threshold calculation for cf estimation
29	Cf_DeltaCntHigh1_M	8	wr	01	control of confidence threshold calculation for cf estimation
2A	Cf_DeltaCntHigh2_M	2	wr	00	
2B	Cf_InitDelay_M	5	wr	17	control of initial behavior of cf estimation
2D	Cf_KexpThAct_M	8	r	--	current confidence threshold value
30	Cf_EstAct1_M	8	r	--	coarse frequency estimation of received AMSS before averaging
31	Cf_EstAct2_M	8	r	--	
35	Cf_KestActExp_M	8	r	--	coarse frequency confidence exponent of received AMSS before averaging
40	Cf_Est1_M	8	r	--	coarse frequency estimation of received AMSS after averaging
41	Cf_Est2_M	8	r	--	
45	Cf_EstExp_M	8	r	--	coarse frequency confidence exponent of received AMSS after averaging
50	Cf_AvgEst1_M	8	r	--	current MCM CF Averager estimate
51	Cf_AvgEst2_M	8	r	--	
55	Cf_AvgEstExp_M	8	r	--	current MCM CF Averager confidence estimate
80	Cf_AvgCtrl	8	wr	B0	MCM Coarse Freq Averager control vector
81	Cf_AvgMinEstConf_M	8	wr	00	MCM Coarse Freq Averager: threshold for CF confidence

2.2 QPSK Demodulator (S1-Early/S2-Late)

The two QPSK demodulators (S1-Early and S2-Late) have the same register set so they have been listed below once. The registers have different addresses and the same reset value except for the IFFREQ register.

QPSK_DEMOD_EN - QPSK Demodulator Enable Register

This register disables the QPSK demodulator when bit-0 is set to '0'. When disabled the demodulator output is fixed to '0x00' or to '0x80' depending on the bit-4 setting of the QPSK_CTRL register (address 0x005A/0x0080)

Type: SingleByte - R/W **Word Length:** 1				
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
QPSK_DEMOD_EN1	S1/S2	0059/007F	7-0	01

b7-b1: Not Used

b0: DEM_EN 0=Demodulator disabled; 1=Demodulator enabled.

QPSK_CTRL - QPSK Demodulator Control Register

This is a control register for the QPSK demodulator.

Type: SingleByte - R/W **Word Length:** 8				
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
QPSK_CTRL	S1/S2	005A/0080	7-0	4F

b7: AVG_OFF This bit disables the averager filter of the integrators.
0=Averager Filter enabled; 1=Averager Filter disabled.

b6: NULOFS_EN This bit enables/disables the NULOFS block.
0=Disabled; 1=Enabled.

b5: Reserved.

b4: DEM2TDM_FMT Output Data Format.
0=Two's complement; 1=Offset binary.

b3: IQSWAP This bit swaps the I and Q component of the demodulator output.
0=No Change; 1=Swaps I with Q.

b2: QCHS This bit inverts the Q component sign in the I/Q mixer.
0=No invertion; 1=Sign invertion.

b1: TIMCHS This bit inverts the timing loop sign.
0=No invertion; 1=Sign invertion.

b0: CARCHS This bit inverts the carrier loop sign.
0=No invertion; 1=Sign invertion.

PFDTHR - Phase/Frequency Error Detector Threshold

This register sets the threshold for the frequency detector. The number format is positive integer.

Type: SingleByte - R/W **Word Length:** 6				
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
PFDTHR	S1/S2	005B/0081	5-0	14

SYMFREQ - Symbol Frequency

This register sets the symbol frequency of the Timing NCO (equal to 1.64MHz for both satellite demodulators).

It is 25 bit long and is divided into four bytes; SYMFREQ0 is the LSB byte, SYMFREQ3 is the MSB. SYMFREQ must be loaded with an interger value given by $SYMFREQ = int\left(0.5 + \frac{F_{sym}}{F_{MCLK}} 2^{25}\right)$ where F_{MCLK} = 23.92MHz is the master clock frequency, F_{sym} is the symbol frequency and Int(.) is the integer part of the number.

Type: MultiBytes - R/W **Word Length:** 25				
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
SYMFREQ3	S1/S2	005F/0085	24	00
SYMFREQ2	S1/S2	005E/0084	23-16	23
SYMFREQ1	S1/S2	005D/0083	15-8	1A
SYMFREQ0	S1/S2	005C/0082	7-0	8B

IFFREQ - Intemediate Frequency

This register sets the 2nd intermediate carrier frequency of the I/Q Mixer. It is 28 bit long and is divided into four bytes; IFFREQ0 is the LSB byte, IFFREQ3 is the MSB. IFFREQ must be loaded with an interger value given by $IFFREQ = int\left(0.5 + \frac{F_c}{F_{MCLK}} 2^{28}\right)$ where F_{MCLK} = 23.92MHz is the master clock frequency, F_c is the second intermediate frequency (5.175MHz for S2-Late satellite and 7.015MHz for S1-Early satellite) and Int(.) is the integer part of the number.

Type: MultiBytes - R/W **Word Length:** 28				
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
IFFREQ3	S1/S2	0063/0089	27-24	04/03
IFFREQ2	S1/S2	0062/0088	23-16	B1/76
IFFREQ1	S1/S2	0061/0087	15-8	3B/27
IFFREQ0	S1/S2	0060/0086	7-0	14/62

ALFACAR - Carrier Loop Filter Alpha Parameter

This register sets the proportional gain of the carrier loop. It must be loaded with a positive integer number from 0x00 to 0xFF (0 to 255 decimal).

Type: SingleByte - R/W **Word Length:** 8				
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
ALFACAR	S1/S2	0064/008A	7-0	17

b7-b0: ALPHA Positive integer, range 0 to 255 decimal.

BETACAR - Carrier Loop Filter Beta Parameter

This register sets the integral gain of the carrier loop. The representation of the number is mantissa-exponent (base 2): beta = beta_m x $2^{(beta\_e)}$

Type: SingleByte - R/W **Word Length:** 8				
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
BETACAR	S1/S2	0065/008B	7-0	15

b7-b5: BETA_E Exponent of the number. Positive integer, range 0 to 7 decimal.

b4-b0: BETA_M Mantissa of the number. Positive integer, range 0 to 31 decimal.

ALFATIM - Timing Loop Filter Alpha Parameter

This register sets the proportional gain of the timing loop. It must be loaded with a positive integer number from 0x00 to 0xFF (0 to 255 decimal).

Type: SingleByte - R/W **Word Length:** 8				
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
ALFATIM	S1/S2	0066/008C	7-0	07

b7-b0: ALPHA Positive integer, range 0 to 255 decimal.

BETATIM - Timing Loop Filter Beta Parameter

This register sets the integral gain of the timing loop. The representation of the number is mantissa-exponent (base 2): beta = beta_m x $2^{(beta\_e)}$

Type: SingleByte - R/W **Word Length:** 8				
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
BETATIM	S1/S2	0067/008D	7-0	0E

b7-b5: BETA_E Exponent of the number. Positive integer, range 0 to 7 decimal.

b4-b0: BETA_M Mantissa of the number. Positive integer, range 0 to 31 decimal.

RAMPCTRL - **Frequency Sweep Control Register**

This register controls the operation of the frequency sweep block.

Type: SingleByte - R/W **Word Length:** 7				
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
RAMPCTRL	S1/S2	0068/008E	6-0	20

b7: RFU

b6: SLOPE 0=Positive; 1=Negative

b5: SWON 0=Sweep Disabled; 1=Sweep Enabled

b4: SWSTEP 0=Multiply by 1; 1=Multiply by 2

b3-b0: STEPPER 0000=Divide by 1

0001=Divide by 2

.

1111=Divide by 16

AGC2BETA - **AGC2 Loop Gain**

This register sets the AGC2 Loop Gain according to the following formula: $\beta_{AGC2} = 2^{AGC2BETA}$

Type: SingleByte - R/W **Word Length:** 3				
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
AGC2BETA	S1/S2	0069/008F	2-0	03

b7-b3: Not Used

b2-b0: AGC2BETA

000 -> Gain=1	011 -> Gain=8	110 -> Gain=64
001 -> Gain=2	100 -> Gain=16	111 -> Gain=0
010 -> Gain=4	101 -> Gain=32	

AGC2REF - **AGC2 Reference**

This registers sets the reference level or the AGC2 loop. The format is positive integer from 0 to 255 decimal.

Type: SingleByte - R/W **Word Length:** 8				
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
AGC2REF	S1/S2	006A/0090	7-0	5A

b7-b0: AGC2REF Positive integer, range 0 to 255 decimal

AGC2INTG - **8 MSBs of AGC2 Loop Integrator**

This register contains the 8 MSBs of the AGC2 loop integrator. The format is two's complement.

Type: SingleByte - R/W **Word Length:** 8				
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
AGC2INTG	S1/S2	006B/0091	7-0	00

TIMINTG - 8 MSBs of Timing Loop Integrator

This register contains the 8 MSBs of the timing loop integrator. The format is two's complement.

Type: SingleByte - R/W	**Word Length:** 8			
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TIMINTG	S1/S2	006C/0092	7-0	00

CARINTG - 8 MSBs of Carrier Loop Integrator

This register contains the 8 MSBs of the carrier loop integrator. The format is two's complement.

Type: SingleByte - R/W	**Word Length:** 8			
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
CARINTG	S1/S2	006D/0093	7-0	00

CARFREQ - Locked Carrier Frequency

This register is 28 bit long and is divided into four bytes; CARFREQ0 is the LSB byte, CARFREQ3 is the MSB. It contains the carrier frequency on which the demodulator is locked. The format is two's complement.

Type: MultiBytes - R	**Word Length:** 28			
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
CARFREQ3	S1/S2	0071/0097	27-24	--
CARFREQ2	S1/S2	0070/0096	23-16	--
CARFREQ1	S1/S2	006F/0095	15-8	--
CARFREQ0	S1/S2	006E/0094	7-0	--

CN - Carrier to Noise Esteem

This register gives the Carrier to Noise Ratio estimation in dB. The number has a fixed point format.

Type: SingleByte - R	**Word Length:** 8			
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
CN	S1/S2	0072/0098	7-0	--

b7- **b3** : Integer Part
b2- **b0** : Fractional Part
Example : CN = '10010111' = (100101.11)bin = (37.75)dec => C/N = 37.75dB

FLAG - Demodulator Status Register

This is a read only register containing specific status bit of the demodulator.

Type: SingleByte - R	**Word Length:** 4			
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FLAG	S1/S2	0073/0099	7-4	--

b7: LOCK 0=Demodulator Locked; 1=Demodulator Unlocked

b6: TIMINTG_CLR 0=Timing Integrator Cleared; 1=Timing Integrator Active

b5: CARINTG_CLR 0=Carrier Integrator Cleared; 1=Carrier Integrator Active

b4: CLR_RAMP 0=Ramp Cleared; 1=Ramp Active

b3-**b0**: RFU

NULOFS_WIN - **Null Carrier Offset Window**

The CarrierNullOffset block writes the new IF Frequency in the Carrier NCO if the demodulator lock signal is low for a period of time equal to the value written in this register. The window length is given in msec.

Type: SingleByte - R/W **Word Length:** 4				
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
NULOFS_WIN	S1/S2	0074/009A	3-0	07

b3-**b0**: NULOFS_WIN

0000 -> 10msec	0100 -> 50msec	1000 -> 175msec	1100 -> 350msec
0001 -> 20msec	0101 -> 100msec	1001 -> 200msec	1101 -> 400msec
0010 -> 30msec	0110 -> 125msec	1010 -> 250msec	1110 -> 450msec
0011 -> 40msec	0111 -> 150msec	1011 -> 300msec	1111 -> 500msec

NULOFS_DELTAF - **Null Carrier Offset Delta Frequency**

The CarrierNullOffset block subtracts from the locked carrier frequency the value contains in this register before writing the new IF Frequency in the Carrier NCO. The register format is two's complent.

Given a frequency FREQ in Hz, the value to load in the register is given by:

$$NULOFS\_DELTAF = Int\left[FREQ\frac{2^{28}}{512F_{MCLK}} + 0.5\right]$$ where Int(.) is the integer function.

Type: SingleByte - R/W **Word Length:** 8				
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
NULOFS_DELTAF	S1/S2	0075/009B	7-0	2B

TIMLPF_CTRL - Timing Loop Filter Control

This register controls the operation of the Timing Loop Filter.

Type: SingleByte - R/W **Word Length:** 8				
Byte Name		**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TIMLPF_CTRL	S1/S2	0076/009C	7-0	90

b7: TIMAVG_OFF 0=Self-Noise Filter enabled; 1=Self-Noise Filter disabled.

b6-b5: TIMINTG_CLR_WIN

00 -> Window=10sec	10 -> Window=40sec
01 -> Window=20sec	11 -> Window=60sec

b4: TIMINTG_CLR_EN 0=TimintgCtrl block disabled; 1=TimintgCtrl block enabled

b3: RFU

b2-b0: TIMLPF_LENGTH 000 -> Timing Integrator bit length =8100 -> Timing Integrator bit length =14
001 -> Timing Integrator bit length =9101 -> Timing Integrator bit length =16
010 -> Timing Integrator bit length =10110 -> Timing Integrator bit length =18
011 -> Timing Integrator bit length =12111 -> Timing Integrator bit length =20

LOCKTHR - Lock Detector Threshold

This register sets the threshold for the lock detector block.

Type: SingleByte - R/W **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
LOCKTHR S1/S2	0077	1-0	02

b1-b0: LOCKTHR 00 -> Threshold = 32 dec
01 -> Threshold = 64 dec
10 -> Threshold = 80 dec
11 -> Threshold = 96 dec

2.3 Terrestrial Demodulator (Section 1)

Enable_M - **MCM Demodulator Enable Register**

MCM Submodules Enable Signals. Enable active on '1'.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Enable_M	0100	7-0	FF

b7: mrm_ff_demod_en enable of Fine Frequency submodule
b6: mrm_fc_demod_en enable of Frequency Control submodule
b5: mrm_cf_demod_en enable of Coarse Frequency submodule
b4: mrm_ss_demod_en enable of Symbol Synchronization submodule
b3: mrm_fs_demod_en enable of Frame Synchronization submodule
b2: mrm_pp_demod_en enable of Pre Processing submodule
b1: mrm_fft_demod_en enable of FFT submodule
b0: mrm_iqg_demod_en enable of I/Q Generation submodule

Status_M - **MCM Demodulator Status Register**

Status information of mcm submodule

Type: MultiBytes - R **Word Length:** 10			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
STATUS2_M	0102	9-8	--
STATUS1_M	0101	7-0	--

b9 : mfc_freq_lock 0= NO LOCK; 1= LOCK
b8 : mff_ff_state 0=IDLE; 1= OPERATIONAL
b7-b6 : mfc_fc_state 00= IDLE
01= INIT
10= TRACKING
11= FREEZE
b5 : mcf_cf_state 0=IDLE; 1= OPERATIONAL
b4 : mss_ss_state 0= IDLE; 1= ACTIVE (channel window active)
b3-b2 : mfs_fs_state 00= IDLE
01= HUNT
10= PRE SYNC
11= SYNC
b1 : mpp_pp_state 0=IDLE; 1= OPERATIONAL
b0 : mfft_fft_state 0=IDLE; 1= OPERATIONAL

DataOvf_M - **MCM Demodulator Blocks Overflow Register**

Overflow bit event counter of iqgen, lpf and nco.The internal overflow bits are “ored” and counted. This may be an indication that the input signal is to strong so that internal overflow occurs.

Type: SingleByte - PR **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
DataOvf_M	0104	7-0	00

IQGMode_M - **IQ Generation Mode**

Inverts and interchanges of I and Q at the output of the IQ Generation. Required for A,B ensemble switch. For ensemble A value of 02h and for ensemble B the default value of 00h must be used.

Type: SingleByte - R/W **Word Length:** 3			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
IQGMode_M	0106	2-0	02

b2 : Interchange of Re and Im data
b1 : Sign Invertion of Im data
b0 : Sign Invertion of Re data

Clk_devcomp_M - **Clock Deviation Compensation Mode**

Type: SingleByte - R/W **Word Length:** 1			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Clk_devcomp_M	0107	0	01

b0 : ‘1’=Signal coming from TDM management will be used
‘0’=Signal coming from Register Map (CycleCntRe) will be used

AMSSThrL_M - **AMSS Detection Low Threshold**

If the correlation exceeds this threshold a valid AMSS sequence is recognized and the Channel window is started.

Type: SingleByte - R/W **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
AMSSThrL_M	0108	6-0	37

AMSSThrH_M - **AMSS Detection High Threshold**

This threshold is used in addition to mrm_amss_low_corr_th to improve performance for good channels showing a high correlation value.

Type: SingleByte - R/W **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
AMSSThrH_M	0109	6-0	41

AMSSFailed_M - **AMSS Not Detected Event**

This register sets the number of events that are necessary to reach the sync state within SyncSearch_M subsequent *frame_windows*. Otherwise the state machine will be set back to the hunt state.

Type: SingleByte - R/W **Word Length:** 3			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
AMSSFailed_M	010A	2-0	07

SyncSearch_M - **Pre-Synch MCM Frames Number**

See AMSSFailed_M for description

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
SyncSearch_M	010B	3-0	0A

SyncLoss_M - **Number of Allowed AMSS Failed Event**

If AMSS failed events equal to the value ste in this register occurs subsequently, the state machine will be set back to the hunt state.

Type: MultiBytes - R/W **Word Length:** 11			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
SyncLoss2_M	010D	10-8	03
SyncLoss1_M	010C	7-0	FF

FrameLen_M - **AMSS Detection Frame Window Length**

This register sets the window value within which, before and after the expected AMSS sequence, the occurance of the AMSS sequence is searched. Value corresponds to mcm symbol rate

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FrameLen_M	010E	7-0	B4

ChannelLen_M - **AMSS Detection Channel Window Length**

Window while searching for higher AMSS correlation peaks. Value corresponds to mcm symbol rate.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
ChannelLen_M	010F	7-0	B4

CycleCnt_M - **MCM Frame Cycle Count Difference wrt Nominal Value**

This value is computed due to the internal clock adjustment based on MFP evaluation.

Type: MultiBytes - R **Word Length:** 12			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
CycleCnt2_M	0111	11-8	--
CycleCnt1_M	0110	7-0	--

CycleCntRef_M - **MCM Frame Cycle Count Difference Setting**

External setting of actual difference of mcm-frame cycle count to nominal value.

Type: MultiBytes - WRT **Word Length:** 12			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
CycleCntRef2_M	0113	11-8	00
CycleCntRef1_M	0112	7-0	00

AttFactor_M - **Attenuation Factor**

Attenuation factor for correlation results inside channel window. Used for determination of guard window position.

Type: MultiBytes - R/W **Word Length:** 13			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
AttFactor2_M	0116	12-8	1F
AttFactor1_M	0115	7-0	F0

attenuation function:

$$\alpha(k) = 10^{\frac{k}{2k_0} \cdot \frac{a}{20dB}} \quad ; \quad \alpha(k+1) = \alpha(k) + b$$

k_0 = channel window length (in Symbol Rate), *a* = attenuation factor (in dB) and b= corr_weight_factor / 2^{13}

$$b = 10^{\frac{k}{2k_0} \cdot \frac{a}{20dB}}$$

Constant Channel Window (Ko=180 samples):

Attenuation	b (*2^{13})
0dB	8192
3dB	8184
6dB	8176
12dB	8160

Constant Attenuation (3dB):

Channel Window	b(*2^{13})
180	8184
90	8176
45	8160

HistLen_M - **History Register Length**

Stores the last 15 shift operations of the window start position. The chosen value will restrict the array out of which the minimum shift operation will be searched.

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
HistLen_M	0117	3-0	0F

b3-b0 : 0000=Current correlation maximum will be proceeded

.

1111=Current and the last 15 correlation positions will be taken account

CN_M - **Estimated Noise ans Signal to Noise Power**

Uses 12 adjacent carriers besides the active carriers. Estimates power within these 24 adjacent carriers (mff_n_guard) and power within all 637 active carriers (mff_cpn_act).

Type: MultiBytes - R **Word Length:** 24			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
CN3_M	011B	23-16	--
CN2_M	011A	15-8	--
CN1_M	0119	7-0	--

b23-b12 : mff_n_guard

b11-b0 : mff_cpn_act

FfCtrl_M - **Fine Frequency Control Register**

If mrm_ff_fed_mean_en is set to '1' the ouput of the FED is averaged over two adjacent mcm symbols. If mrm_ff_lpf_sel is set to '1' an IT1 controller is implemented, otherwise a pure I controller. The mrm_ff_alpha value determines the integral part for both IT1 and I controller.

Type: SingleByte - R/W **Word Length:** 6			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FfCtrl_M	011C	5-0	1E

b5-b2: mrm_ff_alpha

b1: mrm_ff_lpf_set

b0: mrm_ff_fed_mean_en

FfBeta_M - **Fine Frequency Loop Filter Beta Constant**

If mrm_ff_lpf_sel is set to '1' the mrm_ff_beta value sets the proportional part for the IT1 controller. For a pure I controller mrm_ff_beta is not used.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FfBeta_M	011D	7-0	04

BlkDetect_M - **Frequency Control Blockage Condition**

During blockage (mrm_blockage_detect = '1') the Frequency Control state is set to FREEZE. In that state the frequency offset is held and no further actions are untertaken.

Type: SingleByte - R/W **Word Length:** 1			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
BlkDetect_M	011F	0	00

b0: mrm_blockage_detect

InitDelay_M - **Fine Frequency Statup Delay**

This register sets the number for which the Frequency Control remains within the INIT state before entering the TRACKING state, i.e. the corresponding number of Fine Frequency estimates are discarded after external reset or internal clear.

Type: SingleByte - R/W **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
InitDelay_M	0120	1-0	00

MaxFreq_M - **Fine Frequency Out-Of-Range Setting**

Maximum Allowed Difference of fine frequency and coarse frequency estimation to Detect Out-of-Range Condition of ff. If the difference between Fine and Coarse Frequency estimation is equal or larger than this value, the Fine Frequency is considered out of range and is internally cleared. The value is in units of 91.25Hz (2.99e6/32368).

Type: MultiBytes - R/W **Word Length:** 13			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MaxFreq2_M	0122	12-8	00
MaxFreq1_M	0121	7-0	46

MinCf_M - **Coarse Frequency Estimation Confidence Value**

Only Coarse Frequency estimations with a confidence value equal or larger than the value set in this register are considered as valid and loaded into the internal coarse frequency estimation value register.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MinCf_M	0123	7-0	90

CfRef_M - **Coarse Frequency Offset Setting**

External value for coarse frequency estimation. This value will be overwritten if the Coarse Frequency delivers valid estimations. The value is in units of 91.25Hz (2.99e6/32768).

Type: MultiBytes - WRT **Word Length:** 13			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
CfRef2_M	0125	12-8	00
CfRef1_M	0124	7-0	00

CfValue_M - **Coarse Frequency Offset Value**

The value is in units of 91.25Hz (2.99e6/32768).

Type: MultiBytes - R **Word Length:** 13			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
CfValue2_M	0127	12-8	--
CfValue1_M	0126	7-0	--

FfScale_M - **Fine Frequency Scale Factor**

Factor that is multiplied with the Fine Frequency estimates to get the Frequency Control's internally used estimate. The msb bit has a weight of 0.5, i.e. a value of FF h is interpreted as a factor of 255/256. This value has to considered together with the control constants of the Fine Frequency Control loop.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FfScale_M	0128	7-0	E0

Ff_OOR_M - **Fine Frequency Out-Of-Range Counter**

This counter counts up if the Fine Frequency Estimate is considered as out of range and the Fine Frequency Control loop is reset (see register max Freq_M, addr: 0x0121/22).

Type: SingleByte - PR **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Ff_OOR_M	012A	7-0	00

EpocEn_M - **Error Phase Offset Correction Enable**

If this bit is set, the EPOC algorithm inside the Post Processing is enabled

Type: SingleByte - R/W **Word Length:** 1			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
EpocEn_M	0133	0	01

DemapCtrl_M - **Demapping Control**

The Re and Im input values are cross added to get the output Re and Im values corresponding to the metric used for the FEC. This register determines this metric generation calculations.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
DemapCtrl_M	0134	7-0	E0

b7: sign control inverts Re input value for the Re output

b6: sign control inverts Im input value for the Re output

b5: sign control inverts Re input value for the Im output

b4: sign control inverts Im input value for the Im output

b3: pass control force zero of Re input value for the Re output

b2: pass control force zero of Im input value for the Re output

b1: pass control force zero of Re input value for the Im output

b0: pass control force zero of Im input value for the Im output

EpocThr_M - Error Phase Offset Correction Threshold

Only carriers with a Re value equal or larger than mrm_epoc_thresh are taken for the EPOC internally calculations. The value is relative to the dynamic range of the signal. A value of 0FFF corresponds to 2047/2048. The msb must be set always to '0'.

Type: MultiBytes - R/W **Word Length:** 14			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
EpocThr2_M	0136	13-8	06
EpocThr1_M	0135	7-0	00

NormShift_M - FFT Normalization

Normalization factor for FFT output. This register scales the FFT output by a factor of $2^{norm\_shift\_M}$. (mantissa only)

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
NormShift_M	0137	3-0	0B

LinScale_M - FFT Output Linear Scaling

The register mrm_lin_scale performs a linear scaling of the FFT output data. The register values from 0 to 255 correspond to an actual scaling factor of Lin_scale_M/128, i.e. from 0 to 255/128. The default of 128 corresponds to a scaling factor of 1.0.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
LinScale_M	0138	7-0	80

ShiftOvfl_M - NormShift Overflow Counter

Overflow counter of FFT shift and norm shift together. The counter trigger is set if the normalization 0x37 is too large so that overall scaling is too large.

Type: SingleByte - PR **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
ShiftOvfl_M	0139	7-0	00

LimitOvfl_M - Pre Processing Overflow Counter

Overflow event counter if the range of scale FFT data exceeds input range of PreProcessing.

Type: SingleByte - PR **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
LimitOvfl_M	013B	7-0	00

EpocCarriers_M - **Number of Carrier for Error Phase Offset Correction**

Shows the number of utilized active sub-carriers to compute EPOC correction phasor for current MCM symbol. Number can range from 0 to 636 (=0x27C).

Type: MultiBytes - R **Word Length:** 10			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
EpocCarriers2_M	013D	9-8	--
EpocCarriers1_M	013C	7-0	--

EpocRotRe_M - **Error Phase Offset Correction Phasor (Real Part)**

Real part of EPOC correction phasor. The value is in 2's complement with a range from -1 to $1 - 2^{-7}$ quantized with 8 bits.

Type: SingleByte - R **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
EpocRotRe_M	013E	7-0	--

EpocRotIm_M - **Error Phase Offset Correction Phasor (Imaginary Part)**

Imaginary part of EPOC correction phasor. The value is in 2's complement with a range from -1 to $1 - 2^{-7}$ quantized with 8 bits.

Type: SingleByte - R **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
EpocRotIm_M	013F	7-0	--

PSFrameCnt_M - **Frame Counter in Pre Sync State**

Counter of frames during presync state

Type: SingleByte - R **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
PSFrameCnt_M	0140	3-0	--

PS_NoAMSSCnt_M - **Frame Counter Without AMSS Detection**

Type: SingleByte - R **Word Length:** 3			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
PS_NoAMSSCnt_M	0141	2-0	--

AMSSFailCnt_M - **Sequent Frame Counter Without AMSS Detection**

Counter of sequent frames without AMSS detection during sync state. It will be reset after one succesfull detection

Type: MultiBytes - R **Word Length:** 16			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
AMSSFailCnt2_M	0143	15-8	--
AMSSFailCnt1_M	0142	7-0	--

OivlAMSSFail_M - **AMSS Failed Detection Number**

Number of failed amss detections during an interval whose length can be set by register adr. 0x0196/96

Type: MultiBytes - R **Word Length:** 12			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
OivlAMSSFail2_M	0145	11-8	--
OivlAMSSFail1_M	0144	7-0	--

MaxCorrIw_M - **Maximum Correlation Inside Channel Window**

Type: SingleByte - RT **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MaxCorrIw_M	0147	6-0	--

MaxCorrOw_M - **Maximum Correlation Outside Channel Window**

Type: SingleByte - RT **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MaxCorrOw_M	0149	6-0	--

MinCorrIw_M - **Minimum Correlation Inside Channel Window**

Type: SingleByte - RT **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MinCorrIw_M	014B	6-0	--

MinCorrOw_M - **Minimum Correlation Outside Channel Window**

Type: SingleByte - RT **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MinCorrOw_M	014D	6-0	--

FrameToggle_M - **Frame Toggle Flag Register**

Type: SingleByte - R **Word Length:** 1			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FrameToggle_M	014F	0	--

CorrMaxAkt_M - **Actual Maximum Correlation Inside Channel Window**

This value stores the actual weighted maximum correlation value inside the channel window

Type: SingleByte - R **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
CorrMaxAkt_M	0150	6-0	--

CorrMaxPos_M - **Actual Correlation Position Inside Frame Window**

This value stores the actual position inside the channel window of weighted maximum correlation value:

Type: MultiBytes - R **Word Length:** 11			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
CorrMaxPos2_M	0152	10-8	--
CorrMaxPos1_M	0151	7-0	--

PosShift_M - **Shift After History Checking**

Type: MultiBytes - R **Word Length:** 12			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
PosShift2_M	0154	11-8	--
PosShift1_M	0153	7-0	--

WinJump_M - **Window Jump**

Type: MultiBytes - R **Word Length:** 11			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
WinJump2_M	0156	10-8	--
WinJump1_M	0155	7-0	--

NCOInc_M - **NCO Increment**

The register provides the current NCO increment. The value is in 2's complement with a resolution of 5.703 Hz per LSB. This corresponds to a maximum control range of ± 2^{16} * 5.703 Hz= ± 373.75 kHz (± 156 ppm @ 2.4 GHz).

Type: MultiBytes - R **Word Length:** 17			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
NCOInc3_M	0162	16	--
NCOInc2_M	0161	15-8	--
NCOInc1_M	0160	7-0	--

FfEst_M - Actual Fine Frequency Value

The register provides the current value of the fine frequency contribution to the NCO increment. The value is in 2's complement with a resolution of 5.703 Hz per LSB.

Type: MultiBytes - R **Word Length:** 17			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FfEst3_M	0172	16	--
FfEst2_M	0171	15-8	--
FfEst1_M	0170	7-0	--

MctlEn_M - MCM Demodulator Control

MCM Control is enabled if his register is set to '1', disabled if set to '0'. The reset value enables this block.

Type: SingleByte - R/W **Word Length:** 1			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MctlEn_M	0180	0	00

MctlMask_M - MCM Demodulator Control Mask

This register is a mask vector for internal state transitions and output control signals of MCM Control. The output signals are masked out, i.e. set to logic 0, when the corresponding output mask bit (bits 0,1 or 2) is set to 0. By default the outputs are not masked. If transition mask 2 (bit 5) is set to 0, signal full_avg_len of the MCM CF Averager is taken as is, otherwise it is internally forced to 1. If transition mask 1 (bit 4) is set to 0, the transition from state NO_UPDATE to TDM_LOCK of MCM Control is disabled. By default it is enabled. If transition mask 0 (bit 3) is set to 0, the transition from state NO_UPDATE to FS_LOCK of MCM Control is disabled. By default it is enabled. Setting bits 3 and 4 to '0' means that after entering the state NO_UPDATE this state is not left except when forced by a block disable (reg. 0x180 set to 0) or an external initialization (reg 0x182 set to 1).

Type: SingleByte - R/W **Word Length:** 6			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MctlMask_M	0181	5-0	1F

b5: full_avg_len
b4: tdm_lock
b3: fs_lock
b2: timeout_disa
b1: fc_noup
b0: fs_init

MctlInit_M - **MCM Demodulator Control Initialization Trigger**

Setting this register to 1 will trigger an intialization of MCM Control when not already in state IDLE (then no action would occur). This action also triggers an initialization of MCM Frame Sync and MCM Coarse Frequency.

Type: SingleByte - R/W **Word Length:** 1			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MctlInit_M	0182	0	00

TdmCntTh_M - **Number of TDM Frames in Lock**

The register value corresponds to the number of subsequent TDM frames which have to be in lock before state NO_UPDATE is entered.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TdmCntTh_M	0183	7-0	18

MctlState_M - **MCM Demodulator Control Status**

This register displays the internal state of MCM Control.

Type: SingleByte - R **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MctlState_M	0184	1-0	--

b1-b0: 00 -> Status=IDLE
01 -> Status=FS_LOCK
10 -> Status=TDM_LOCK
11 -> Status=NO_UPDATE

MeanAbs_M - **MCM Demodulator Output Symbols Mean**

The register provides the mean of the amplitude of real and imaginary part of the MCM output symbols. The value range is from 0 to 255 =0xFF. The absolute value is in multiples of 1/256.

Type: SingleByte - R **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MeanAbs_M	0190	7-0	--

ClipRate_M - **MCM Demodulator Output Clip Rate**

The register provides the clipping rate of the MCM output. The value range is from 0 to 0xFF (255). The clipping rate is in multiples of 1/256, i.e. 0xFF corresponds to full clipping, 0x80 to 50% clipping rate.

Type: SingleByte - R **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
ClipRate_M	0191	7-0	--

OivlLenAMSSFail_M - **Observation Interval Length**

This register sets the length of observation interval of the register "*OivlAMSSFail*" (Addr: 0x0144/45).

$$OivlLen = \frac{T_{ivl}}{T_{MF}} \; ; \quad \text{MCM Frame length: } \boldsymbol{T_{MF}}\textit{=7,2 msec}$$

Type: MultiBytes - R/W **Word Length:** 12			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
OivlLenAMSSFail2_M	0196	11-8	0F
OivlLenAMSSFail1_M	0195	7-0	8B

b11-b0: 0x086 -> Interval (T_{ivl}) = 1.0 sec
0x2B6 -> Interval (T_{ivl}) = 5.0 sec
0x56C -> Interval (T_{ivl}) = 10.0 sec
0x823 -> Interval (T_{ivl}) = 15.0 sec
0xAD9 -> Interval (T_{ivl}) = 20.0 sec
0xFFF -> Interval (T_{ivl}) = 29.5 sec

WinJpLimit_M - **Maximum Allowed Window Jump**

jp_limit = T_{JP}/T_S ; Sample Frequency f_S=5.98 MHz ; T_S=0.167 µsec

Type: MultiBytes - R/W **Word Length:** 11			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
WinJpLimit2_M	0198	10-8	00
WinJpLimit1_M	0197	7-0	03

b10-b0: 0x003 -> Jump (T_{jp}) = 0.5 usec
0x01E -> Jump (T_{jp}) = 5.0 usec
0x03C -> Jump (T_{jp}) = 10.0 usec
0x05A -> Jump (T_{jp}) = 15.0 usec
0x078 -> Jump (T_{jp}) = 20.0 usec
0x168 -> Jump (T_{jp}) = 60.0 usec

JpLimitEvt_M - **Jump Limit Events Counter**

Type: SingleByte - PR **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
JpLimitEvt_M	019A	7-0	00

WinJpNoLimit_M - **Actual Requested Window Jump w/o Limit**

Actual requesteted jump of window without limit function. (See table of register adr 0x097/98).

Type: MultiBytes - R/W **Word Length:** 11			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
WinJpNoLimit2_M	019C	10-8	00
WinJpNoLimit1_M	019B	7-0	00

IQGDataOvf_M - **IQGEN LPF Overflow Counter**

Event counter of overflow bit of halfband filter in IQ generator

Type: SingleByte - PR **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
IQGDataOvf_M	01B0	7-0	00

NCODataOvf_M - **NCO Overflow Counter**

Event counter of overflow bit of NCO

Type: SingleByte - PR **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
NCODataOvf_M	01B2	7-0	00

LPFDataOvf_M - **LPF Overflow Counter**

Event counter of ‘ored’ overflow bits of halfband filters in the Low Pass Filterf

Type: SingleByte - PR **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
LPFDataOvf_M	01B4	7-0	00

IrqMask_M - **MCM Demodulator Interrupt Mask**

If the mask bits are set the corresponding interrupt is enabled, i.e. if the Irq_Status_M bit is set an external interupt is generated.

Type: SingleByte - INT **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
IrqMask_M	01C0	1-0	00

b1 : frequency unlock

b0 : frame sync unlock

IrqStatus_M - **MCM Demodulator Interrupt Status**

Bit 0 is set if the Frequency Control is enabled (cf. bit 6 of Enable_M) and the frequency lock indicator has changed from LOCK to NO LOCK (cf. bit 9 of status_M). This bit is set if the Frame Sync is enabled (cf. bit 3 of Enable_M) and the it's state has changed from SYNC to HUNT (cf. bit 3-2 of Status_M).

Type: SingleByte - INT **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
IrqStatus_M	01C1	1-0	00

b1 : frequency unlock

b0 : frame sync unlock

2.4 TDM (Section 1)

TdmEnable_S - Satellite TDM Decoding Block Enable

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TdmEnable_S	0200	7-0	FF

b7 : sat2_tfm_en enable sub-block satellite two TDM FIFO management

b6 : sat2_td_en enable sub-block satellite two TDM de-scrambling

b5 : sat2_qmg_en enable sub-block satellite two QPSK metric generation

b4 : sat2_ts_en enable sub-block satellite two TDM synchronization

b3 : sat1_tfm_en enable sub-block satellite one TDM FIFO management

b2 : sat1_td_en enable sub-block satellite one TDM de-scrambling

b1 : sat1_qmg_en enable sub-block satellite one QPSK metric generation

b0 : sat1_ts_en enable sub-block satellite one TDM synchronization

TdmSync_S1 - Satellite One TDM Decoding Synchronization Data Control T

Type: SingleByte - R/W **Word Length:** 5			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TdmSync_S1	0204	4-0	10

b4 : fsm_fallback

b3 : invert_data_out

b2 : invert_data_in

b1 : iq_swap_data_out

b0 : iq_swap_data_in

MfpLength_S1 - Sat1 TDM Decoding Extended MFP Detection Window Length

Once the MFP is found the subsequent appearance is scanned within this symmetric window around the MFP's predicted position on the soft-symbol stream.

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpLength_S1	0205	3-0	0F

MfpThr_S1 - Sat1 TDM Decoding Extended MFP Detection Threshold

Threshold of the extended MFP correlation determining extended MFP detection if reached or exceeded.

Type: SingleByte - R/W **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpThr_S1	0206	6-0	44

SyncLength_S1 - Sat1 TDM Decoding Synchronization Window Length

Number of (predicted) subsequent extended MFP positions which are evaluated to determine the status of the MFP synchronization.

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
SyncLength_S1	0207	3-0	03

PreSyncThr_S1 - Sat1 TDM Decoding Pre-Synchronization Lost Threshold

Number of undetected extended MFP's within the TDM decoding synchronization window, forcing the TDM synchronization to reenter the initial synchronization procedure searching the extended MFP on the entire soft-symbol stream. . Value 0x00 disables loss of lock.

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
PreSyncThr_S1	0208	3-0	02

SyncThr_S1 - Sat1 TDM Decoding Synchronization Lost Threshold

Number of subsequent undetected extended MFP's while being sychronized, forcing the TDM synchronization to reenter the initial synchronization procedure searching the extended MFP on the entire soft-symbol stream. (Long range drop-out condition).

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
SyncThr_S1	0209	3-0	0B

FspThr_S1 - Sat1 TDM Decoding FSP Invalid Threshold

Threshold of the FSP correlation determining an invalid FSP detection if not exceeded.

Type: SingleByte - R/W **Word Length:** 6			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FspThr_S1	020A	5-0	14

MetricCtrl_S1 - Satellite One TDM Decoding QPSK Metric Generation Data Control

Enables swap of data I- and Q-component and QPSK-map inversion if the corresponding bit is set. Determines the threshold of the Soft Decision Slicer and the applied data output format.

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MetricCtrl_S1	020B	3-0	00

b3 : mgen_map_inv

b2 : mgen_format 0 = Two's complement; 1= Offset binary

b1 : mgen_lim_thold 0-> Threshold = (64)dec; 1-> Threshold = (80)dec

b0 : mgen_iq_swap_data_in

Scrambler_S1 - Satellite One TDM Decoding Scrambler Polinomial

Type: MultiBytes - R/W **Word Length:** 12			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Scrambler2_S1	020D	11-8	08
Scrambler1_S1	020C	7-0	05

TdmSync_S2 - Satellite Two TDM Decoding Synchronization Data Control

Type: SingleByte - R/W **Word Length:** 5			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TdmSync_S2	0212	4-0	10

b4 : fsm_fallback

b3 : invert_data_out

b2 : invert_data_in

b1 : iq_swap_data_out

b0 : iq_swap_data_in

MfpLength_S2 - Sat2 TDM Decoding Extended MFP Detection Window Length

Once the MFP is found the subsequent appearance is scanned within this symmetric window around the MFP's predicted position on the soft-symbol stream.

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpLength_S2	0213	3-0	0F

MfpThr_S2 - Sat2 TDM Decoding Extended MFP Detection Threshold

Threshold of the extended MFP correlation determining extended MFP detection if reached or exceeded.

Type: SingleByte - R/W **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpThr_S2	0214	6-0	44

SyncLength_S2 - Sat2 TDM Decoding Synchronization Window Length

Number of (predicted) subsequent extended MFP positions which are evaluated to determine the status of the MFP synchronization.

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
SyncLength_S2	0215	3-0	03

PreSyncThr_S2 - Sat2 TDM Decoding Pre-Synchronization Lost Threshold

Number of undetected extended MFP's within the TDM decoding synchronization window, forcing the TDM synchronization to reenter the initial synchronization procedure searching the extended MFP on the entire soft-symbol stream. . Value 0x00 disables loss of lock.

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
PreSyncThr_S2	0216	3-0	02

SyncThr_S2 - Sat2 TDM Decoding Synchronization Lost Threshold

Number of subsequent undetected extended MFP's while being sychronized, forcing the TDM synchronization to reenter the initial synchronization procedure searching the extended MFP on the entire soft-symbol stream. (Long range drop-out condition).

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
SyncThr_S2	0217	3-0	0B

FspThr_S2 - Sat2 TDM Decoding FSP Invalid Threshold

Threshold of the FSP correlation determining an invalid FSP detection if not exceeded.

Type: SingleByte - R/W **Word Length:** 6			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FspThr_S2	0218	5-0	14

MetricCtrl_S2 - Satellite One TDM Decoding QPSK Metric Generation Data Control

Enables swap of data I- and Q-component and QPSK-map inversion if the corresponding bit is set. Determines the threshold of the Soft Decision Slicer and the applied data output format.

b3 : mgen_map_inv

b2 : mgen_format 0 = Two's complement; 1= Offset binary

b1 : mgen_lim_thold 0-> Threshold = (64)dec; 1-> Threshold = (80)dec

b0 : mgen_iq_swap_data_in

Scrambler_S2 - Satellite Two TDM Decoding Scrambler Polinomial

Type: MultiBytes - R/W **Word Length:** 12			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Scrambler2_S2	021B	11-8	08
Scrambler1_S2	021A	7-0	05

MfpLock_S1 - Satellite One TDM Decoding Status

Type: SingleByte - R **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpLock_S1	021D	6-0	--

b6-b5 : tdm_sync 00= IDLE 10= FSP RESYNC
01= XMFP HUNT 11= XMFP RESYNC

b4-b3 : tdm_dropout_align 00= IDLE 10= MEDIUM
01= SHORT 11= LONG

b2-b1 : tdm_sync_status 00= IDLE/FLUSH 10= SYNC
01= PRESYNC 10= SYNC

b0 : tdm_lock 0= UNLOCK; 1= LOCK

MfpLost_S1 - Satellite One TDM Decoding Extended MFP Counter

Number of extended MFP's not found within the synchronization window whilest presynchronized (range from 0 to the value loaded into the register PreSyncThr_S1, addr:0x0208) or subsequent not found whilest synchronized (range from 0 to the value loaded into the register SyncThr_S1, addr:0x0209).

Type: SingleByte - R **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpLost_S1	021E	3-0	--

MfpW_re_S1 - Satellite One TDM Decoding Extended MFP Correlation Weight, Real Part

Result of the latest extended MFP real part correlation.

Type: SingleByte - R **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpW_re_S1	0220	7-0	--

MfpW_im_S1 - Satellite One TDM Decoding Extended MFP Correlation Weight, Imaginary Part

Result of the latest extended MFP imaginary part correlation.

Type: SingleByte - R **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpW_im_S1	0221	7-0	--

FspW_re_S1 - Satellite One TDM Decoding FSP Correlation Weight, Real Part

Result of the latest FSP real part correlation.

Type: SingleByte - R **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FspW_re_S1	0222	6-0	--

MspW_im_S1 - Satellite One TDM Decoding FSP Correlation Weight, Imaginary Part

Result of the latest FSP imaginary part correlation.

Type: SingleByte - R **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FspW_im_S1	0223	6-0	--

FspPhase_S1 - Satellite One TDM Decoding Phase

Type: SingleByte - R **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FspPhase_S1	0224	1-0	--

b1-b0 : 00= 0° 10= 90°
01= 270° 11= 180°

MfpLock_S2 - Satellite Two TDM Decoding Status

Type: SingleByte - R **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpLock_S2	0225	6-0	--

b6-b5 :	tdm_sync		00= IDLE10= FSP RESYNC
			01= XMFP HUNT11= XMFP RESYNC
b4-b3 :	tdm_dropout_align	00= IDLE	10= MEDIUM
			01= SHORT11= LONG
b2-b1 :	tdm_sync_status	00= IDLE/FLUSH10= SYNC	
			01= PRESYNC11= UNLOCK
b0 :	tdm_lock		0= UNLOCK; 1= LOCK

MfpLost_S2 - Satellite Two TDM Decoding Extended MFP Counter

Number of extended MFP's not found within the synchronization window whilest presynchronized (range from 0 to the value loaded into the register PreSyncThr_S2, addr:0x0216) or subsequent not found whilest synchronized (range from 0 to the value loaded into the register SyncThr_S2, addr:0x0217).

Type: SingleByte - R	**Word Length:** 4		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpLost_S2	0226	3-0	--

MfpW_re_S2 - Satellite Two TDM Decoding Extended MFP Correlation Weight, Real Part

Result of the latest extended MFP real part correlation.

Type: SingleByte - R	**Word Length:** 8		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpW_re_S2	0228	7-0	--

MfpW_im_S2 - Satellite Two TDM Decoding Extended MFP Correlation Weight, Imaginary Part

Result of the latest extended MFP imaginary part correlation.

Type: SingleByte - R	**Word Length:** 8		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpW_im_S2	0229	7-0	--

FspW_re_S2 - Satellite Two TDM Decoding FSP Correlation Weight, Real Part

Result of the latest FSP real part correlation.

Type: SingleByte - R	**Word Length:** 7		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FspW_re_S2	022A	6-0	--

MspW_im_S2 - Satellite Two TDM Decoding FSP Correlation Weight, Imaginary Part

Result of the latest FSP imaginary part correlation.

Type: SingleByte - R	**Word Length:** 7		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FspW_im_S2	022B	6-0	--

FspPhase_S2 - Satellite Two TDM Decoding Phase

Type: SingleByte - R	**Word Length:** 2		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FspPhase_S2	022C	1-0	--

b1-b0 : 00= 0° 10= 90°
01= 270° 11= 180°

TdmEnable_T - Terrestrial TDM Decoding Block Enable

Type: SingleByte - R/W	**Word Length:** 5		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TdmEnable_T	022D	4-0	1F

b4 : terr_tf_en enable sub-block terrestrial TDM FIFO
b3 : terr_twc_en enable sub-block terrestrial TDM write controller
b2 : terr_td_en enable sub-block terrestrial TDM de-scrambling
b1 : terr_tt_en enable sub-block terrestrial TDM data formating
b0 : terr_ts_en enable sub-block terrestrial TDM synchronization

MfpLength_T - Terrestrial TDM Decoding MFP Detection Window Length

Once the MFP is found, the subsequent appearance is scanned within this symmetric window around the MFP perdicted position on the solf-symbol stream.

Type: SingleByte - R/W	**Word Length:** 4		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpLength_T	022E	3-0	07

MfpThrPreSync_T - Terrestrial TDM Decoding MFP Detection Threshold, Pre-Synchronization

Threshold of the MFP correlation determining MFP detection to achieve pre-synchronization if reached or exceeded.

Type: SingleByte - R/W	**Word Length:** 7		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpThrPreSync_T	022F	7-0	2C

MfpThrSync_T - Terrestrial TDM Decoding MFP Detection Threshold, Synchronization

Threshold of the MFP correlation determining MFP detection to achieve synchronization if reached or exceeded.

Type: SingleByte - R/W **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpThrSync_T	0230	7-0	28

SyncLength_T - Terrestrial TDM Synchronization Window Length

Number of (predicted) subsequent MFP positions, which are evaluated to determine the status of the MFP synchronization.

Type: SingleByte - R/W **Word Length:** 5			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
SyncLength_T	0231	4-0	03

SyncThr_T - Terrestrial TDM Synchronization Found Threshold

Number of detected MFPs within the TDM decoding synchronization window to achieve synchronization. If this number is not reached or exceeded, the TDM synchronization reenters the initial synchronization procedure searching the MFP on the entire soft-symbol stream.

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
SyncThr_T	0232	3-0	02

SyncLost_T - Terrestrial TDM Synchronization Lost Threshold

Number of subsequent undetected MFP's while being synchronized, forcing the TDM synchronization to reenter the initial synchronization procedure searching the MFP on the entire soft-symbol stream.

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
SyncLost_T	0233	3-0	0B

Scrambler_T - Terrestrial TDM Decoding Scrambler Polinomial

Type: MultiBytes - R/W **Word Length:** 12			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Scrambler2_T	0235	11-8	08
Scrambler1_T	0234	7-0	05

DataFormat_T - Terrestrial TDM Decoding Data Formatting

Enables swap of data I- and Q-component, MCM-map inversion and limiter if the corresponding bit is set. De-

termines the applied data output format. If the limiter is enabled, data with MSB = '1' is replaced by "all-ones", data with MSB = '0' is shifted left logically.

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
DataFormat_T	0236	3-0	00

b3 : map_inv
b2 : format 0= Two's complement; 1= Offset binary
b1 : limit
b0 : iq_swap

TdmStatus_T - Terrestrial TDM Decoding Status

Type: SingleByte - R **Word Length:** 3			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TdmStatus_T	0237	2-0	--

b2-b1 : tdm_sync_status 00= IDLE 10= SYNC
01= PRESYNC 11= UNLOCK
b0 : tdm_lock 0 = UNLOCK 1= LOCK

MfpLost_T - Terrestrial TDM Decoding MFP Correlation Lost

Number of MFPs found within the synchronization window whilest pre-synchronized (range from 0 to the value loaded into the register SyncLost_T, addr:0x0233).

Type: SingleByte - R **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpLost_T	0239	3-0	--

MfpW_re_T - Terrestrial TDM Decoding MFP Correlation Weight, Real Part

Result of the latest MFP real part correlation.

Type: SingleByte - R **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpW_re_T	023A	7-0	--

MfpW_im_T - Terrestrial TDM Decoding MFP Correlation Weight, Imaginary Part

Result of the latest MFP imaginary part correlation.

Type: SingleByte - R **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpW_im_T	023B	7-0	--

TdmPhase_T - Terrestrial TDM Decoding Phase

Type: SingleByte - R **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TdmPhase_T	023C	1-0	--

b1-b0 : 00= 0° 10= 90°
1= 270° 11= 180°

TdmSyncCtrl_T - Terrestrial TDM Decoding Synchronization Control

Type: SingleByte - R/W **Word Length:** 1			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TdmSyncCtrl_T	023F	0	01

b0 : fsm_fallback_en

SwfgEnable_S - Satellite Weighting Factor Generation Block Enable

Type: SingleByte - R/W **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Swfg_Enable_S	0240	7-0	FF

b7: swfg2_fsp_invalid_en enable satellite two weighting factor generation FSP invalid evalutation.Weights are forced to '0' if this bit is set to '1' and the TDM decode block detects an invalid FSP.

b6: swfg2_cycle_slip_en enable satellite two weighting factor generation cycle slip evalutation. Weights are forced to '0' if this bit is set to '1' and the TDM decode block detects a cycle slip.

b5: swfg2_fifo_en enable sub-block satellite two weighting factor FIFO

b4: swfg2_comp_en enable sub-block satellite two weighting factor calculation

b3: swfg1_fsp_invalid_en enable satellite one weighting factor generation FSP invalid evalutation.Weights are forced to '0' if this bit is set to '1' and the TDM decode block detects an invalid FSP.

b2: swfg1_cycle_slip_en enable satellite one weighting factor generation cycle slip evalutation. Weights are forced to '0' if this bit is set to '1' and the TDM decode block detects a cycle slip.

b1: swfg1_fifo_en enable sub-block satellite one weighting factor FIFO

b0: swfg1_comp_en enable sub-block satellite one weighting factor calculation

SwfgStatus_S - Satellite Weighting Factor Generation Status

Type: SingleByte - R **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
SwfgStatus_S	0241	1-0	--

b1: swfg2_status Sat2 weighting factor generation status 0=idle1=operational
b0: swfg1_status Sat1 weighting factor generation status 0=idle1=operational

Prc_En - TDM PRC Interface Block Enable

Type: SingleByte - R/W **Word Length:** 3			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Prc_En	0250	2-0	00

b2-b1: prc source 00= Satellite1 10= Terrestrial
01= Satellite2 11= RFU
b0: block_en 0= Disabled 1= Enabled

Prc_Num - PRC Number

This register sets the PRC number in the range from 1 to 258.

Type: MultiByte2 - R/W **Word Length:** 9			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Prc_Num2	0252	8	00
Prc_Num1	0251	7-0	00

DescDataEn - Signal Selection for Multiplexer After Descrambler

Select signals for multiplexer after tdm descrambling (0: original data; 1: register contents)

Type: SingleByte - R/W **Word Length:** 5			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
DescDataEn	0260	4-0	00

b4: swfg2_data_out_en
b3: swfg1_data_out_en
b2: sat2_data_out_en
b1: sat1_data_out_en
b0: terr_data_out_en

DescData_re_T - Terrestrial Test Real Data

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
DescData_re_T	0261	7-0	00

DescData_im_T - Terrestrial Test Imaginary Data

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
DescData_im_T	0262	7-0	00

DescData_re_S1 - Sat1 Test Real Data

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
DescData_re_S1	0263	3-0	00

DescData_im_S1 - Sat1 Test Imaginary Data

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
DescData_im_S1	0264	3-0	00

DescData_re_S2 - Sat2 Test Real Data

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
DescData_re_S2	0265	3-0	00

DescData_im_S2 - Sat2 Test Imaginary Data

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
DescData_im_S2	0266	3-0	00

DescData_S1wfg - Sat1 Weighting Test Data

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
DescData_S1wfg	0267	3-0	00

DescData_S2wfg - Sat2 Weighting Test Data

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
DescData_S2wfg	0268	3-0	00

TpmEnable_S - Satellite TDM Preamble Monitor Enable

Type: SingleByte - R/W **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmEnable_S	0280	1-0	00

b1: tpm2_en enable sub-block satellite two TDM preamble monitor

b0: tpm1_en enable sub-block satellite one TDM preamble monitor

TpmDataFormat_S1 - Sat1 TDM Preamble Monitor Input Data Format

Control swap of I- and Q-component and data inversion for input data. If one bit is set to '1' it's corresponding functionality is invoked.

Type: SingleByte - R/W **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmDataFormat_S1	0281	1-0	00

b1: tpm_invert_data_in

b0: tpm_iq_swap_data_in

TpmMfpThr_S1 - Sat1 TDM Preamble Monitor MFP Detection Threshold

Threshold of the MFP correlation determining MFP detection if reached or exceeded.

Type: SingleByte - R/W **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmMfpThr_S1	0282	6-0	28

TpmFspThr_S1 - Sat1 TDM Preamble Monitor FSP Detection Threshold

Threshold of the FSP correlation determining FSP detection if reached or exceeded.

Type: SingleByte - R/W **Word Length:** 6			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmFspThr_S1	0283	5-0	14

TpmDataFormat_S2 - Sat2 TDM Preamble Monitor Input Data Format

Control swap of I- and Q-component and data inversion for input data. If one bit is set to '1' it's corresponding

functionality is invoked.

Type: SingleByte - R/W **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmDataFormat_S2	0284	1-0	00

b1: tpm_invert_data_in

b0: tpm_iq_swap_data_in

TpmMfpThr_S2 - Sat2 TDM Preamble Monitor MFP Detection Threshold

Threshold of the MFP correlation determining MFP detection if reached or exceeded.

Type: SingleByte - R/W **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmMfpThr_S2	0285	6-0	28

TpmFspThr_S2 - Sat2 TDM Preamble Monitor FSP Detection Threshold

Threshold of the FSP correlation determining FSP detection if reached or exceeded.

Type: SingleByte - R/W **Word Length:** 6			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmFspThr_S2	0286	5-0	14

TpmMfpW_re_S1 - Sat1 TDM Preamble Monitor MFP Correlation Weight, Real Part

Result of the latest MFP real part correlation.

Type: SingleByte - R **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmMfpW_re_S1	0290	7-0	--

TpmMfpW_im_S1 - Sat1 TDM Preamble Monitor MFP Correlation Weight, Imaginary Part

Result of the latest MFP imaginary part correlation.

Type: SingleByte - R **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmMfpW_im_S1	0291	7-0	--

TpmMfpSymSlip_S1 - Sat1 TDM Preamble Monitor MFP Symbol Slip

Type: MultiBytes - R **Word Length:** 12			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmMfpSymSlip2_S1	0293	11-8	--
TpmMfpSymSlip1_S1	0292	7-0	--

TpmFspW_re_S1 - Sat1 TDM Preamble Monitor FSP Correlation Weight, Real Part

Result of the latest FSP real part correlation.

Type: SingleByte - R **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmFspW_re_S1	0294	6-0	--

TpmFspW_im_S1 - Sat1 TDM Preamble Monitor FSP Correlation Weight, Imaginary Part

Result of the latest FSP imaginary part correlation.

Type: SingleByte - R **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmFspW_im_S1	0295	6-0	--

TpmFspPosSlip_S1 - Sat1 TDM Preamble Monitor FSP Position Slip

Type: MultiBytes - R **Word Length:** 12			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmFspPosSlip2_S1	0297	11-8	--
TpmFspPosSlip1_S1	0296	7-0	--

TpmFspTdmPhase_S1 - Sat1 TDM Preamble Monitor FSP Phase

Phase of the TDM soft-symbol stream basing the result on the lastest FSP correlation.

Type: SingleByte - R **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmFspTdmPhase_S1	0298	1-0	--

b1-b0 : 00= 0°10= 90°

01= 270°11= 180°

TpmPrDetect_S1 - Sat1 TDM Preamble Monitor Preamble Detection

Preamble detection based on the result of the latest preamble correlation.

Type: SingleByte - R **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmPrDetect_S1	0299	1-0	--

TpmFspCySlipCnt_S1 - Sat1 TDM Preamble Monitor FSP Cycle Slip Counter

Cycle slip counter based on FSP evaluation whilst FSP detected for the latest TDM frame.

Type: SingleByte - R **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmFspCySlipCnt_S1	029A	7-0	--

TpmFspPoSlipCnt_S1 - Sat1 TDM Preamble Monitor FSP Position Slip Counter

FSP position slip counter based on the distorsion of the detected FSPs to their expected position with respect to the lastest detected MFP.

Type: SingleByte - R	**Word Length:** 8		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmFspPoSlipCnt_S1	029B	7-0	--

TpmMfpW_re_S2 - Sat2 TDM Preamble Monitor MFP Correlation Weight, Real Part

Result of the latest MFP real part correlation.

Type: SingleByte - R	**Word Length:** 8		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmMfpW_re_S2	02A0	7-0	--

TpmMfpW_im_S2 - Sat2 TDM Preamble Monitor MFP Correlation Weight, Imaginary Part

Result of the latest MFP imaginary part correlation.

Type: SingleByte - R	**Word Length:** 8		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmMfpW_im_S2	02A1	7-0	--

TpmMfpSymSlip_S2 - Sat2 TDM Preamble Monitor MFP Symbol Slip

Type: MultiBytes - R	**Word Length:** 12		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmMfpSymSlip2_S2	02A3	11-8	--
TpmMfpSymSlip1_S2	02A2	7-0	--

TpmFspW_re_S2- Sat2 TDM Preamble Monitor FSP Correlation Weight, Real Part

Result of the latest FSP real part correlation.

Type: SingleByte - R	**Word Length:** 7		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmFspW_re_S2	02A4	6-0	--

TpmFspW_im_S2- Sat2 TDM Preamble Monitor FSP Correlation Weight, Imaginary Part

Result of the latest FSP imaginary part correlation.

Type: SingleByte - R	**Word Length:** 7		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmFspW_im_S2	02A5	6-0	--

TpmFspPosSlip_S2 - Sat2 TDM Preamble Monitor FSP Position Slip

Type: MultiBytes - R	**Word Length:** 12		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmFspPosSlip2_S2	02A7	11-8	--
TpmFspPosSlip1_S2	02A6	7-0	--

TpmFspTdmPhase_S2 - Sat2 TDM Preamble Monitor FSP Phase

Phase of the TDM soft-symbol stream basing the result on the lastest FSP correlation.

Type: SingleByte - R	**Word Length:** 2		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmFspTdmPhase_S2	02A8	1-0	--

b1-b0 : 00= 0° 10= 90°
01= 270° 11= 180°

TpmPrDetect_S2 - Sat2 TDM Preamble Monitor Preamble Detection

Preamble detection based on the result of the latest preamble correlation.

Type: SingleByte - R	**Word Length:** 2		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmPrDetect_S2	02A9	1-0	--

TpmFspCySlipCnt_S2 - Sat2 TDM Preamble Monitor FSP Cycle Slip Counter

Cycle slip counter based on FSP evaluation whilst FSP detected for the latest TDM frame.

Type: SingleByte - R	**Word Length:** 8		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmFspCySlipCnt_S2	02AA	7-0	--

TpmFspPoSlipCnt_S2 - Sat2 TDM Preamble Monitor FSP Position Slip Counter

FSP position slip counter based on the distorsion of the detected FSPs to their expected position with respect to the lastest detected MFP.

Type: SingleByte - R	**Word Length:** 8		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmFspPoSlipCnt_S2	02AB	7-0	--

TpmSySlip_S1 - Sat1 TDM Decoding Symbol Slip

Extended MFP detection based symbol slip.

Type: MultiBytes - R	**Word Length:** 12		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmSySlip2_S1	02B1	11-8	--
TpmSySlip1_S1	02B0	7-0	--

TpmSySlip_S2 - Sat2 TDM Decoding Symbol Slip

Extended MFP detection based symbol slip.

Type: MultiBytes - R	**Word Length:** 12		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmSySlip2_S2	02B3	11-8	--
TpmSySlip1_S2	02B2	7-0	--

TpmSySlip_T - Terrestrial TDM Decoding Symbol Slip

Type: MultiBytes - R	**Word Length:** 10		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TpmSySlip2_T	02B5	9-8	--
TpmSySlip1_T	02B4	7-0	--

FspStartWinLen_S1 - Sat1 TDM Decoding FSP Detection Start Window Length

Entering a short range dropout condition, the FSP is searched within a symetrical (start) window around the nominal FSP position.

Type: SingleByte - R/W	**Word Length:** 3		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FspStartWinLen_S1	02C0	2-0	02

FspHuntWinInc_S1 - Sat1 TDM Decoding FSP Detection Hunt Window Increment

Entering a medium range dropout condition, the FSP is searched within a symetrical window around the nominal FSP position. This window is increased on FSP period bases with an increment of inc/8 symbols begining with the start window length.

Type: SingleByte - R/W	**Word Length:** 4		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FspHuntWinInc_S1	02C1	3-0	03

FspShDropOutLen_S1 - Sat1 TDM Decoding FSP Short DropOut Length

Number of subsequent undetected FSPs determining the upper limit of a short range dropout condition.

Type: SingleByte - R/W **Word Length:** 5			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FspShDropOutLen_S1	02C2	4-0	0F

FspSecuAlignThr_S1 - Sat1 TDM Decoding FSP Secure Alignment Threshold

Number of subsequent detected FSPs with nominal FSP period length determining secure alignment to the TDM soft-symbol stream within a medium range dropout condition.

Type: SingleByte - R/W **Word Length:** 3			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FspSecuAlignThr_S1	02C3	2-0	03

FspStartWinLen_S2 - Sat2 TDM Decoding FSP Detection Start Window Length

Entering a short range dropout condition, the FSP is searched within a symetrical (start) window around the nominal FSP position.

Type: SingleByte - R/W **Word Length:** 3			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FspStartWinLen_S2	02C8	2-0	02

FspHuntWinInc_S2 - Sat2 TDM Decoding FSP Detection Hunt Window Increment

Entering a medium range dropout condition, the FSP is searched within a symetrical window around the nominal FSP position. This window is increased on FSP period bases with an increment of inc/8 symbols begining with the start window length.

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FspHuntWinInc_S2	02C9	3-0	03

FspShDropOutLen_S2 - Sat2 TDM Decoding FSP Short DropOut Length

Number of subsequent undetected FSPs determining the upper limit of a short range dropout condition.

Type: SingleByte - R/W **Word Length:** 5			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FspShDropOutLen_S2	02CA	4-0	0F

FspSecuAlignThr_S2 - Sat2 TDM Decoding FSP Secure Alignment Threshold

Number of subsequent detected FSPs with nominal FSP period length determining secure alignment to the

TDM soft-symbol stream within a medium range dropout condition.

Type: SingleByte - R/W **Word Length:** 3			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FspSecuAlignThr_S2	02CB	2-0	03

2.5 FEC

Control_F - **FEC Control Register**

The control flags enable the corresponding operation if set, otherwise the operation is disabled. The flags fec_en and fec_prep enable the operation of the FEC and FEC Preprocessing. Weighting of the two satellite data streams is performed only when wgt_en=1, otherwise the data from the memory are not weighted. The flags terr_format and sat_format determine the Viterbi input data format for both terrestrial and satellite data streams. As only one Viterbi Decoder is applied both flags have to be equal. The Viterbi flush operation is enabled at the end of a PRC packet when vd_flush_on=1.

Type: SingleByte - R/W **Word Length:** 6			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Control_F	0300	5-0	3F

b5 : vd_flush_on ‘0’= VD flush disabled
‘1’= VD flush enabled

b4 : sat_format ‘0’= satellite data in two’s complement (Viterbi input)
‘1’= satellite data in offset binary (Viterbi input)

b3 : terr_format ‘0’= terrstrial data in two’s complement (Viterbi input)
‘1’= terrestrial data in offset binary (Viterbi input)

b2 : wgt_en ‘0’= Satellite Weighting disabled
‘1’= Satellite Weighting enabled

b1 : fec_prep_en ‘0’= FEC Preprocessing disabled
‘1’= FEC Preprocessing enabled

b0 : fec_en ‘0’= FEC disabled
‘1’= FEC enabled

Status_F - **FEC Status Register**

The status vector comprises the status flags of the sub-modules of the FEC Processing. An inactive module is indicated by status=0, an active module by status=1

Type: SingleByte - R **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Status_F	0301	3-0	--

b3 : FEC Preprocessing ‘0’= FEC Preprocessing inactive

		‘1’= FEC Preprocessing operational
b2 :	RS Input Control	‘0’= RS Input Control inactive
		‘1’= RS Input Control operational
b1 :	Viterbi Decoder	‘0’= VD inactive
		‘1’= VD operational
b0 :	FEC Management	‘0’= FEC Management inactive
		‘1’= FEC Management operational

ErrorCtrl_F - **FEC Error Register**

Type: SingleByte - R/W **Word Length:** 6			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
ErrorCtrl_F	0302	5-0	01

b5-b0 : 0x00 -> Asynchronous status overwrite for each PRC proceed
0x01 -> Update FEC error registers with TSCC1 status only
0x02 -> Update FEC error registers with TSCC2 status only
0x03 -> Update FEC error registers with 1st PRC packet after TSCCs
...
0x32 -> Update FEC error registers with 48th PRC packet after TSCCs
x33-0x3F -> Undefined

InitState_F - **Convolutional Decoder Initial State Control Register**

Initial state of convolutional decoder after training sequence, which corresponds to the reverse of the last 6 bits of the PRC preamble 1D(hex)=00011101 -> 101110 = 2E(hex)=46(dec).

Type: SingleByte - R/W **Word Length:** 6			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
InitState_F	0307	5-0	2E

InitLfsr_F - **Viterbi Decoder LFSR Initial State**

Type: MultiBytes - R/W **Word Length:** 12			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
InitLfsr2_F	0309	11-8	0C
InitLfsr1_F	0308	7-0	CC

InitTerm_F - Termination Sequence After Flush Operation

Sequence after flush operation for termination of Viterbi decoder. The upper 8 bits have to be the PRC preamble 1D(hex) in ascending order (b12..b19).

Type: MultiBytes - R/W **Word Length:** 20			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
InitTerm3_F	030C	19-16	0B
InitTerm2_F	030B	15-8	80
InitTerm1_F	030A	7-0	00

VitBerCtrl_F - Viterbi BER Measurements Control

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
VitBerCtrl_F	0310	3-0	0F

b3 : fvd_csat_ber_mode '0'= Sat. measurment as single acquisition
'1'= Sat. measurement as continuous acquisition

b2 : fvd_csat_ber_en '0'= Sat. BER measurement disabled
'1'= Sat BER measurement enabled

b1 : fvd_terr_ber_mode '0'= Terr. measurment as single acquisition
'1'= Terr. measurement as continuous acquisition

b0 : fvd_terr_ber_en '0'= Terr. BER measurement disabled
'1'= Terr. BER measurement enabled

TerrBer_F - Terrestrial Channel Bit Error Rate

The terrestrial channel error rate states the number of channel symbol errors which where determined within one PRC packet by reencoding of the Viterbi-decoded terrestrial data stream. A new measurement is indicated by the signal terr_ber_done which is comprised in the interrupt vector (addr. 0x0350)

Type: MultiBytes - R **Word Length:** 12			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TerrBer2_F	0321	11-8	--
TerrBer1_F	0320	7-0	--

Sat1Ber_F - Satellite 1 Channel Bit Error Rate

The Sat1 channel error rate states the number of channel symbol errors which where determined within one PRC packet by reencoding of the Viterbi-decoded Sat1 data stream. A new measurement is indicated by the

signal sat1_ber_done which is comprised in the interrupt vector (addr. 0x0350)

Type: MultiBytes - R **Word Length:** 12			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Sat1Ber2_F	0325	11-8	--
Sat1Ber1_F	0324	7-0	--

Sat2Ber_F - **Satellite 2 Channel Bit Error Rate**

The Sat2 channel error rate states the number of channel symbol errors which where determined within one PRC packet by reencoding of the Viterbi-decoded Sat2 data stream. A new measurement is indicated by the signal sat2_ber_done which is comprised in the interrupt vector (addr. 0x0350)

Type: MultiBytes - R **Word Length:** 12			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Sat2Ber2_F	0329	11-8	--
Sat2Ber1_F	0328	7-0	--

ForceCorr_F - **FEC Control Register**

This Register is used to force the correction value for PRC preamble (System value 0x1D) at RS input

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
ForceCorr_F	0330	7-0	1D

RS_Ctrl_F - **RS Decoder Configuration**

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
RS_Ctrl_F	0331	3-0	03

b3-b2 : RS Error count conf ‘00’= Count 16 RS Blocks (8 PRCs);
‘01’= Count 64 RS Blocks (32 PRCs);
‘10’= Count 256 RS Blocks (128 PRCs);
‘11’= Count 1024 RS Blocks (512 PRCs).

b1 : terr_csat_comb ‘1’= Enable Terrestrial-Satellite Combining
‘0’= Disable Terrestrial-Satellite Combining

b0 : force_corr_en ‘1’= enable forced correction of PRC preamble;
‘0’= disable forced correction of PRC preamble

RS_Cnt_F - **RS Decoder Error Count Control**

This register controls the RS Error Counter. After reset the counter is disabled. To start BER measurement a value must be written in this register. When written, this register generates a one clock cycle trigger signal for

the RS Error Counter.

Type: SingleByte - WRT **Word Length:** 1			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
RS_Cnt_F	0332	0	01

b0 : Error counter control '0'= Continuos acquisition;
'1'= Single acquisition.

RS_ByteCnt_F - **RS Byte Corrected Error Counter**

This register is 14 bits long and is divided into two bytes. The LSB byte is named RS _ByteCnt1, the MSB byte is named RS_ByteCnt2. It cointains the number of the corrected RS bytes with unsigned format.

Type: MultiBytes - R **Word Length:** 14			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
RS_ByteCnt2_F	0336	13-8	--
RS_ByteCnt1_F	0335	7-0	--

RS_FrameCnt_F - **Corrupted RS Block Counter**

This register is 10 bits long and is divided into two bytes. The LSB byte is named RS _FrameCnt1, the MSB byte is named RS _FrameCnt2. It cointains the number of the corrupted RS blocks with unsigned format.

Type: MultiBytes - R **Word Length:** 10			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
RS_FrameCnt2_F	0338	9-8	--
RS_FrameCnt1_F	0337	7-0	--

InitSeq_F - **Viterbi Decoder Initialization Sequence**

The Viterbi decoder is initialized with the PRC preamble (hex 1D)

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
InitSeq_F	0340	7-0	1D

RS1_TerrByteErr_F - **Terrestrial RS Block1 Error Register**

Type: SingleByte - R **Word Length:** 5			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
RS1_TerrByteErr_F	0342	4-0	--

b4-b0 : 0x00 -> No Errors

0x01 -> 1 byte error corrected
0x02 -> 2 byte errors corrected
...
0x10 -> 16 byte errors corrected
0x1F -> Uncorrectable errors

RS2_TerrByteErr_F - **Terrestrial RS Block2 Error Register**

Type: SingleByte - R **Word Length:** 5			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
RS2_TerrByteErr_F	0343	4-0	--

b4-b0 : 0x00 -> No Errors
0x01 -> 1 byte error corrected
0x02 -> 2 byte errors corrected
...
0x10 -> 16 byte errors corrected
0x1F -> Uncorrectable errors

RS1_SatByteErr_F - **Satellite RS Block1 Error Register**

Type: SingleByte - R **Word Length:** 5			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
RS1_SatByteErr_F	0344	4-0	--

b4-b0 : 0x00 -> No Errors
0x01 -> 1 byte error corrected
0x02 -> 2 byte errors corrected
...
0x10 -> 16 byte errors corrected
0x1F -> Uncorrectable errors

RS2_SatByteErr_F - **Satellite RS Block2 Error Register**

Type: SingleByte - R **Word Length:** 5			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
RS2_SatByteErr_F	0345	4-0	--

b4-b0 : 0x00 -> No Errors
0x01 -> 1 byte error corrected
0x02 -> 2 byte errors corrected

...
0x10 -> 16 byte errors corrected
0x1F -> Uncorrectable errors

RS_Block_decis_F - **Status of the Last RS Diversity Decision**

Type: SingleByte - R **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
RS_Status_decis_F	0346	1-0	--

b1-b0 : 00 = Satellite Path selected for current frame
01 = Terrestrial Path selected for current frame
10 = Undefined
01 = Undefined

IrqMask_F - **FEC Interrupt Mask**

This register masks the interrupt request when a '0' is written in the relative bit.

Type: SingleByte - INT **Word Length:** 5			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
IrqMask_F	0350	4-0	00

b4 : interrupt mask for rs_cnt_end
b3 : interrupt mask for sat2_ber_done
b2 : interrupt mask for sat1_ber_done
b1 : interrupt mask for terr_ber_done
b0 : interrupt mask for fec_irq_status

IrqStatus_F - **FEC Interrupt Status**

This is the interrupt status vector. When a bit means that an interrupt is requested by the corresponding block. To reset a single bit, a '0' must be written into. '0x00' resets the complete vector.

Type: SingleByte - INT **Word Length:** 5			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
IrqStatus_F	0351	4-0	00

b4 : rs_cnt_end interrupt for new RS error count measurement
b3 : sat2_ber_done interrupt for new Sat2 BER measurement sat2_ber
b2 : sat1_ber_done interrupt for new Sat1 BER measurement sat1_ber
b1 : terr_ber_done interrupt for new terr. BER measurement terr_ber
b0 : fec_irq_status interrupt signal from FEC Management

2.6 IF Sampling and Control Interface

AGC_CTRL1 - AGC Control Register #1

This register controls Terrestrial and satellite AGC loop gain and the sense of the TAGC and SAGC control pins.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
AGC_CTRL1	0400	7-0	88

b7: TAGCCHS Terrestrial AGC Loop Change Sign
b6-b4: TAGCBETA(2:0) Terrestrial AGC Loop Gain.
b3: SAGCCHS Satellite AGC Loop Change Sign
b2-b0: SAGCBETA(2:0) Satellite AGC Loop Gain.

TAGCBETA and SAGCBETA Gain Table:

TAGCBETA/ SAGCBETA	**Loop Gain**
000	2**0 = 1
001	2**1 = 2
010	2**2 = 3
011	2**3 = 4
100	2**4 = 16
101	2**5 = 32
110	2**6 = 64
111	Open Loop

SAGCREF - Satellite AGC Reference Level

This register is 13 bits long and is divided into two bytes. The LSB byte is named SAGCREF0, the MSB byte is named SAGCREF1. It sets the signal level at the Satellite ADC input.

Type: MultiBytes - R/W **Word Length:** 13			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
SAGCREF1	0402	12-8	01
SAGCREF0	0401	7-0	90

SAGCINTG - Satellite AGC Integrator

This register is connected to the 8MSB of the internal integrator of the satellite AGC loop. It gives an image of the power level at the satellite analog input. The register format is two's complement.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
SAGCINTG	0403	7-0	00

TAGCREF - **Terrestrial AGC Reference Level**

This register is 13 bits long and is divided into two bytes. The LSB byte is named TAGCREF0, the MSB byte is named TAGCREF1. It sets the signal level at the terrestrial ADC input.

Type: MultiBytes - R/W **Word Length:** 13			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TAGCREF1	0405	12-8	01
TAGCREF0	0404	7-0	90

TAGCINTG - **Terrestrial AGC Integrator**

This register is connected to the 8MSB of the internal integrator of the terrestrial AGC loop. It gives an image of the power level at the terrestrial analog input. The register format is two's complement.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TAGCINTG	0406	7-0	00

IF_CTRL - **IF Sampling Control Register**

This register selects the external ADC format and controls the average filter of the AGC integrator.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
IF_CTRL	0407	7-0	00

b7: AVG_OFF Internal averager circuit disable. '1'=Averager disabled; '0'=Averager enabled.

b6-b2: Reserved for Future Use

b1 : FORMAT External/Internal ADC code format. '1'=Two's complement; '0'=Offset Binary.

b0: Reserved

SELTSTOUT - **Internal Test Bus Selection for each Block**

This register selects, for each internal blocks, which signals are connected to the FTESTOUT pins. It must ve used together with the TSTMUXCTL register (addr 0x040B).

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
SELTSTOUT	040A	3-0	00

b3-b0: TBD

TSTMUXCTL - **Selection of the Internal Block for Functional Test**

This register selects, among 16 test buses from the internal functional blocks, the one to be connected to the FTESTOUT bus according with the table below. It must ve used together with the SELTSTOUT register (addr

0x040A).

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TSTMUXCTL	040B	3-0	00

b3-b0: 0000 Reserved
0001 Reserved
0010 Reserved for Future Use
0011 Reserved for Future Use
0100 Reserved for Future Use
0101 PC Bitstream Interface #2
0110 PC Bitstream Interface #1
0111 FEC_RS (Reed-Solomon decoder)
1000 FEC_FPP (FEC Pre-Processing)
1001 FEC_VD
1010 TDM
1011 Reserved for Future Use
1100 Terrestrial Demodulator (MCM demodulator)
1101 Satellite Demodulator #2 (QPSK2)
1110 Satellite Demodulator #1 (QPSK1)
1111 IF Sampling

CLKDIV_CONF - Master Clock Programmable Divider

This register sets the division factor (2,4 or 8) of the master clock applied to XTI/MCLK input. The divided clock is available at CLKD output (pin 56).

Type: SingleByte - R/W **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
CLKDIV_CONF	040C	1-0	03

b1- b0 : CLK_DIV 00 = MCLK/2 (CLKD frequency = 23.92MHz/2=11.96MHz)
01 = MCLK/4 (CLKD frequency = 23.92MHz/2=11.96MHz)
10 = MCLK/8 (CLKD frequency = 23.92MHz/2=11.96MHz)
11 = Disabled (CLKD fixed to GND)

QPSK_BER_CTRL - Satellite Demodulators BER Control

This register is used in functional test mode for B.E.R. Measurement after satellite demodulation, using an external serial BER Tester. The BER measurement is on the hard decided output symbol and the relative clock available at the FTESTOUT interface (see SELTSTOUT Register description).

This register controls the interface operations to synchronize the BER Tester on the demodulated satellite sym-

bols before starting the BER computation.

Type: SingleByte - R/W **Word Length:** 3			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
QPSK_BER_CTRL	040D	2-0	00

b2: IQ SWAP Swap between I and Q components of the received symbols

b1-**b0**: PHCHG Phase ambiguity correction

00 = 0 degrees

01 = 90 degrees

10 = 180 degrees

11 = 270 degrees

CONTROL - **General Purpose Control Register**

This register controls the master clock outputs, the bidirectional buses mode to access the external memory and the BIST access mode (reserved for structural test).

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
CONTROL	0410	7-0	00

b7: MCLKO_OFF MCLKO output buffer disable.

0 = Buffer active;

1 = Buffer disabled (output fixed to ground).

b6: MCLKON_OFF MCLKON output buffer disable.

0 = Buffer active;

1 = Buffer disabled (output fixed to ground).

b5: MDQM_CTRL External memory input/output mask polarity.

0 = High level active;

1 = Low level active.

b4-b1: Reserved

b0: IRQ_RST_CTRL Reset after read on the interrupt register (IRQ1_STATUS)

0 = Disabled;

1 = Enabled.

IRQ1_MASK - Interrupt Mask Register

Enable/Disable interrupts on INTR pin.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
IRQ1_MASK	0417	7-0	00

b7: Sat2 Lock indicator interrupt masked 0=disabled; 1=enabled.
b6: Sat1 Lock indicator interrupt masked 0=disabled; 1=enabled.
b5: MFP_CLK interrupt masked (5 msec impulse sync) 0=disabled; 1=enabled.
b4: MFP_CLK interrupt masked (level) 0=disabled; 1=enabled.
b3: IIC-bus illegal address masked 0=disabled; 1=enabled.
b2: TDM interrupt masked 0=disabled; 1=enabled.
b1: FEC interrupt masked 0=disabled; 1=enabled.
b0: MCM interrupt masked 0=disabled; 1=enabled.

Note: bit5 and bit4 cannot be used togheter, i.e. if bit5 is used the bit4 must be masked and viceversa. If both are enabled, bit4 will be sent to INTR pin.

IRQ1_STATUS - Interrupt Status Register

This register represents the interrupt vector when the INTR pin is activated (HIGH level active). It can be reset after read if the bit0 (IRQ_RST_CTRL) of the CONTROL register is set to '1' or a single bit can be reset directly writing '0'.

Type: SingleByte - PR **Word Length:** 8

Byte Name	Address (Hex)	Bit Map	Reset Value (Hex)
IRQ1_STATUS	0419	7-0	00

b7: Interrupt request from Sat2 lock indicator (high active);
b6: Interrupt request from Sat1 lock indicator (high active);
b5: Interrupt request from MFP_CLK (5 msec impulse continuos sync signal);
Bit5 is generated from the MFP_CLK and is a 432msec period signal with ~1.16% duty-cycle (5msec/432msec); there is no need to reset bit5 by the interrupt routine.
b4: Interrupt request from MFP_CLK (high active).
Bit4 is activated by the positive edge of the MFP_CLK and is a high level signal; the interrupt routing must reset this bit.
b3: Interrupt request from IIC-bus illegal address (high active);
b2: Interrupt request from TDM (high active);
b1: Interrupt request from FEC (high active);
b0: Interrupt request from MCM (high active).

STATUS1 - CDEC Status Register

This register represents the interrupt vector when the INTR pin is activated (HIGH level active). It can be reset after read if the bit0 (IRQ_RST_CTRL) of the CONTROL register is set to '1' or a single bit can be reset directly writing '0'.

Type: SingleByte - R **Word Length:** 8

Byte Name	Address (Hex)	Bit Map	Reset Value (Hex)
STATUS1	041F	7-0	--

b7-b4: Reserved for Future Use

b4: Terrestrial Demodulator lock indicator
0 = locked
1 = unlocked

b3: Satellite #2 lock indicator
0 = locked
1 = unlocked

b2: Satellite #1 lock indicator
0 = locked
1 = unlocked

b1: FEC terrestrial-satellite combining decision for RS block #2
0 = satellite;
1 = terrestrial;

b0: FEC terrestrial-satellite combining decision for RS block #1
0 = satellite;
1 = terrestrial;

2.7 PC Bitstream Interface

PCDC_CONF_0 - **Clock Configuration for PC Interface #0**

Type: SingleByte - R/W **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
PCDC_CONF_0	0500	6-0	00

b6-b2: PCDC_DIVVALUE_0 Master clock divider. The master clock is divided by (PCDC_DIVVALUE_0+1)*2.

b1: PCDC_NEG_0 1=PCDC0 is inverted.

b0: PCDC_RUNFREE_0 0=Clock running only when data is sent out; 1=Clock always running.

PCDC_CONF_1 - **Clock Configuration for PC Interface #1**

Type: SingleByte - R/W **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
PCDC_CONF_1	0501	6-0	00

b6-b2: PCDC_DIVVALUE_1 Master clock divider. The master clock is divided by (PCDC_DIVVALUE_1+1)*2.

b1: PCDC_NEG_11=PCDC0 is inverted.

b0: PCDC_RUNFREE_10=Clock running only when data is sent out; 1=Clock always running.

PCSD_CONF_0 - **Data Configuration for PC Interface #0**

Type: SingleByte - R/W **Word Length:** 6			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
PCSD_CONF_0	0502	5-0	00

b5-b4: PCSD_FFLAGMODE_0
00=Frame flag bit is always set to '0';
01=Frame flag bit is set to '1' only for the first byte of TSCC1;
10=Frame flag bit is set to '1' for the first byte of all PRCs;

11=Frame flag bit is set to '1' for the first byte of all PRCs.

b3: PCSD_FRAMEFLAG_0 1=Frame flag bit is appended to each data byte

b2: PCSD_ODDPARITY_0 0=Even parity bit is generated; 1=Odd parity bit is generated.

b1: PCSD_ADDPARITY_0 1=Parity bit is appended to each data.

b0: PCSD_LSBFIRST_0 0=Parallel data sent out MSB first; 1=Parallel data sent out LSB first.

PCSD_CONF_1 - **Data Configuration for PC interface #1**

Type: SingleByte - R/W **Word Length:** 6			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
PCSD_CONF_1	0503	5-0	00

b5-b4: PCSD_FFLAGMODE_1 00=Frame flag bit is always set to '0';
01=Frame flag bit is set to '1' only for the first byte of TSCC1;
10=Frame flag bit is set to '1' for the first byte of all PRCs;
11=Frame flag bit is set to '1' for the first byte of all PRCs.

b3: PCSD_FRAMEFLAG_1 1=Frame flag bit is appended to each data byte.

b2: PCSD_ODDPARITY_1 0=Even parity bit is generated; 1=Odd parity bit is generated.

b1: PCSD_ADDPARITY_1 1=Parity bit is appended to each data.

b0: PCSD_LSBFIRST_1 0=Parallel data sent out MSB first; 1=Parallel data sent out LSB first.

PCSYNC_CONF - Synchronization Signals Configuration for both Interfaces

Type: SingleByte - R/W **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
PCSYNC_CONF	0504	7-0	77

b7: PCTS_EF_SWITCH_1 0=PCTS_EF1 pin send out the TDM frame synchronization.
1=PCTS_EF1 pin send out the PC Interface output error flag.

b6: PCTS_SYNCH_1 0=PCTS1 set to '1' with first bit of TSCC1
1=PCTS1 set to '1' one PCDC cycle before the first bit of TSCC.

b5: PCFS_SYNCH_1 0=PCFS1 set to '1' with first bit of each PRC.
1=PCFS1 set to '1' one PCDC cycle before the first bit of PRC.

b4: PCBS_SYNCH_1 0=PCBS1 set to '1' with the first bit of each byte.
1=PCBS1 set to '1' one PCDC cycle before the first bit of byte.

b3: PCTS_EF_SWITCH_0 0=PCTS_EF0 pin send out the TDM frame synchronization.
1=PCTS_EF0 pin send out the PC Interface output error flag.

b2: PCTS_SYNCH_0 0=PCTS0 set to '1' with first bit of TSCC1
1=PCTS0 set to '1' one PCDC cycle before the first bit of TSCC.

b1: PCFS_SYNCH_0 0=PCFS0 set to '1' with first bit of each PRC.

1=PCFS0 set to ‘1’ one PCDC cycle before the first bit of PRC.

b0: PCBS_SYNCH_0 0=PCBS0 set to ‘1’ with the first bit of each byte.

1=PCBS0 set to ‘1’ one PCDC cycle before the first bit of byte.

PC_ALARM - **Alarm Signal for Interface #0 and #1**

Type: SingleByte - R/W **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
PC_ALARM	0506	1-0	00

b1: PC_ALARM_1 1=Data trasmission error in the interface #1; 0=Interface #1 operating properly.

b0: PC_ALARM_0 1=Data trasmission error in the interface #0; 0=Interface #0 operating properly.

Note: These bits are automatically set to ‘0’ after read.

2.8 TDM (Section 2)

DeltaRefCyc_M - Delta Reference Cycles for MCM Frame Sync

Given in samples and per MCM-frame.

Format: siii,fffffffff with s=sign; i=integer part; f=fractional part

Type: MultiBytes - R	**Word Length:** 13		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
DeltaRefCyc2_M	0611	12-8	--
DeltaRefCyc1_M	0610	7-0	--

MfpSyncMax_S1 - Sat1 MFP Sync Rightmost Distance

Sets the rightmost distance of sat1 MFP sync to the point, when the frame is read. The initial value corresponds to a time of 12ms.

Type: SingleByte - R/W	**Word Length:** 8		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpSyncMax_S1	0620	7-0	46

MfpSyncMin_S1 - Sat1 MFP Sync Leftmost Distance

Sets the leftmost distance of sat1 MFP sync to the point, when the frame is read. The initial value corresponds to a time of 8ms.

Type: SingleByte - R/W	**Word Length:** 8		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpSyncMin_S1	0621	7-0	2F

MfpSyncMax_S2 - Sat2 MFP Sync Rightmost Distance

Sets the rightmost distance of sat1 MFP sync to the point, when the frame is read. The initial value corresponds to a time of 12ms.

Type: SingleByte - R/W	**Word Length:** 8		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpSyncMax_S2	0622	7-0	46

MfpSyncMin_S2 - Sat2 MFP Sync Leftmost Distance

Sets the leftmost distance of sat1 MFP sync to the point, when the frame is read. The initial value corresponds to a time of 8ms.

Type: SingleByte - R/W	**Word Length:** 8		
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpSyncMin_S2	0623	7-0	2F

MfpSyncMax_T - Terrestrial MFP Sync Rightmost Distance

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpSyncMax_T	0624	7-0	11

MfpSyncMin_T - Terrestrial MFP Sync Leftmost Distance

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MfpSyncMin_T	0625	7-0	29

Xmem_Type - External Memory Device Type

Type: SingleByte - R/W **Word Length:** 1			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Xmem_Type	0630	0	00

b0: 0= 64 Mbit memory 1= 128Mbit memory

XmemRefCyc - External Memory Refresh Cycle Period

Type: MultiBytes - R/W **Word Length:** 9			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
XmemRefCyc2	0632	8	01
XmemRefCyc1	0631	7-0	75

XmemMode - External Memory Management Mode

Type: SingleByte - R/W **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
XmemMode	0634	1-0	00

b1-b0: 00= Normal 10= Unused
01= Memory Dump 11= Self Test

XmemStatus - External Memory Management Status

TDM external memory management self test error status

Type: SingleByte - R **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
XmemStatus	0635	1-0	--

b1-b0: 00= No Error 10= Unused
01= Memory error, 1st test sequence 11= Memory error, 2nd test sequence

XmemStErrAdr - External Memory Management Self-Test Error Address

TDM external memory error address. Only one error address will be stored.

Type: MultiBytes - R **Word Length:** 24			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
XmemStErrAdr3	0638	23-9	--
XmemStErrAdr2	0637	15-8	--
XmemStErrAdr1	0636	7-0	--

b23-b12: Row Address
b11-b9: Memory Bank Number
b8-b0: Column Address

UdCycDelta_T - MFP Cycle Number Up-Down Delta

Sets the number of system clock cycles the MFP cycle number is shortened or extended if tdm_rd_sync is not at the allowed position. This register influences delta_ref_cyc.

Type: MultiBytes - R/W **Word Length:** 11			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
UdCycDelta2_T	0641	10-8	00
UdCycDelta1_T	0640	7-0	00

Cnt_Prio - MFP Cycles Time Interval Setting

Sets the time interval in MFP cycles the priority is decremented

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cnt_Prio	0642	7-0	80

UdCycles - MFP Cycle Number Adjustment

Sets the number of system clock cycles the MFP cycle number is shortened or extended if tdm_rd_sync is not at the allowed position. This directly influences the jitter of the MFP clock.

Type: MultiBytes - R/W **Word Length:** 11			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
UdCycles2	0644	10-8	00
UdCycles1	0643	7-0	9C

FrameLen - TDM Frame Length

Sets the nominal TDM frame length in system clock cycles. This value is used for the prediction of the MFP clock. The default value corresponds to 432ms at nominal system clock.

Type: MultiBytes - R/W **Word Length:** 24			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
FrameLen3	0647	23-9	9D
FrameLen2	0646	15-8	AD
FrameLen1	0645	7-0	00

DeltaCycles - MFP Clock Period Monitor

Displays the deviation of the actual MFP clock period from the nominal value set in register FrameLen (0x0645/46/47). The value is given in number of system clock cycles.

Type: MultiBytes - R **Word Length:** 11			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
DeltaCycles2	0649	10-8	--
DeltaCycles1	0648	7-0	--

MFC - Master Frame Counter

Type: MultiBytes - R **Word Length:** 11			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MFC2	064B	10-8	--
MFC1	064A	7-0	--

MFC_lsb - Master Frame Counter (LSB)

Type: SingleByte - R **Word Length:** 7			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MFC_lsb	064C	6-0	--

TDM2Enable - TDM Management Block Enable

This register enables/disables the TDM2 internal blocks. The single block is enabled loading '1' in the corresponding bit.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TDM2Enable	064D	7-0	FF

b7: trs_en enable TDM read synchronization
b6: mcg_en enable MFP clock generation
b5: pdc_en enable PRC demultiplex controller
b4: trm_en enable TDM read management
b3: tam_en enable TDM external memory access management
b2: tmc_en enable TDM external memory controller
b1: twm_en enable TDM write management
b0: trb_en enable TDM bookkeeping

XmemFifoLevel - External Memory Write Access Buffer Filling Level

External memory write access buffer filling level. Maximum value is 12dec.

Type: SingleByte - R **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
XmemFifoLevel	064E	3-0	--

PcidDataRd - PCID Table Read Register

Using this register the internal prc demux table can be read together with the address register PcidAddr (0x0653) . In this register the pcid value together with the control flags for both pc interfaces is provided.

PcidDataWr1 (0x0651) contains the pcid number. PcidDataWr2 (0x0652) contains whether the pcid interface 0 (b8) or 1 (b9) is enabled (=1) or disabled (=0)

Type: MultiBytes - R **Word Length:** 10			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
PcidDataRd2	0650	9-8	--
PcidDataRd1	064F	7-0	--

PcidDataWr - PCID Number Write and PC Interface Port Enable

Using this register the internal prc demux table can be configured together with the address register PcidAddr (0x0653). In this register the pcid value together with the control flags for both pc interfaces is provided.

PcidDataWr1 (0x0651) contains the pcid number. PcidDataWr2 (0x0652) contains whether the pcid interface 0 (b8) or 1 (b9) is enabled (=1) or disabled (=0)

Type: MultiBytes - WRT **Word Length:** 10			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
PcidDataWr2	0652	9-8	00
PcidDataWr1	0651	7-0	00

PcidAddr - Payload Channel Identifier Table Address

Using this register the internal PRC demux table can be configured. The table has 28dec entries. This register holds the address where the PCID entry contained in register PcidDataWr (0x0652/51) is written into the table. In order to program the PCID table this register has to be set first. Starting with writing of PcidDataWr, the entry

is taken over into the internal PCID table.

Type: SingleByte - R/W **Word Length:** 5			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
PcidAddr	0653	4-0	00

PRC_ti - Time Interval Between two PRCs

The number written in this register must be multiplied by 1024 to get the time interval (in number of master clock cycles).

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
PRC_ti	0654	7-0	C8

Clock cycles between two PRCs: Prc_ti * 1024 + 1.

Since there are maximum 50 PRCs in a 432ms frame, with the reset value of this register the PRCs in the frame occupy the following time interval:

$$\frac{116 \cdot 1024 + 1}{23.92\Sigma 6} 50 = 248.3\text{ms}$$

WARNING: This value must be greater than 8 and less than 202 to have a correct function of the PC Interface.

TSCW_Err - Action Setting After Uncorrected TSCW

Determines the behaviour in case of an uncorrected TSCC1 of a TDM frame, i.e. possible corrupted TSCW.

Type: SingleByte - R/W **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TSCW_Err	0655	1-0	00

b1-b0: 00 = The TSCW of the last received error free TDM frame are used for decoding the PCs

01 = No PCs are decoded in case of TSCC1 RS uncorrected errors

10 = The received TSCWs are used for decoding

11 = NOT VALID.

TSCW_AddrRd - Word Address in the TSCW Table

This register addresses the word in the TSCW table the user wants to read. Whenever register Tscw_Data (0x0657) is read, this address is automatically incremented.

Type: SingleByte - WRT **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TSCW_AddrRd	0656	7-0	00

TSCW_Data - Addressed TSCW Word Contents

Contains the TSCW word which shall be read.

Type: SingleByte - RT **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
TSCW_Data	0657	7-0	--

StatusErr_T - Management Error and Error Flag

If trm_error=1 the next time interval has been started although not all data of the previous time interval have been processed.

Type: SingleByte - R **Word Length:** 2			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
StatusErr_T	0658	1-0	--

b1: trm_error TDM Read Management error flag

b0: trm_status 0= TDM Read Management disabled

1= TDM Read Management operational

MgmtCtrl_T - TDM Management Control Vector

If trm_first_proc=0/1 the satellite/terrestrial PRC packet is processed first in a time interval. If trm_terr_sat_comb_en=1 both terrestrial and satellite PRC packets are read. If trm_terr_sat_comb_en=0 only the PRC packets indicated by trm_first_proc (0:sat, 1:terr) are processed.

Type: SingleByte - R/W **Word Length:** 4			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
MgmtCtrl_T	0659	3-0	03

b3: trm_sat_format 0= satellite data from SDRAM in 2's complement

1= satellite data from SDRAM in offset binary

b2: trm_terr_format 0= terrestrial data from SDRAM in 2's complement

1= terrestrial data from SDRAM in offset binary

b1: trm_terr_sat_comb_en 0= Terr-Sat Combining disabled

1= Terr-Sat Combining enabled

b0: trm_first_proc 0= satellite PRC packet first

1= terrestrial PRC packet first

Tswc_AddCurr - TSCW Table Current Register Address

Type: SingleByte - R **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Tscw_AddCurr	065B	7-0	--

BK1-BK144 - TDM Management Book-Keeping Matrix

Type: SingleByte - TRT **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
BK1	0661	7-0	FF
BK2	0662	7-0	FF
...	...	...	...
BK144	06F0	7-0	FF

IrqMask_T - TDM Interrupt Mask

Type: SingleByte - INT **Word Length**: 3			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
IrqMask_T	06F5	2-0	00

b2: RFU
b1: RFU
b0: RFU

IrqStatus_T - TDM Interrupt Status

Type: SingleByte - INT **Word Length:** 3			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
IrqStatus_T	06F6	2-0	00

b2: RFU
b1: RFU
b0: RFU

2.9 Terrestrial Demodulator (Section 2)

CfCntGood_M - Counter for Coarse Frequency Good Event

Each time the Coarse Frequency calculates a new estimate that is good and is delivered to the Frequency Control this counter is incremented.

Type: MultiBytes - PR **Word Length:** 16			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
CfCntGood2_M	0711	15-8	00
CfCntGood1_M	0710	7-0	00

CfCntBad_M - **Counter for Coarse Frequency Bad Event**

Each time the Coarse Frequency calculates a new estimate that is bad (and then not used) this counter is incremented.

Type: MultiBytes - PR **Word Length:** 16			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
CfCntBad2_M	0716	15-8	00
CfCntBad1_M	0715	7-0	00

CfCtrl_M - **Coarse Frequency Control**

Type: SingleByte - R/W **Word Length:** 1			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
CfCtrl_M	0708	0	00

b0 : Use_All_AMSS '0'=Use AMSS samples only in case of frame sync detection.
'1'=Use AMSS samples even predidted ones.

Cf_MinKexpLow_M - **Coarse Frequency Estimation Confidence Threshold**

Control of threshold value for good/bad decision of cf algorithm. This value determines the absolute minimum of the confidence threshold value for the distinction between good and bad estimates independently of the history stored within the sliding window buffer (see register 0x072D).

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_MinKexpLow_M	0720	7-0	90

Cf_DiffKexpMaxLow_M - **Coarse Frequency Estimation Confidence Threshold**

Control of threshold value for good/bad decision of cf algorithm. This value is used to determine the relative minimum of the confidence threshold value for the distinction between good and bad estimates dependent on the maximum frequency estimate confidence value stored in the sliding window buffer (see register 0x072D). The relative minimum is calculated by the maximum estimate confidence value within the sliding window buffer minus the register value. The maximum value of both absolute and relative minimum values determines the lowest confidence threshold used by the algorithm.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_DiffKexpMaxLow_M	0721	7-0	08

Cf_Delta_KexpLow_M - **Coarse Frequency Estimation Confidence Threshold**

Control of threshold value for good/bad decision of cf algorithm. This value is the decrement of the threshold

value each time the algorithm lowers the confidence threshold due to bad estimates.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_Delta_KexpLow_M	0722	7-0	01

Cf_DeltaCntLow_M - **Coarse Frequency Estimation Confidence Threshold**

Coarse Frequency Estimation Confidence Threshold Control. This value is the number of subsequent bad estimates for lowering the confidence threshold by a decrement of register 0x0722

Type: SingleByte - R/W **Word Length:** 10			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_DeltaCntLow2_M	0724	9-8	00
Cf_DeltaCntLow1_M	0723	7-0	20

Cf_MaxKexpHigh_M - **Coarse Frequency Estimation Confidence Threshold**

Control of threshold value for good/bad decision of cf algorithm. This value determines the absolute maximum of the confidence threshold value for the distinction between good and bad estimates independent of the history stored within the sliding window buffer (see register 0x072D).

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_MaxKexpHigh_M	0726	7-0	FF

Cf_DiffKexpMaxHigh_M - **Coarse Frequency Estimation Confidence Threshold**

Control of threshold value for good/bad decision of cf algorithm. This value is used to determine the relative maximum of the confidence threshold value for the distinction between good and bad estimates dependent on the maximum frequency estimate confidence value stored in the sliding window buffer (see register 0x072D). The relative maximum is calculated by the maximum estimate confidence value within the sliding window buffer minus the register value. The minimum value of both absolute and relative maximum values determines the highest confidence threshold used by the algorithm.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_DiffKexpMaxHigh_M	0727	7-0	06

Cf_DeltaKexpHigh_M - **Coarse Frequency Estimation Confidence Threshold**

Control of threshold value for good/bad decision of cf algorithm. This value is the increment of the threshold value each time the algorithm enlarges the confidence threshold due to good estimates.

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_DeltaKexpHigh_M	0728	7-0	01

Cf_DeltaCntHigh_M - **Coarse Frequency Estimation Confidence Threshold**

This value is the number of subsequent good estimates for enlarging the confidence threshold by an increment of register 0x0728

Type: SingleByte - R/W **Word Length:** 10			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_DeltaCntHigh2_M	072A	9-8	00
Cf_DeltaCntHigh1_M	0729	7-0	01

Cf_InitDelay_M - **Coarse Frequency Estimation Initial Delay**

This value determines the minimum number of AMSS estimates stored in the sliding window average before the first estimate is put out. For the calculation of the first cf estimate, Cf_InitDelay_M+1 estimates are taken into account. Within the initial phase no confidence threshold is applied and all estimates are good. Nevertheless the confidence threshold is calculated and used for the Cf_InitDelay_M+2nd estimate.

Type: SingleByte - R/W **Word Length:** 5			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_InitDelay_M	072B	4-0	17

Cf_KexpThAct_M - **Current Confidence Threshold Value**

This register hold the current confidence threshold value the CF algorithm takes to distinguish between good and bad Coarse Frequency estimates. If the internally calculated confidence value is equal or larger than the current threshold the estimate is considered as good.

Type: SingleByte - R **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_KexpThAct_M	072D	7-0	--

Cf_EstAct_M - **Coarse Frequency Estimation of AMSS Before Averaging**

With each received AMSS sequence a new frequency estimate is calculated together with a confidence value. Then an averaging over good estimates is performed. Within this register the coarse frequency estimate of the received AMSS before averaging is held.

Type: SingleByte - R/W **Word Length:** 16			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_EstAct2_M	0731	15-8	--
Cf_EstAct1_M	0730	7-0	--

Cf_KexpActExp_M - Coarse Frequency Confidence Exponent of AMSS Before Averaging

With each received AMSS sequence a new frequency estimate is calculated together with a confidence value. Then an averaging over good estimates is performed. Within this register the confidence exponent of the coarse frequency estimate of the received AMSS before averaging is held.

Type: SingleByte - R **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_KexpActExp_M	0735	7-0	--

Cf_Est_M - Coarse Frequency Estimation of AMSS After averaging

With each received AMSS sequence a new frequency estimate is calculated together with a confidence value. Then an averaging over good estimates is performed. Within this register the coarse frequency estimate of the received AMSS after averaging is held.

Type: SingleByte - R/W **Word Length:** 16			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_Est2_M	0741	15-8	--
Cf_Est1_M	0740	7-0	--

Cf_EstExp_M - Coarse Frequency Confidence Exponent of AMSS After Averaging

With each received AMSS sequence a new frequency estimate is calculated together with a confidence value. Then an averaging over good estimates is performed. Within this register the confidence exponen of the coarse frequency estimate of the received AMSS after averaging is held._

Type: SingleByte - R **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_EstExp_M	0745	7-0	--

AvgEst_M - Current Coarse Frequency Averager Estimates

This register shows the current CF estimate after the MCM CF Averager which is applied to the MCM Frequency Control. With each received CF estimate an new averaged CF estimte is put out when the corresponding confidence value exceeds the required threshold.

Type: SingleByte - R/W **Word Length:** 16			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_AvgEst2_M	0751	15-8	--
Cf_AvgEst1_M	0750	7-0	--

Cf_AvgEstExp_M - **Current Coarse Frequency Averager Confidence Estimates**

This register shows the CF confidence value after the MCM CF Averager block. This confidence value is applied to the MCM Frequency Control.

Type: SingleByte - R **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_AvgEstExp_M	0755	7-0	--

Cf_AvgCtrl - **Coarse Frequency Averager Control Register**

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_AvgCtrl	0780	7-0	B0

b7 : avg_en 0 = Disabled; 1 = Enabled

b6 : init_th_en 0 = Disabled; 1 = Enabled

b5-b3 : avg_len TBD

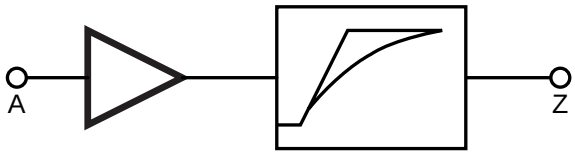
b2-b0 : init_avg_delay TBD

Cf_AvgMinEstConf - **Threshold for Coarse Frequency Confidence**

Type: SingleByte - R/W **Word Length:** 8			
Byte Name	**Address (Hex)**	**Bit Map**	**Reset Value (Hex)**
Cf_AvgCtrl	0780	7-0	B0

3 I/O CELL DESCRIPTION

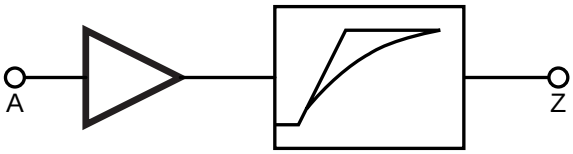
1) CMOS Output Pad Buffer, 2mA with slew rate control.



D98AU920

EXTERNAL PIN	MAX. LOAD
Z	50pF

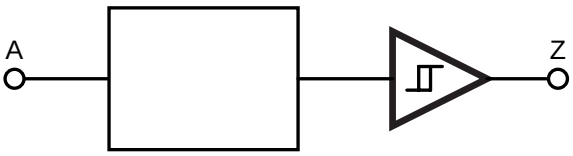
2) CMOS Output Pad Buffer, 4mA with slew rate control.



D98AU920

EXTERNAL PIN	MAX. LOAD
Z	100pF

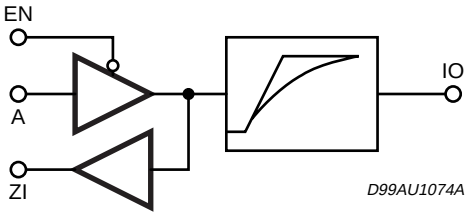
3) CMOS Schmitt Trigger Input Pad Buffer



D99AU1072

EXTERNAL PIN	CAPACITANCE
A	1pF

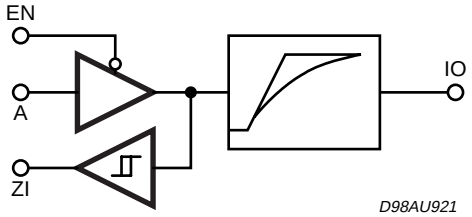
4) CMOS BiDir Pad Buffer, 2mA with slew rate control.



D99AU1074A

EXTERNAL PIN	INPUT CAP	MAX. LOAD
I/O	1.5pF	50pF

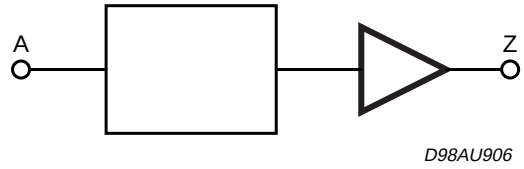
5) CMOS Schmitt Trigger BiDir Pad Buffer, 4mA with slew rate control



D98AU921

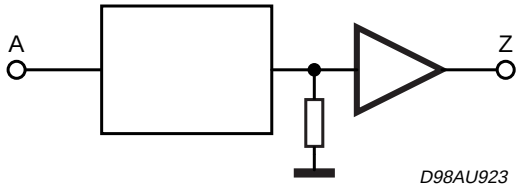
EXTERNAL PIN	INPUT CAP	MAX. LOAD
I/O	1.9pF	100pF

6) CMOS Input Pad Buffer, High Drive



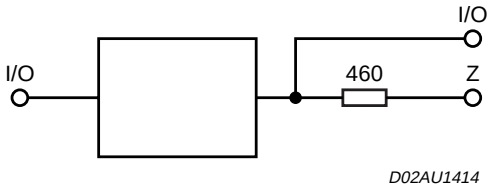
EXTERNAL PIN	CAPACITANCE
A	1.0pF

7) CMOS Input Pad Buffer with Active Pull-Down (50kΩ resistor)



EXTERNAL PIN	CAPACITANCE
A	1.0pF

8) Analog Pad Buffer



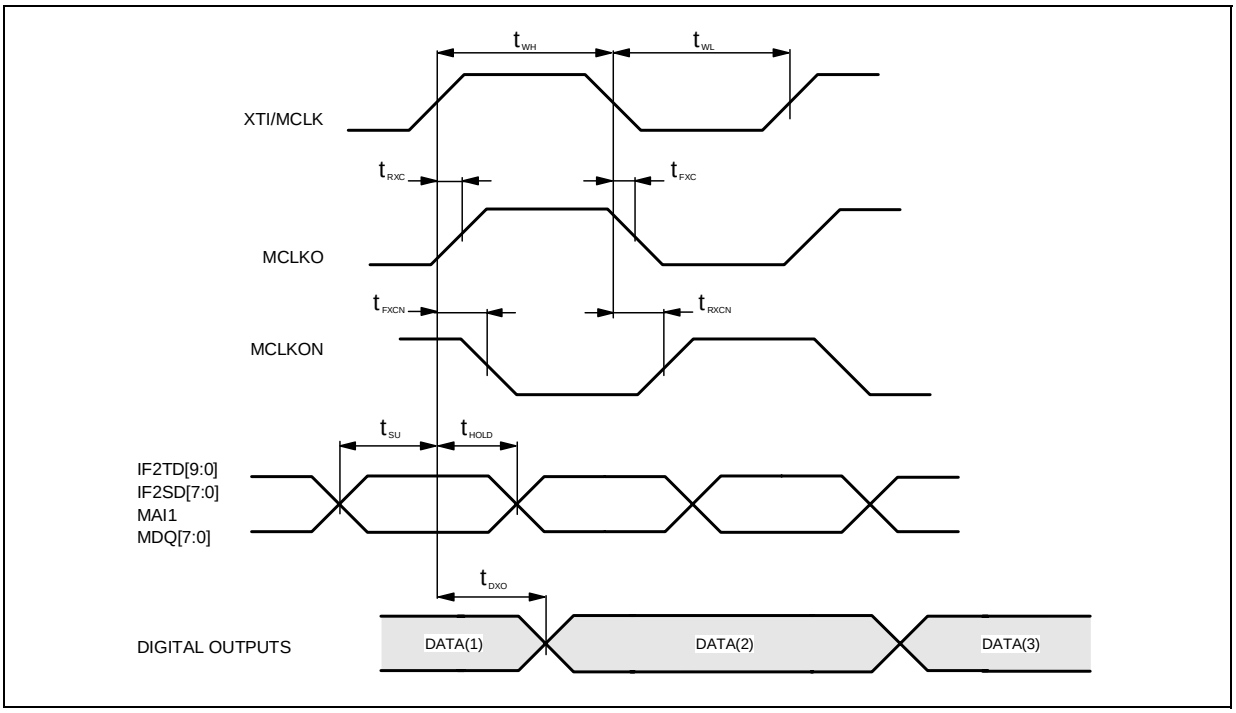
EXTERNAL PIN	INPUT CAP	MAX. LOAD
I/O (when input)	1.9pF	
I/O (when output)		200pF

Max Voltage Swing
min: gnd-0.8 V max: vdd+0.8 V
Vdd = 1.8 V

9 TIMING DIAGRAMS

9.1 AC Characterictics (Guaranteed by Design)

Figure 17. Clocks and I/O Timing Diagram

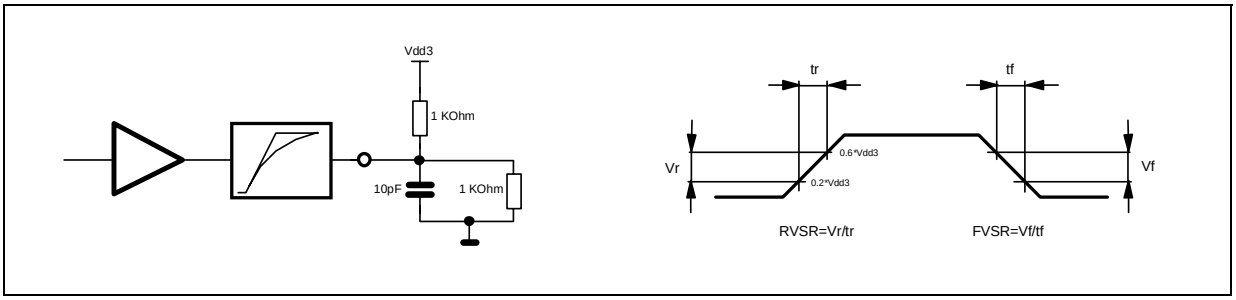


Symbol	Parameter	Min	Max	Unit
t_{WH}	Clock High Pulse Width	6		nsec
t_{WL}	Clock Low Pulse Width	6		nsec
t_{RXC}	Rise Delay (XTI/MCLK Clock Input to MCLKO Clock Output)		7	nsec
t_{RXCN}	Rise Delay (XTI/MCLK Clock Input to MCLKON Clock Output)		10	nsec
t_{FXC}	Fall Delay (XTI/MCLK Clock Input to MCLKO Clock Output)		7	nsec
t_{FXCN}	Fall Delay (XTI/MCLK Clock Input to MCLKON Clock Output)		9	nsec
t_{SU}	Input Set-up Time	1		nsec
t_{HOLD}	Input Hold Time	5		nsec
t_{DXO}	Output Data Valid Delay		13	nsec

Load Circuit: 50 pF to ground.

9.2) Output Buffer Drive Characterictics (Guaranteed by Design)

Figure 18. Slew Rate Load Circuit

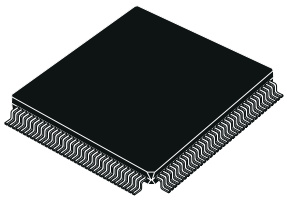


Symbol	Parameter	Buffer	Codition	Min	Typ	Max	Unit
RVSR	Rise Voltage Slew Rate	2mA Driver 1)	With Load 2)	0.8	1.2	1.9	V/ns
			No Load)	4.0	6.1	8.3	V/ns
FVSR	Fall Voltage Slew Rate	2mA Driver	With Load 2)	0.8	1.2	1.9	V/ns
			No Load	3.6	5.3	7.9	V/ns
RVSR	Rise Voltage Slew Rate	4mA Driver 1)	With Load 2)	1.1	1.8	2.8	V/ns
			No Load	4.6	6.8	9.6	V/ns
FVSR	Fall Voltage Slew Rate	4mA Driver	With Load 2)	1.2	1.8	2.6	V/ns
			No Load	3.8	5.4	9.2	V/ns
CSR 3)	Current Slew Rate	2mA Driver 4)	35pF load 6)		8.0		mA/ns
		4mA Driver 5)	35pF load 6)		6.0		mA/ns

1) See PIN DESCRIPTION.
2) Load Circuit: see fig.17.
3) The Current Slew Rate values are the mean values between currents in Vdd=3.3V and GND power lines for one buffer.
4) Typical Peak Current in GND: 24mA.
5) Typical Peak Current in GND: 50mA.
6) Temperature 25 °C, Vdd=3.3V.

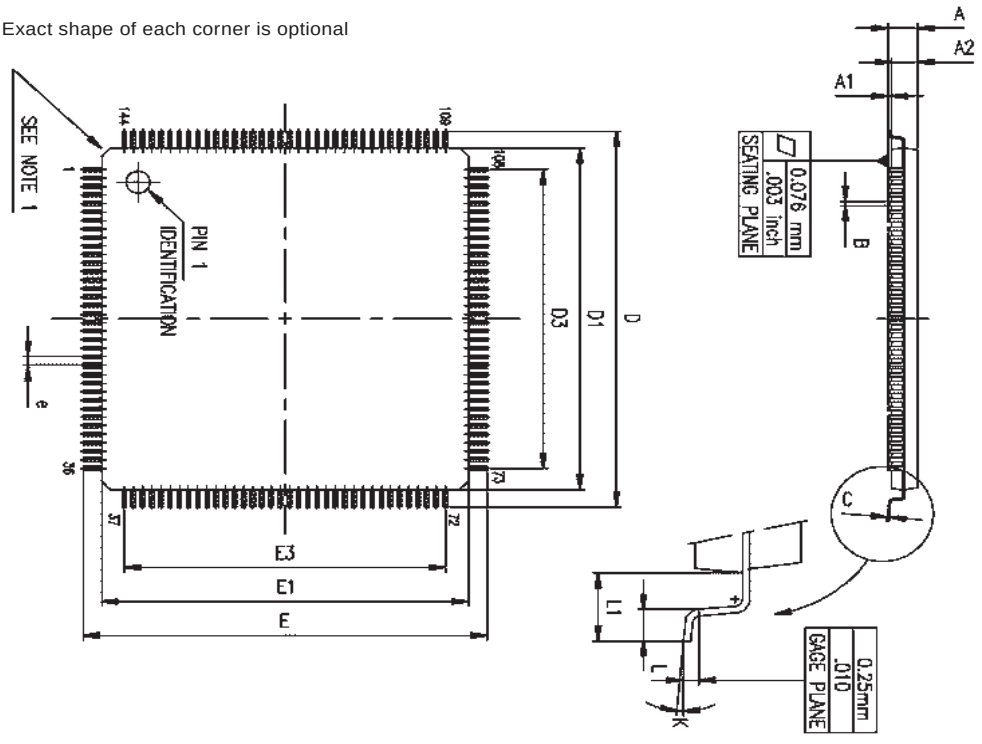
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.003		0.008
D		22.00			0.866	
D1		20.00			0.787	
D3		17.50			0.689	
e		0.50			0.020	
E		22.00			0.866	
E1		20.00			0.787	
E3		17.50			0.689	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.0393	
K	3.5° (min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP144
(20x20x1.40mm)

Note 1: Exact shape of each corner is optional



0099183