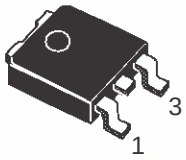
STD30NF03L

N - CHANNEL 30V - 0.020 Ω - 30A DPAK STripFET™ POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STD30NF03L	30 V	< 0.025 Ω	30 A

- TYPICAL $R_{DS(on)}$ = 0.020 Ω
- LOW THRESHOLD DRIVE
- ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL

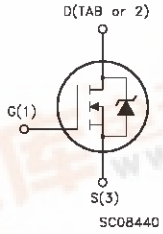


DPAK
TO-252
(Suffix "T4")

DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC & DC-AC CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	30	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	30	V
V_{GS}	Gate-source Voltage	± 20	V
I_D(•)	Drain Current (continuous) at T_c = 25 °C	30	A
I_D	Drain Current (continuous) at T_c = 100 °C	19	A
I_{DM}(••)	Drain Current (pulsed)	120	A
P_{tot}	Total Dissipation at T_c = 25 °C	40	W
	Derating Factor	0.27	W/°C
E_{AS}(1)	Single Pulse Avalanche Energy	100	m/J
T_{stg}	Storage Temperature	-65 to 175	°C
T_j	Max. Operating Junction Temperature	175	°C

(••) Pulse width limited by safe operating area
(1) starting T_j = 25 °C, I_D = 15A , V_{DD} = 15V
(•)Current limited by the package

THERMAL DATA

$R_{thj\text{-}pcb}$	Thermal Resistance Junction-PC Board	Max	3.75	$^oC/W$
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	$^oC/W$
$R_{thj\text{-}sink}$	Thermal Resistance Case-sink	Typ	1.5	$^oC/W$
T_l	Maximum Lead Temperature For Soldering Purpose		275	^oC

ELECTRICAL CHARACTERISTICS (T_{case} = 25 ^oC unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA V_{GS} = 0	30			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_c = 125 ^oC			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	1	1.7	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 15 A V_{GS} = 4.5 V I_D = 15 A		0.020 0.028	0.025 0.035	Ω Ω
$I_{D(on)}$	On State Drain Current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$ V_{GS} = 10 V	30			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$ I_D = 15 A		13		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0 V		830 230 92		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 15 V I_D = 20 A R_G = 4.7 Ω V_{GS} = 4.5 V (Resistive Load, see fig. 3)		35 205		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 24 V I_D = 30 A V_{GS} = 5 V		18 7 8		nC nC nC

SWITCHING OFF

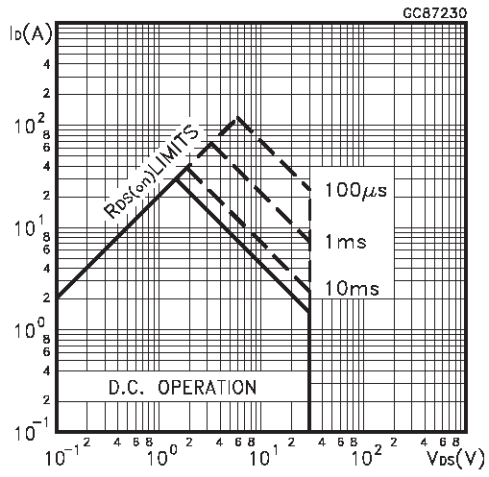
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 15 V I_D = 20 A R_G = 4.7 Ω V_{GS} = 4.5 V (Resistive Load, see fig. 3)		90 240		ns ns

SOURCE DRAIN DIODE

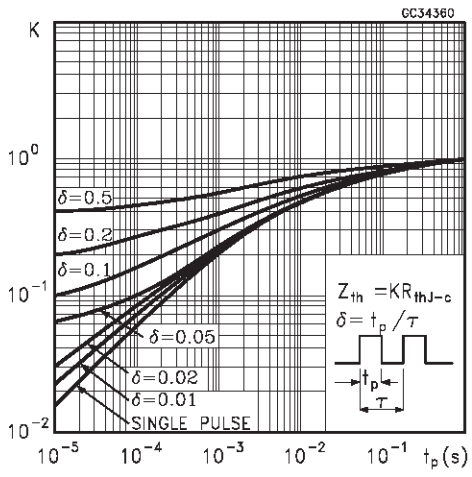
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(•)	Source-drain Current Source-drain Current (pulsed)				30 120	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 30 A V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 40 A di/dt = 100 A/µs V_{DD} = 15 V T_j = 150 °C (see test circuit, fig. 5)		65 72 2		ns nC A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

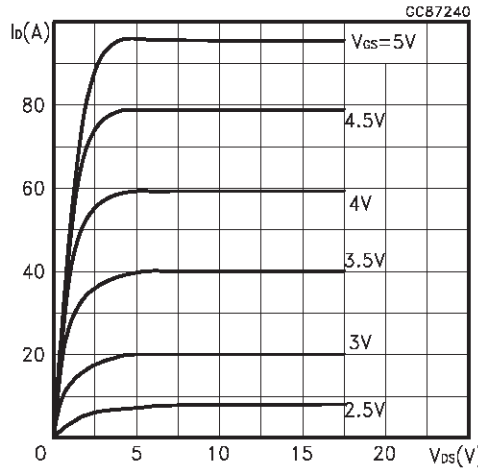
Safe Operating Area



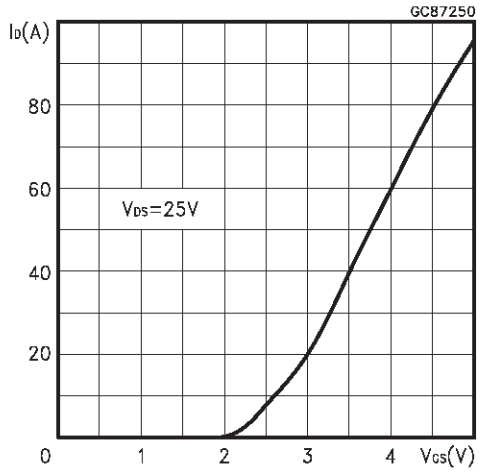
Thermal Impedance



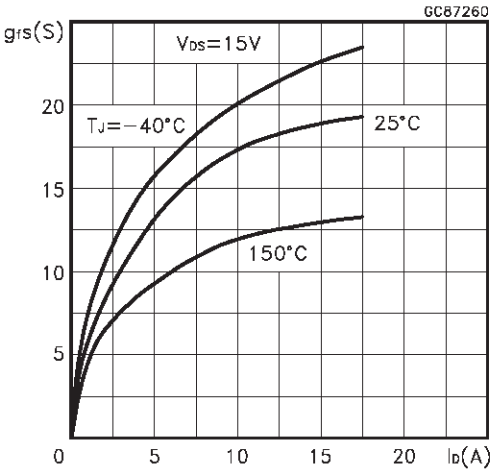
Output Characteristics



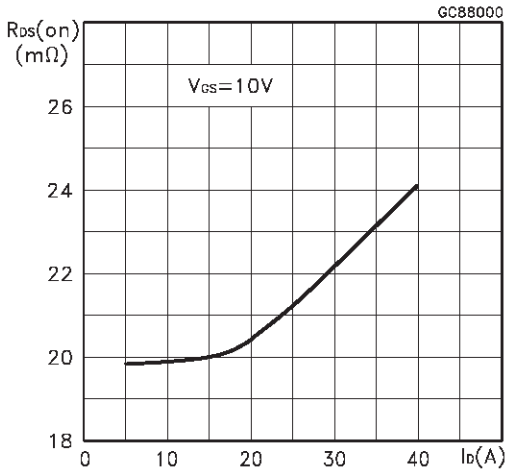
Transfer Characteristics



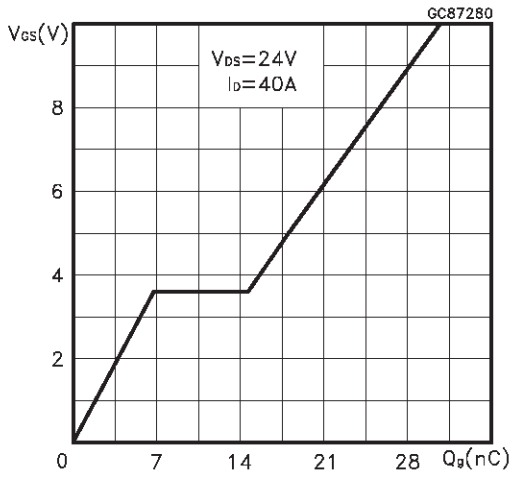
Transconductance



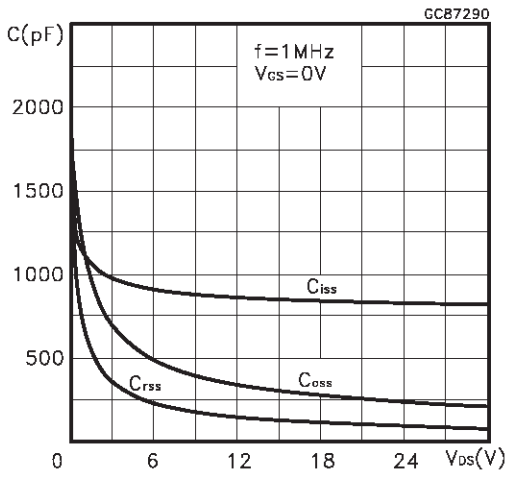
Static Drain-source On Resistance



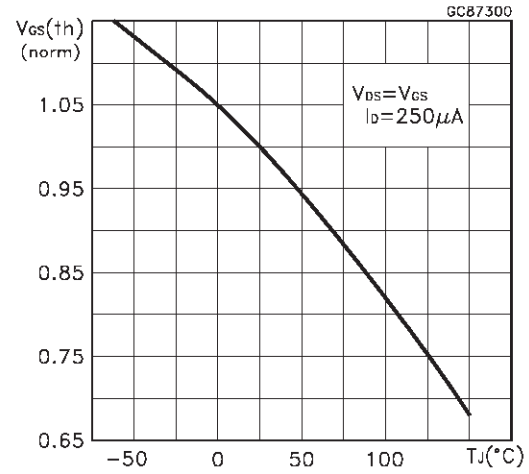
Gate Charge vs Gate-source Voltage



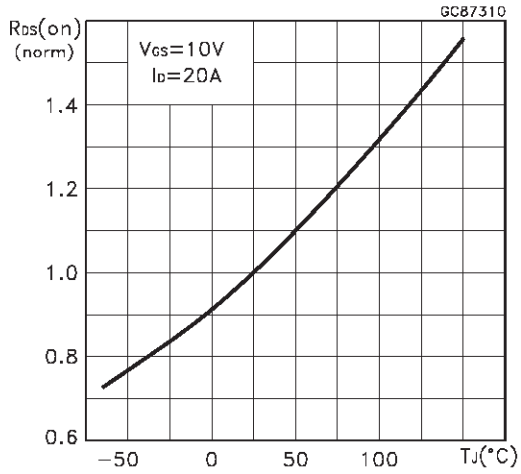
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

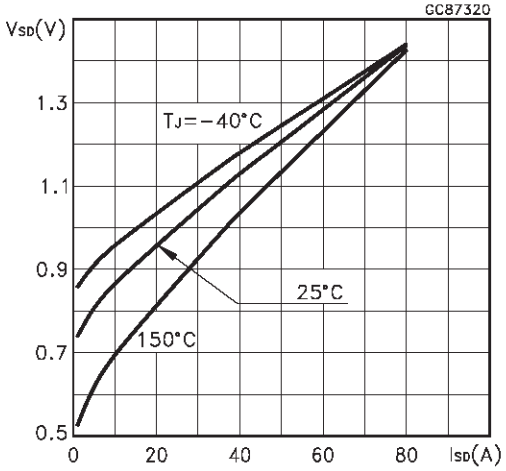


Fig. 1: Unclamped Inductive Load Test Circuit

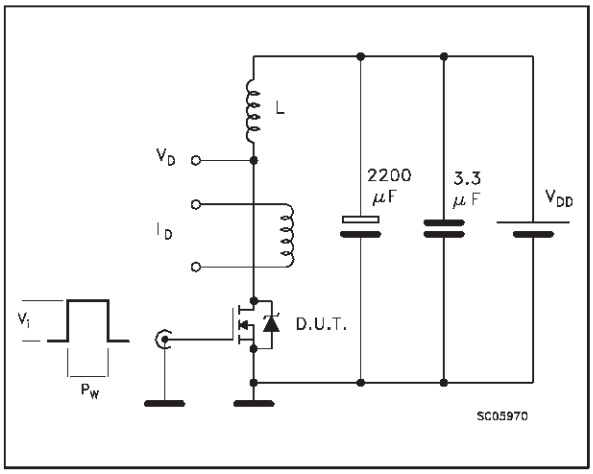


Fig. 2: Unclamped Inductive Waveform

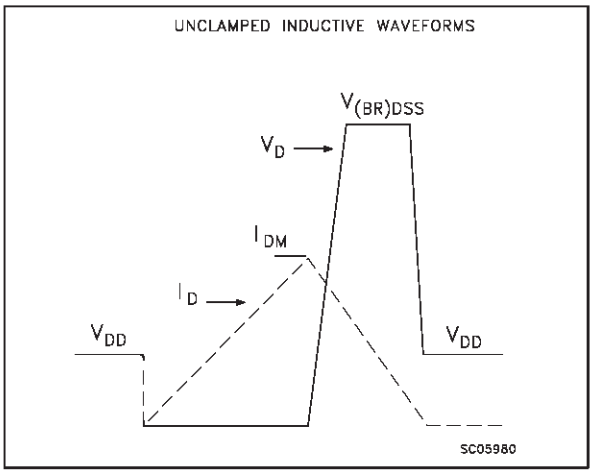


Fig. 3: Switching Times Test Circuits For Resistive Load

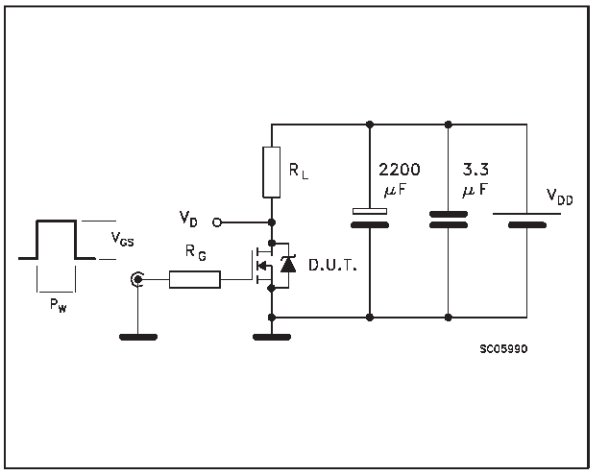


Fig. 4: Gate Charge test Circuit

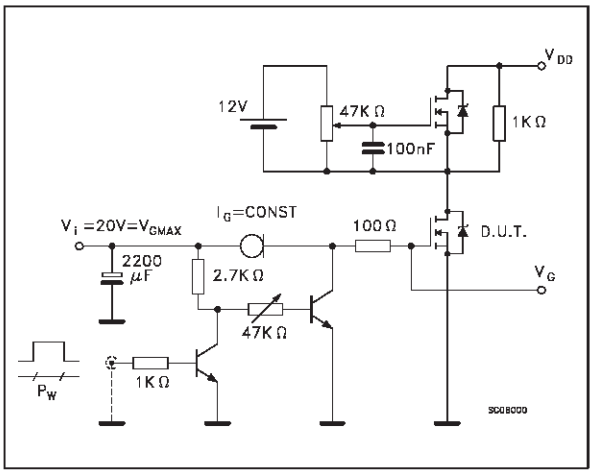
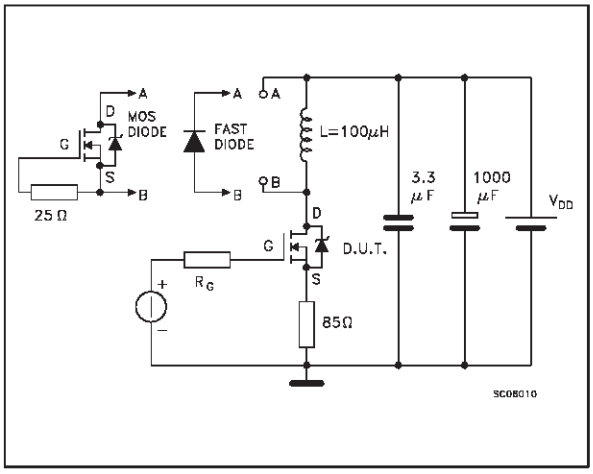
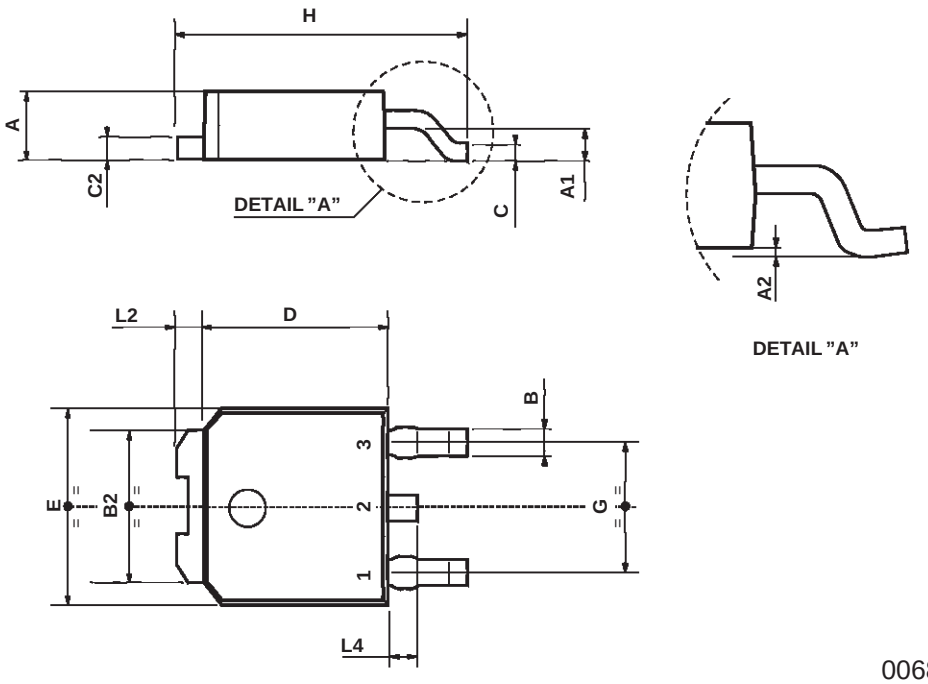


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



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