



STD40NF06LZ

N-CHANNEL 60V - 0.020 Ω - 40A DPAK Zener-Protected STripFET™ II POWER MOSFET

| TYPE | V _{DSS} | R _{DS(on)} | I _D |
|-------------|------------------|---------------------|----------------|
| STD40NF06LZ | 60 V | < 25 mΩ | 40 A |

- TYPICAL R_{DS(on)} = 0.020Ω
- 100% AVALANCHE TESTED
- LOW GATE CHARGE
- LOGIC LEVEL GATE DRIVE
- SURFACE-MOUNTING DPAK (TO-252)
POWER PACKAGE IN TAPE & REEL
(SUFFIX "T4")
- BUILT-IN ZENER DIODES TO IMPROVE ESD
PROTECTION UP TO 2kV

DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

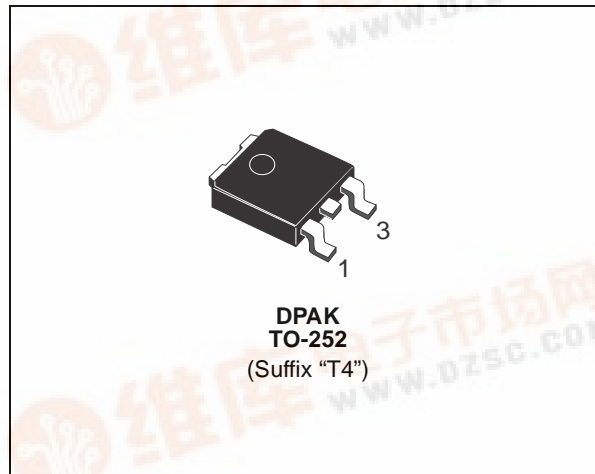
APPLICATIONS

- SINGLE-ENDED SMPS IN MONITOTS,
COMPUTER AND INDUSTRIAL
APPLICATION
- WELDING EQUIPMENT
- AUTOMOTIVE

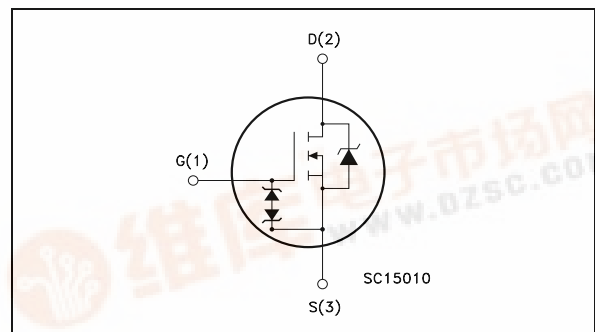
ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------------------|--|------------|------|
| V _{DS} | Drain-source Voltage (V _{GS} = 0) | 60 | V |
| V _{DGR} | Drain-gate Voltage (R _{GS} = 20 kΩ) | 60 | V |
| V _{GS} | Gate- source Voltage | ± 16 | V |
| I _D | Drain Current (continuous) at T _C = 25°C | 40 | A |
| I _D | Drain Current (continuous) at T _C = 100°C | 28 | A |
| I _{DM} (●) | Drain Current (pulsed) | 160 | A |
| P _{tot} | Total Dissipation at T _C = 25°C | 100 | W |
| | Derating Factor | 0.67 | W/°C |
| V _{ESD(G-S)} | Gate-source ESD(HBM-C=100pF, R=15kΩ) | ± 2.5 | kV |
| dv/dt(1) | Peak Diode Recovery voltage slope | 9 | V/ns |
| E _{AS} (2) | Single Pulse Avalanche Energy | 450 | mJ |
| T _{stg} | Storage Temperature | -55 to 175 | °C |
| T _j | Max. Operating Junction Temperature | | |

(●) Pulse width limited by safe operating area.



INTERNAL SCHEMATIC DIAGRAM



(1) I_{SD} ≤ 40A, di/dt ≤ 100A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.
(2) Starting T_j = 25 °C I_D = 20A V_{DD} = 45V

STD40NF06LZ

THERMAL DATA

| | | | | |
|----------------|--|-----|-----|------|
| Rthj-case | Thermal Resistance Junction-case | Max | 1.5 | °C/W |
| Rthj-PCB | Thermal Resistance Junction-PCB (#) | Max | 50 | °C/W |
| T _l | Maximum Lead Temperature For Soldering Purpose | | 300 | °C |

(#) When Mounted on 1 inch² FR-4 board, 2 oz Cu.

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------------------|---|---|------|------|---------|----------|
| V _{(BR)DSS} | Drain-source Breakdown Voltage | I _D = 250 μA, V _{GS} = 0 | 60 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current (V _{GS} = 0) | V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C | | | 1 50 | μA μA |
| I _{GSS} | Gate-body Leakage Current (V _{DS} = 0) | V _{GS} = ± 16 V | | | ±10 | μA |

ON (*)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---------------------|-----------------------------------|---|------|------|----------------|--------|
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} = V _{GS} I _D = 250 μA | 1 | | | V |
| R _{DS(on)} | Static Drain-source On Resistance | V _{GS} = 5 V I _D = 20 A V _{GS} = 10 V I _D = 20 A | | | 0.030 0.025 | Ω Ω |

DYNAMIC

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---------------------|------------------------------|---|------|------|------|------|
| g _{fs} (*) | Forward Transconductance | V _{DS} = 15 V I _D = 20 A | | 25 | | S |
| C _{iss} | Input Capacitance | V _{DS} = 25V, f = 1 MHz, V _{GS} = 0 | | 1360 | | pF |
| C _{oss} | Output Capacitance | | | 302 | | pF |
| C _{rss} | Reverse Transfer Capacitance | | | 115 | | pF |

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------|--|---|------|----------------|------|----------------|
| $t_{d(on)}$ t_r | Turn-on Delay Time Rise Time | $V_{DD} = 30\text{ V}$ $I_D = 20\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 3) | | 17 75 | | ns ns |
| Q_g Q_{gs} Q_{gd} | Total Gate Charge Gate-Source Charge Gate-Drain Charge | $V_{DD} = 48\text{ V}$ $I_D = 40\text{ A}$ $V_{GS} = 10\text{ V}$ | | 54 11 12 | | nC nC nC |

SWITCHING OFF

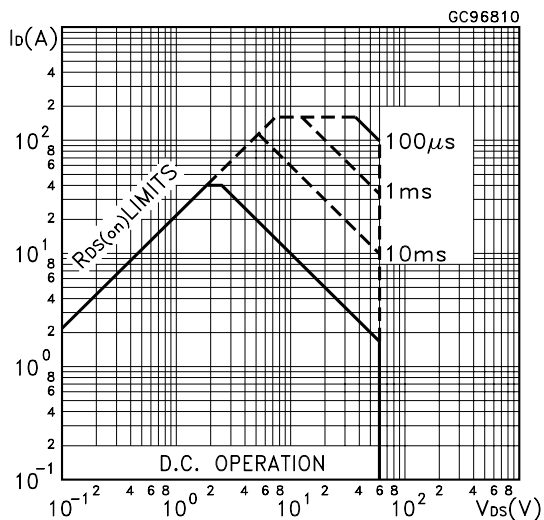
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-----------------------|----------------------------------|---|------|----------|------|----------|
| $t_{d(off)}$ t_f | Turn-off Delay Time Fall Time | $V_{DD} = 30\text{ V}$ $I_D = 20\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 3) | | 38 23 | | ns ns |

SOURCE DRAIN DIODE

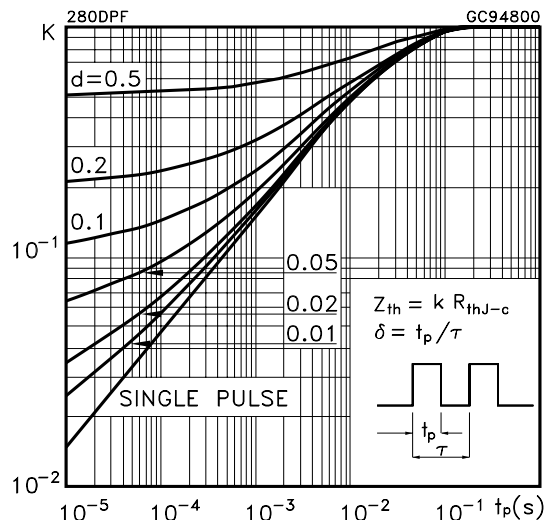
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-----------------------------------|--|---|------|------------------|-----------|---------------|
| I_{SD} $I_{SDM} (\bullet)$ | Source-drain Current Source-drain Current (pulsed) | | | | 40 160 | A A |
| $V_{SD} (*)$ | Forward On Voltage | $I_{SD} = 40\text{ A}$ $V_{GS} = 0$ | | | 1.6 | V |
| t_{rr} Q_{rr} I_{RRM} | Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current | $I_{SD} = 40\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5) | | 66 142 4.3 | | ns nC A |

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %
 (•) Pulse width limited by safe operating area.

Safe Operating Area

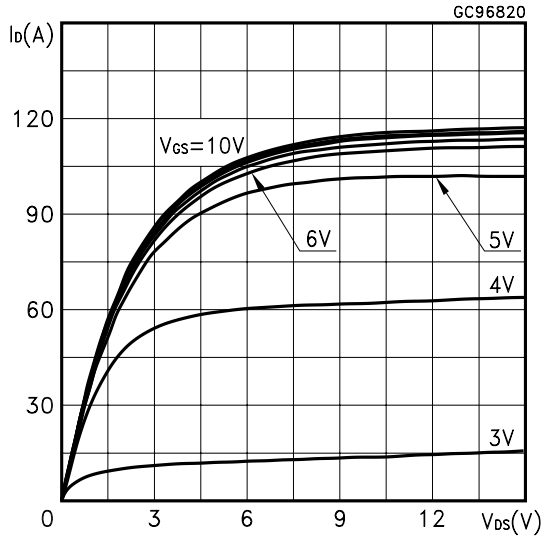


Thermal Impedance

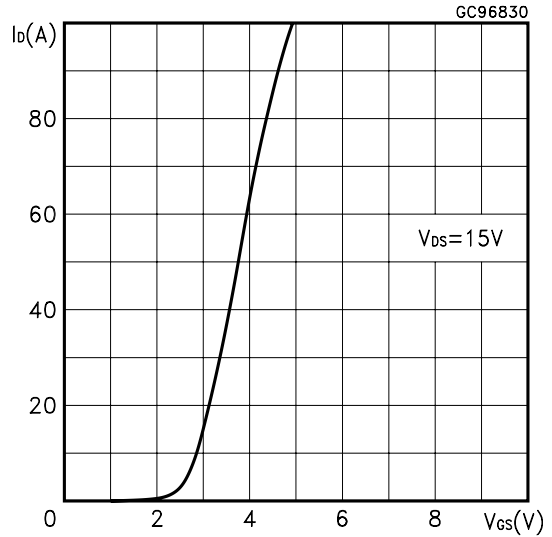


STD40NF06LZ

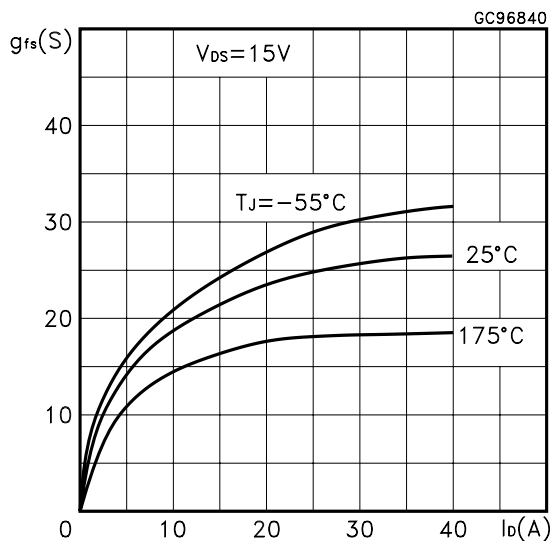
Output Characteristics



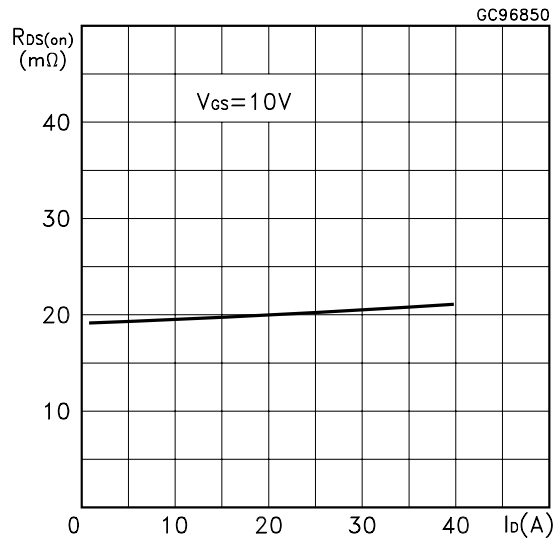
Transfer Characteristics



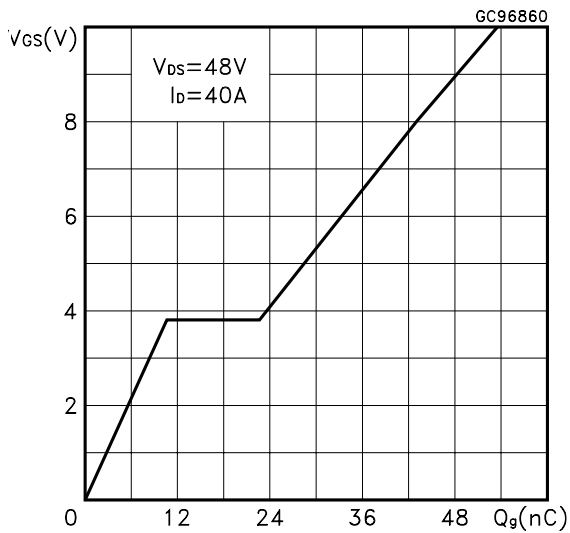
Transconductance



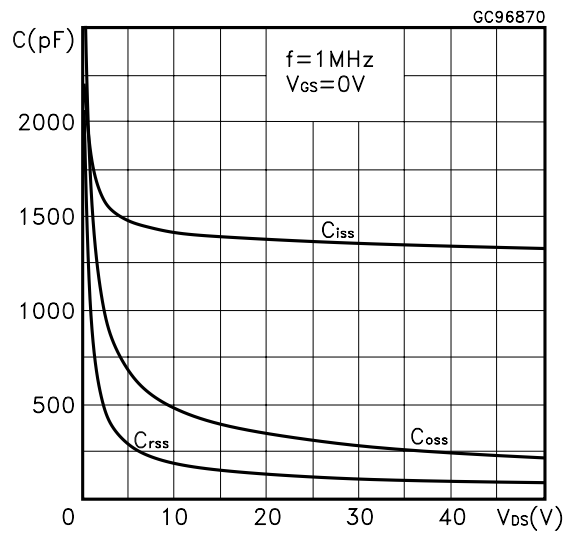
Static Drain-source On Resistance



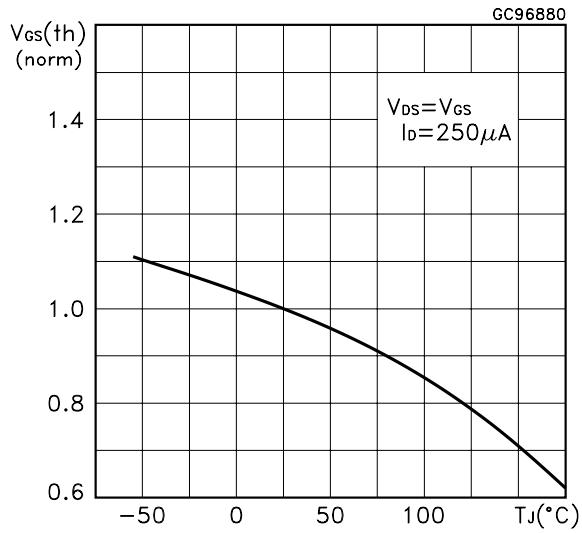
Gate Charge vs Gate-source Voltage



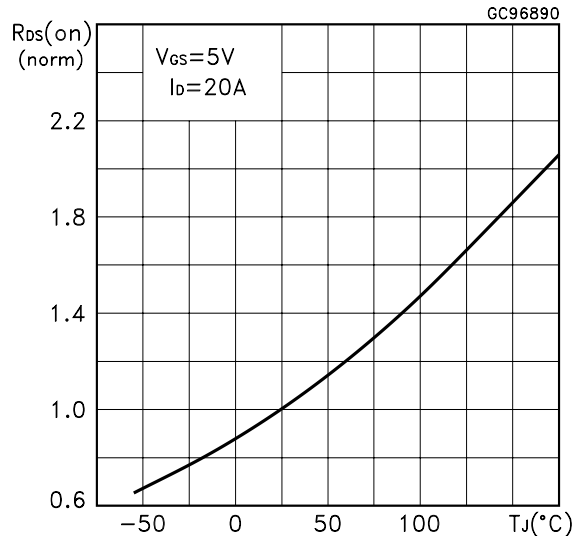
Capacitance Variations



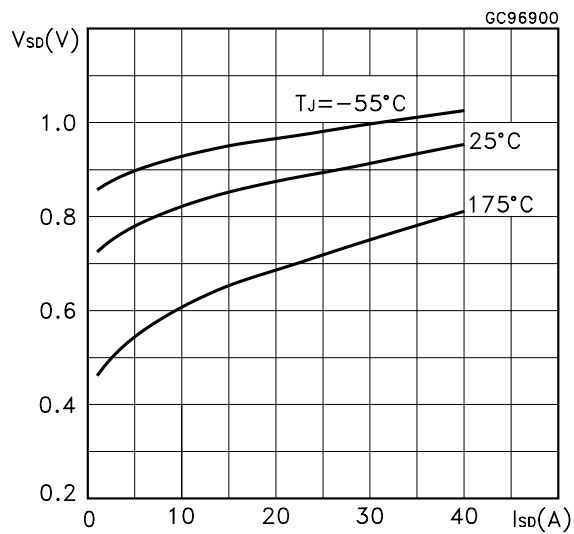
Normalized Gate Threshold Voltage vs Temperature



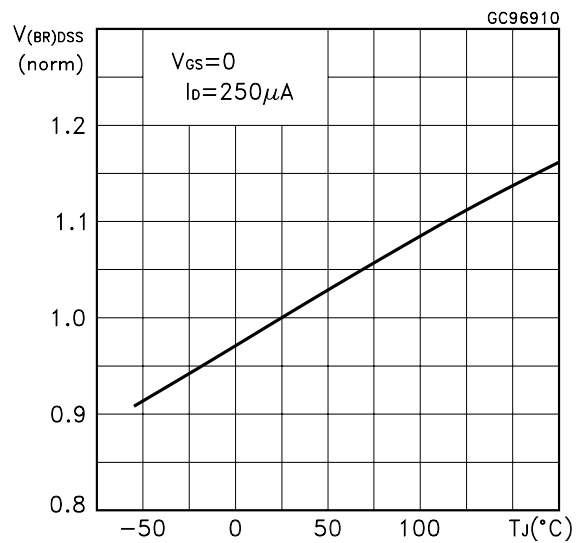
Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Temperature.



STD40NF06LZ

Fig. 1: Unclamped Inductive Load Test Circuit

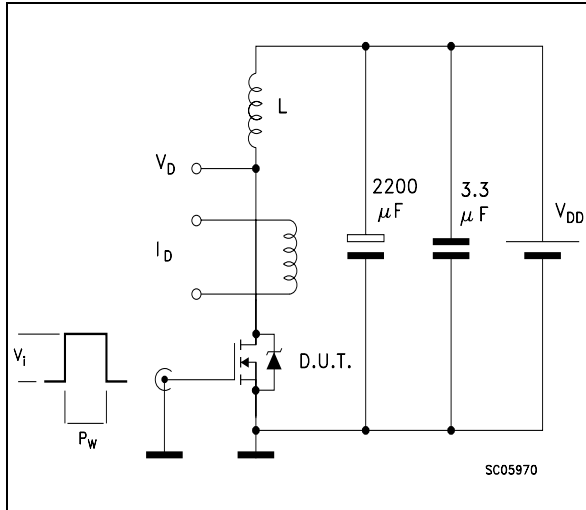


Fig. 2: Unclamped Inductive Waveform

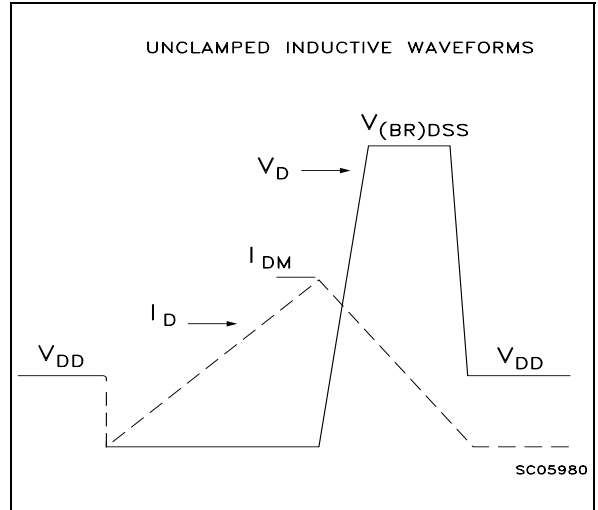


Fig. 3: Switching Times Test Circuits For Resistive Load

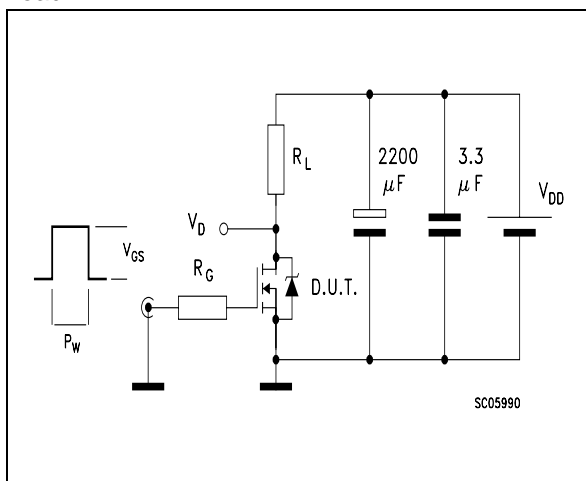


Fig. 4: Gate Charge test Circuit

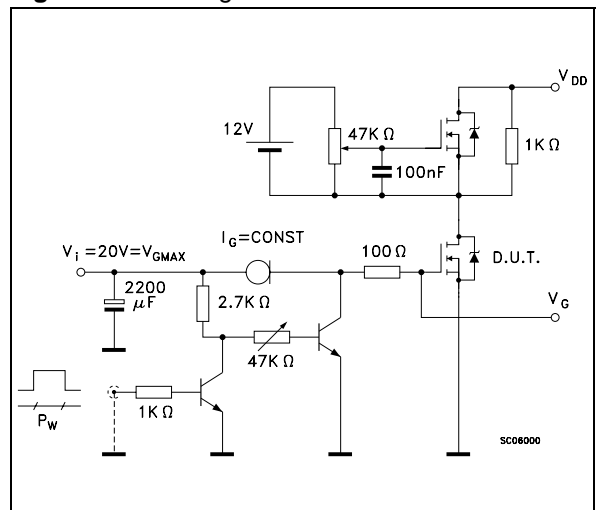
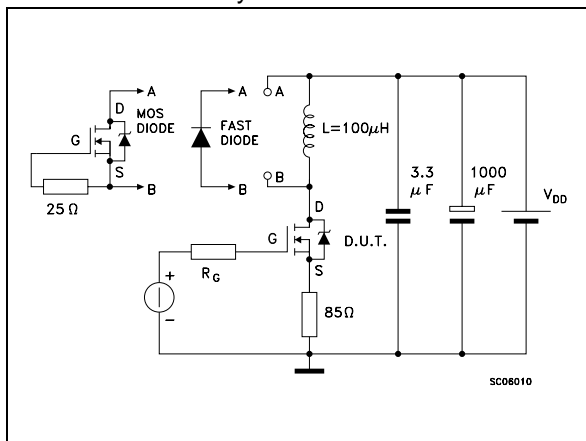
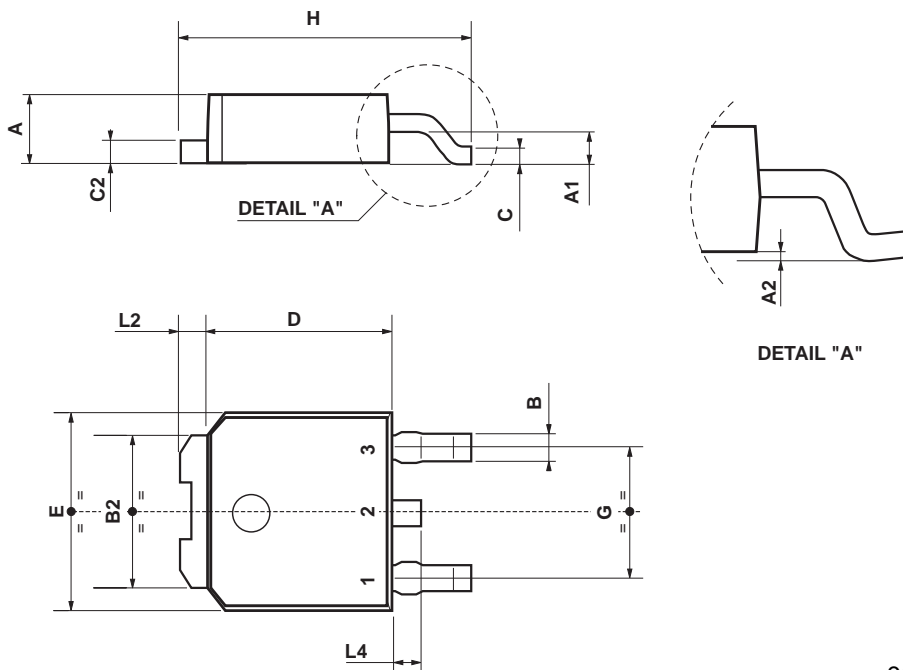


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-252 (DPAK) MECHANICAL DATA

| DIM. | mm | | | inch | | |
|------|------|------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 2.2 | | 2.4 | 0.086 | | 0.094 |
| A1 | 0.9 | | 1.1 | 0.035 | | 0.043 |
| A2 | 0.03 | | 0.23 | 0.001 | | 0.009 |
| B | 0.64 | | 0.9 | 0.025 | | 0.035 |
| B2 | 5.2 | | 5.4 | 0.204 | | 0.212 |
| C | 0.45 | | 0.6 | 0.017 | | 0.023 |
| C2 | 0.48 | | 0.6 | 0.019 | | 0.023 |
| D | 6 | | 6.2 | 0.236 | | 0.244 |
| E | 6.4 | | 6.6 | 0.252 | | 0.260 |
| G | 4.4 | | 4.6 | 0.173 | | 0.181 |
| H | 9.35 | | 10.1 | 0.368 | | 0.397 |
| L2 | | 0.8 | | | 0.031 | |
| L4 | 0.6 | | 1 | 0.023 | | 0.039 |



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