

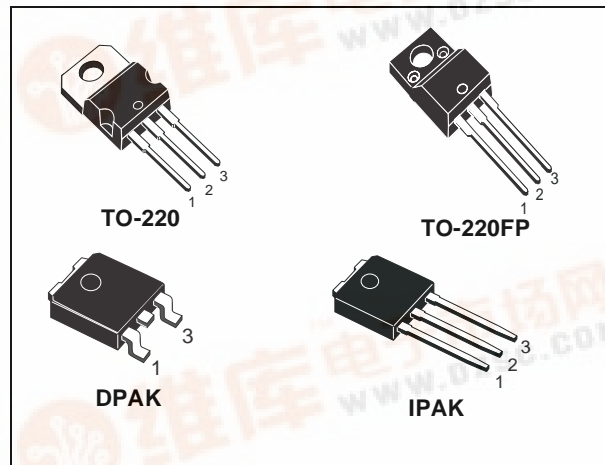


# STP4NK80Z - STP4NK80ZFP STD4NK80Z - STD4NK80Z-1

N-CHANNEL 800V - 3Ω - 3A TO-220/TO-220FP/DPAK/IPAK  
Zener-Protected SuperMESH™ Power MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STP4NK80Z	800 V	< 3.5 Ω	3 A	80 W
STP4NK80ZFP	800 V	< 3.5 Ω	3 A	25 W
STD4NK80Z	800 V	< 3.5 Ω	3 A	80 W
STD4NK80Z-1	800 V	< 3.5 Ω	3 A	80 W

- TYPICAL R<sub>DS(on)</sub> = 3 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY



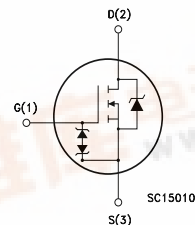
## DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

## APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC
- LIGHTING

## INTERNAL SCHEMATIC DIAGRAM



## ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP4NK80Z	P4NK80Z	TO-220	TUBE
STP4NK80ZFP	P4NK80ZFP	TO-220FP	TUBE
STD4NK80ZT4	D4NK80Z	DPAK	TAPE & REEL
STD4NK80Z-1	D4NK80Z	IPAK	TUBE



## STP4NK80Z - STP4NK80ZFP - STD4NK80Z - STD4NK80Z-1

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		STP4NK80Z	STP4NK80ZFP	STD4NK80Z STD4NK80Z-1	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	800			V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	800			V
V <sub>GS</sub>	Gate- source Voltage	± 30			V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	3	3 (*)	3	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	1.89	1.89 (*)	1.89	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	12	12 (*)	12	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	80	25	80	W
	Derating Factor	0.64	0.21	0.64	W/°C
V <sub>ESD(G-S)</sub>	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	3000			KV
dv/dt (1)	Peak Diode Recovery voltage slope	4.5			V/ns
V <sub>ISO</sub>	Insulation Withstand Voltage (DC)	-	2500	-	V
T <sub>j</sub> T <sub>stg</sub>	Operating Junction Temperature Storage Temperature	-55 to 150			°C

(●) Pulse width limited by safe operating area

(1) I<sub>SD</sub> ≤ 4A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

(\*) Limited only by maximum temperature allowed

### THERMAL DATA

		TO-220	TO-220FP	DPAK IPAK	
R <sub>thj-case</sub>	Thermal Resistance Junction-case Max	1.56	5	1.56	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient Max	62.5		100	°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose	300			°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	3	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	190	mJ

### GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV <sub>GSO</sub>	Gate-Source Breakdown Voltage	I <sub>gs</sub> = ± 1mA (Open Drain)	30			V

### PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## STP4NK80Z - STP4NK80ZFP - STD4NK80Z - STD4NK80Z-1

### ELECTRICAL CHARACTERISTICS (T<sub>CASE</sub> = 25°C UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	800			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 30V			±10	μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 50 μA	3	3.75	4.5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.5 A		3	3.5	Ω

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1.5 A		2.9		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0		575 67 13		pF pF pF
C <sub>oss eq.</sub> (3)	Equivalent Output Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 400 V		60		pF

### SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub> t <sub>r</sub>	Turn-on Delay Time Rise Time	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 1.5 A R <sub>G</sub> = 4.7Ω V <sub>GS</sub> = 10 V (Resistive Load see, Figure 3)		13 12		ns ns
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V <sub>DD</sub> = 640 V, I <sub>D</sub> = 3 A, V <sub>GS</sub> = 10V		22.5 4.2 11.3		nC nC nC

### SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>d(off)</sub> t <sub>f</sub>	Turn-off Delay Time Fall Time	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 1.5 A R <sub>G</sub> = 4.7Ω V <sub>GS</sub> = 10 V (Resistive Load see, Figure 3)		35 32		ns ns
t <sub>r(Voff)</sub> t <sub>f</sub> t <sub>c</sub>	Off-voltage Rise Time Fall Time Cross-over Time	V <sub>DD</sub> = 640 V, I <sub>D</sub> = 3 A, R <sub>G</sub> = 4.7Ω, V <sub>GS</sub> = 10 V (Inductive Load see, Figure 5)		18 7.5 25		ns ns ns

### SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I <sub>SD</sub> I <sub>SDM</sub> (2)	Source-drain Current Source-drain Current (pulsed)				3 12	A A
V <sub>SD</sub> (1)	Forward On Voltage	I <sub>SD</sub> = 3 A, V <sub>GS</sub> = 0			1.6	V
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I <sub>SD</sub> = 3 A, di/dt = 100 A/μs V <sub>DD</sub> = 80 V, T <sub>j</sub> = 150°C (see test circuit, Figure 5)		400 1520 7.6		ns nC A

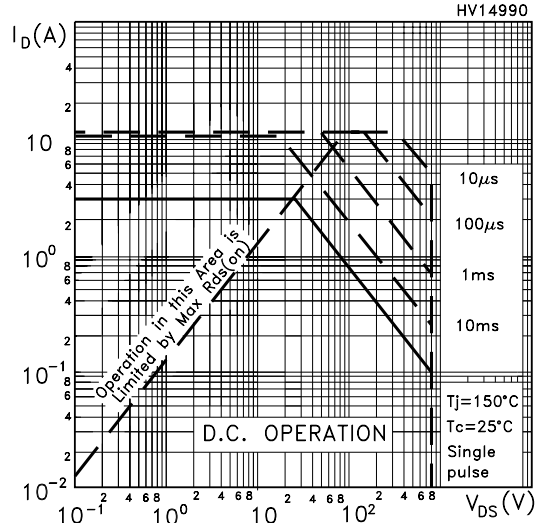
Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

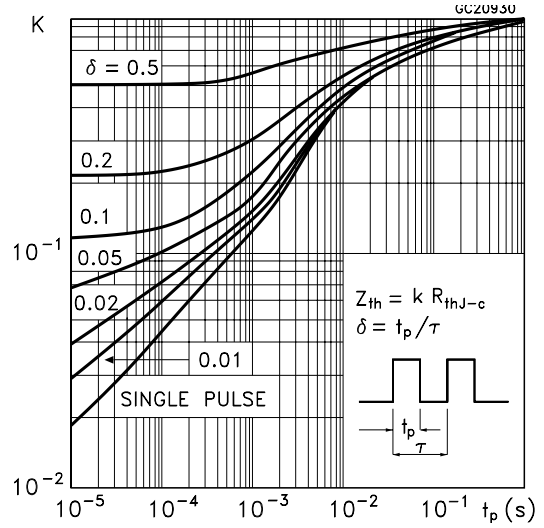
3. C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>.

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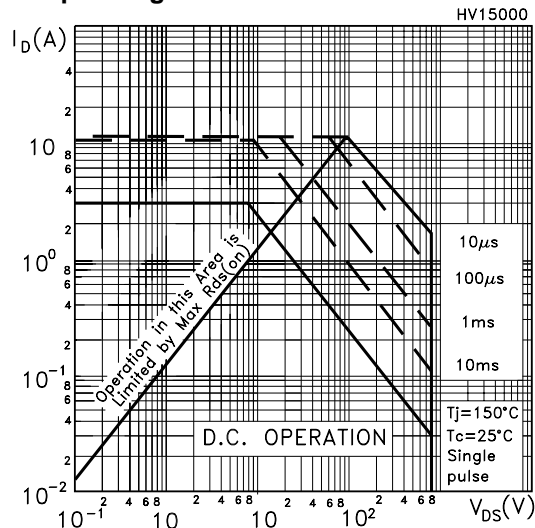
**Safe Operating Area For TO-220/DPAK/IPAK**



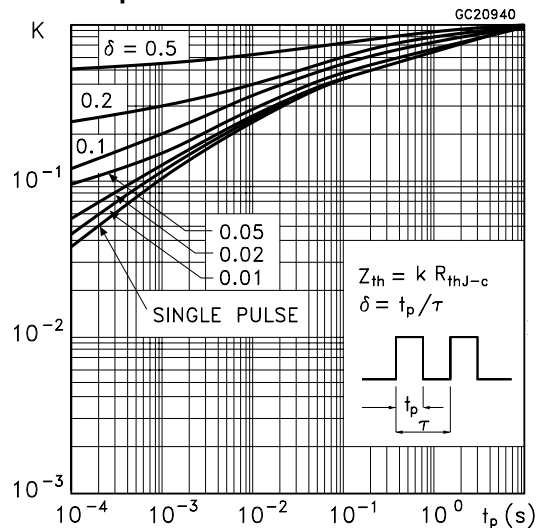
**Thermal Impedance For TO-220/DPAK/IPAK**



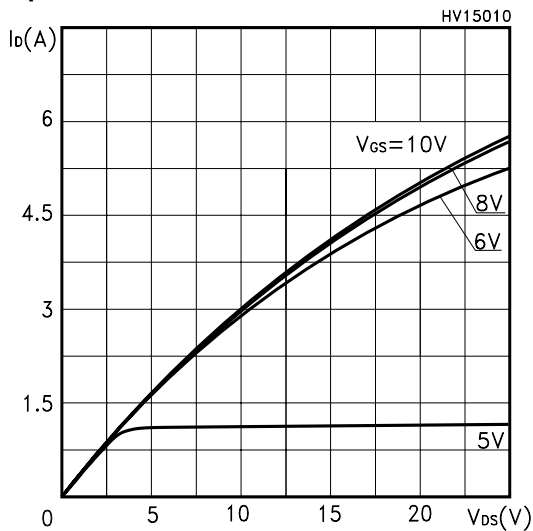
**Safe Operating Area For TO-220FP**



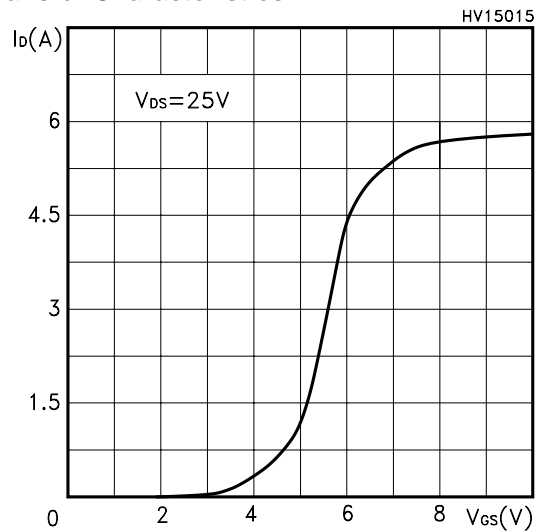
**Thermal Impedance For TO-220FP**



**Output Characteristics**

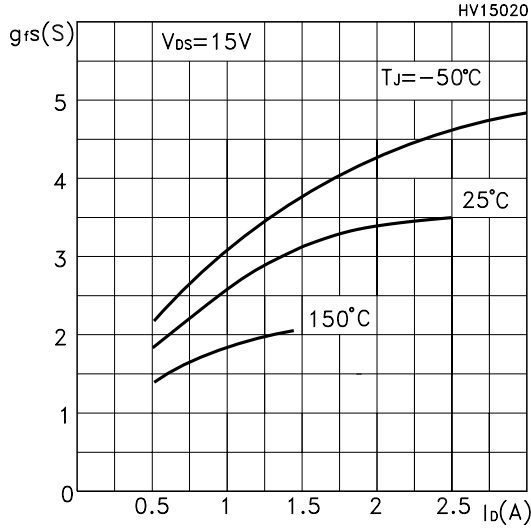


**Transfer Characteristics**

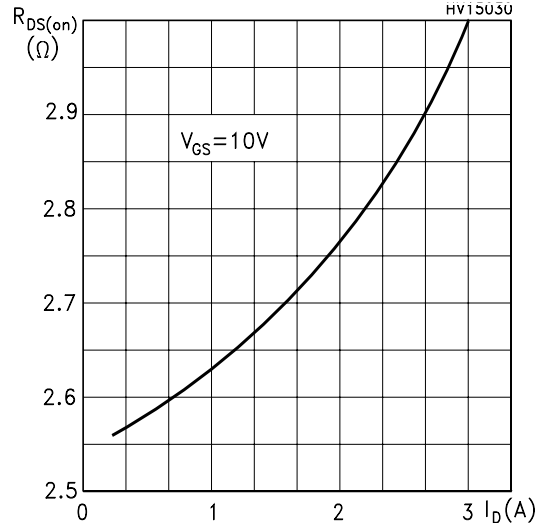


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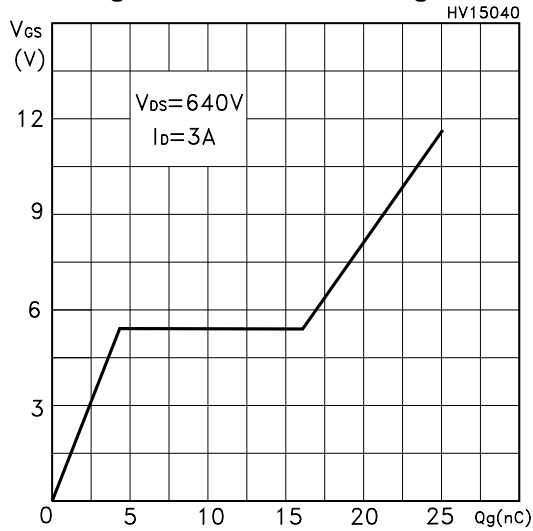
Transconductance



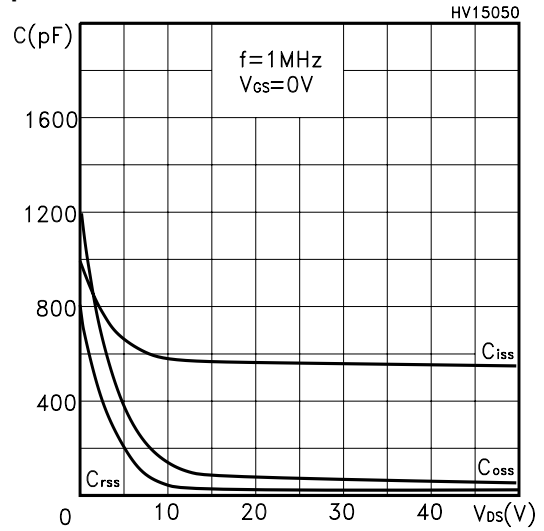
Static Drain-source On Resistance



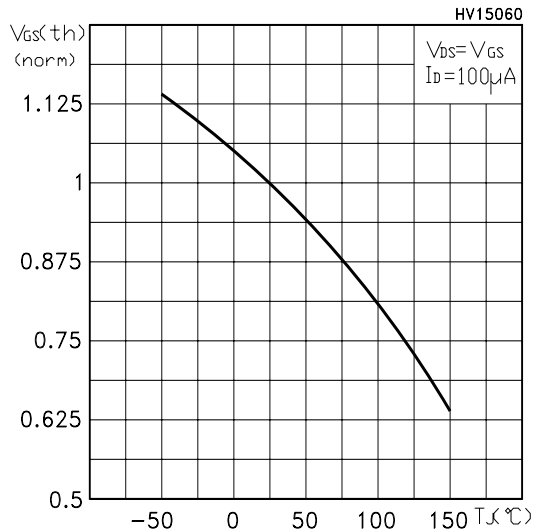
Gate Charge vs Gate-source Voltage



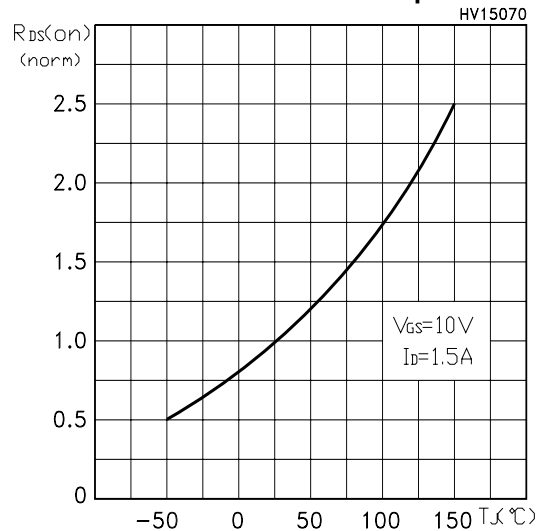
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.

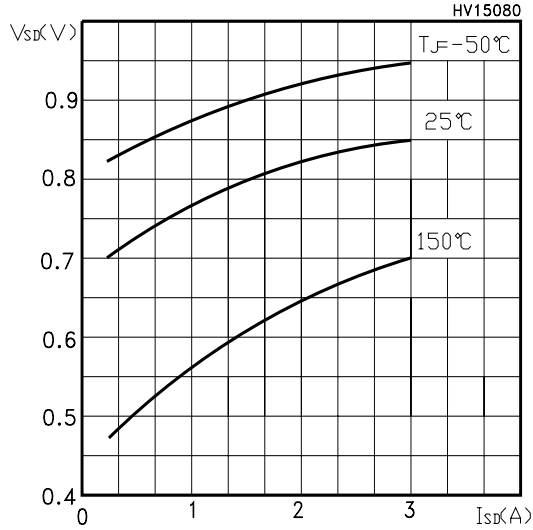


Normalized On Resistance vs Temperature

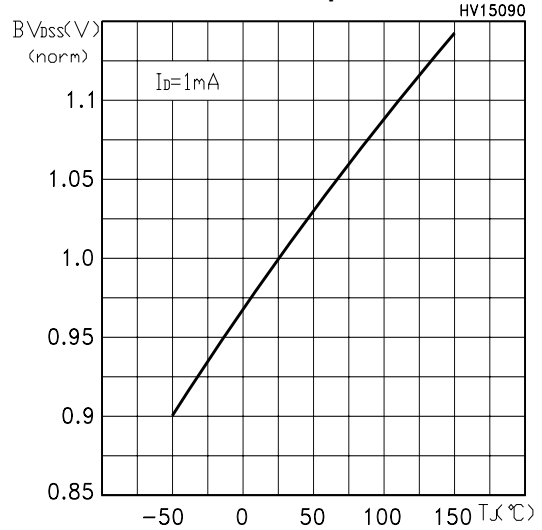


**STP4NK80Z - STP4NK80ZFP - STD4NK80Z - STD4NK80Z-1**

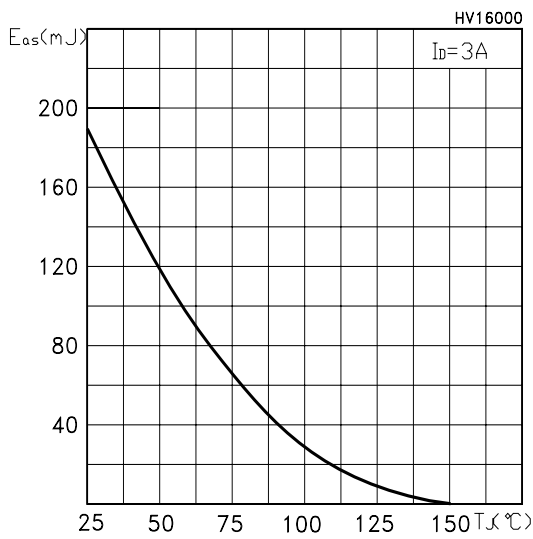
**Source-drain Diode Forward Characteristics**



**Normalized BVDSS vs Temperature**



**Maximum Avalanche Energy vs Temperature**



STP4NK80Z - STP4NK80ZFP - STD4NK80Z - STD4NK80Z-1

Fig. 1: Unclamped Inductive Load Test Circuit

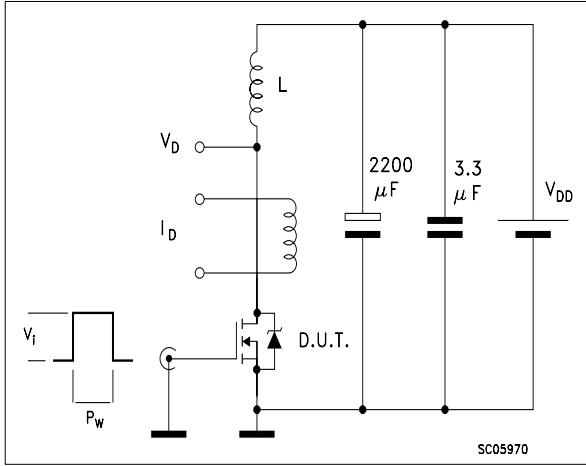


Fig. 2: Unclamped Inductive Waveform

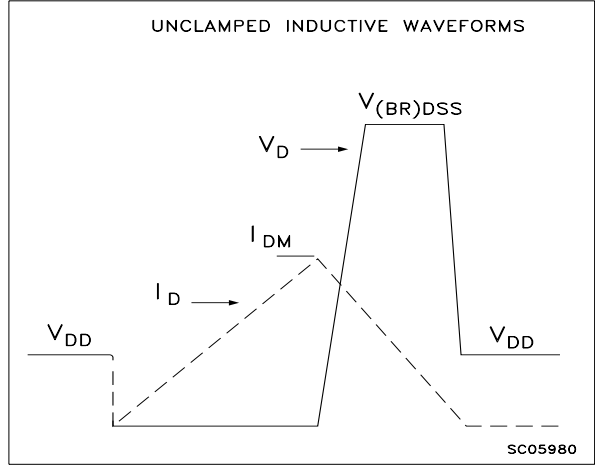


Fig. 3: Switching Times Test Circuit For Resistive Load

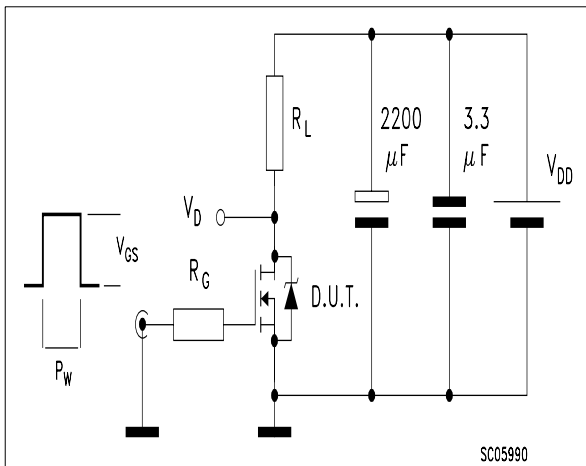


Fig. 4: Gate Charge test Circuit

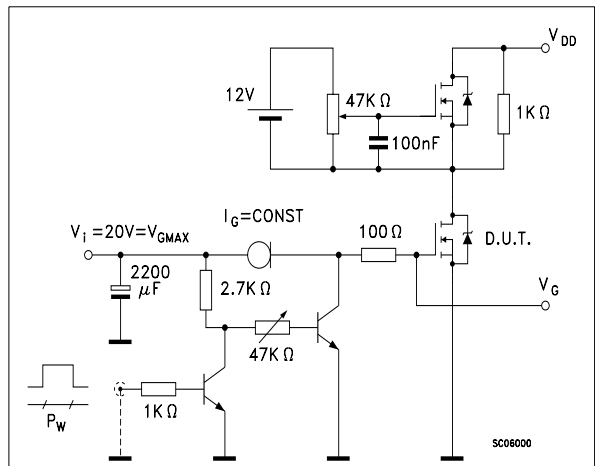
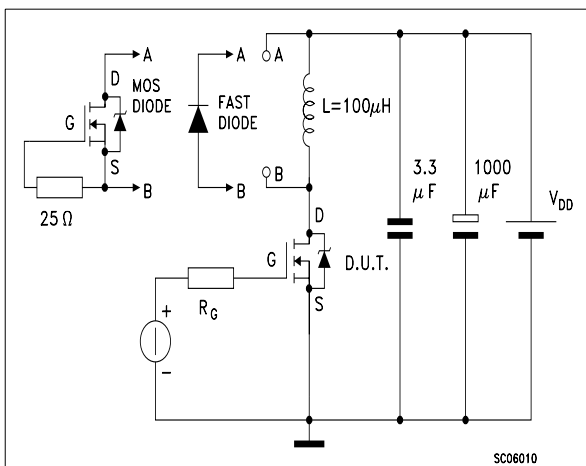


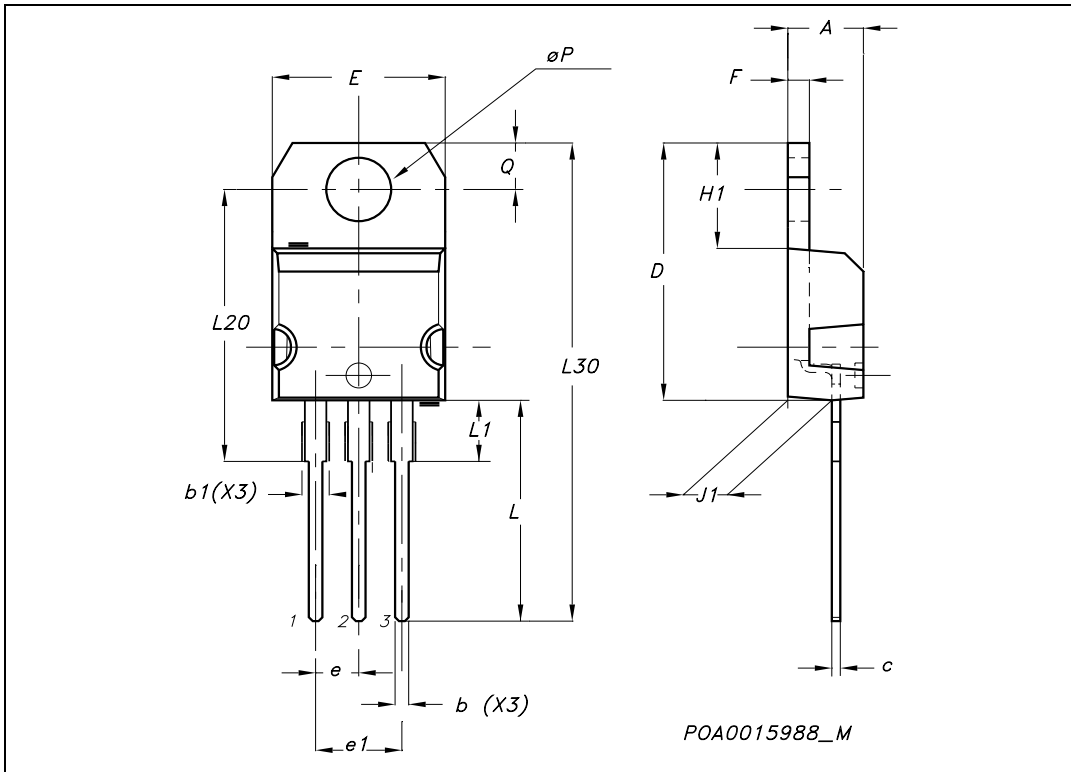
Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



**STP4NK80Z - STP4NK80ZFP - STD4NK80Z - STD4NK80Z-1**

**TO-220 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116

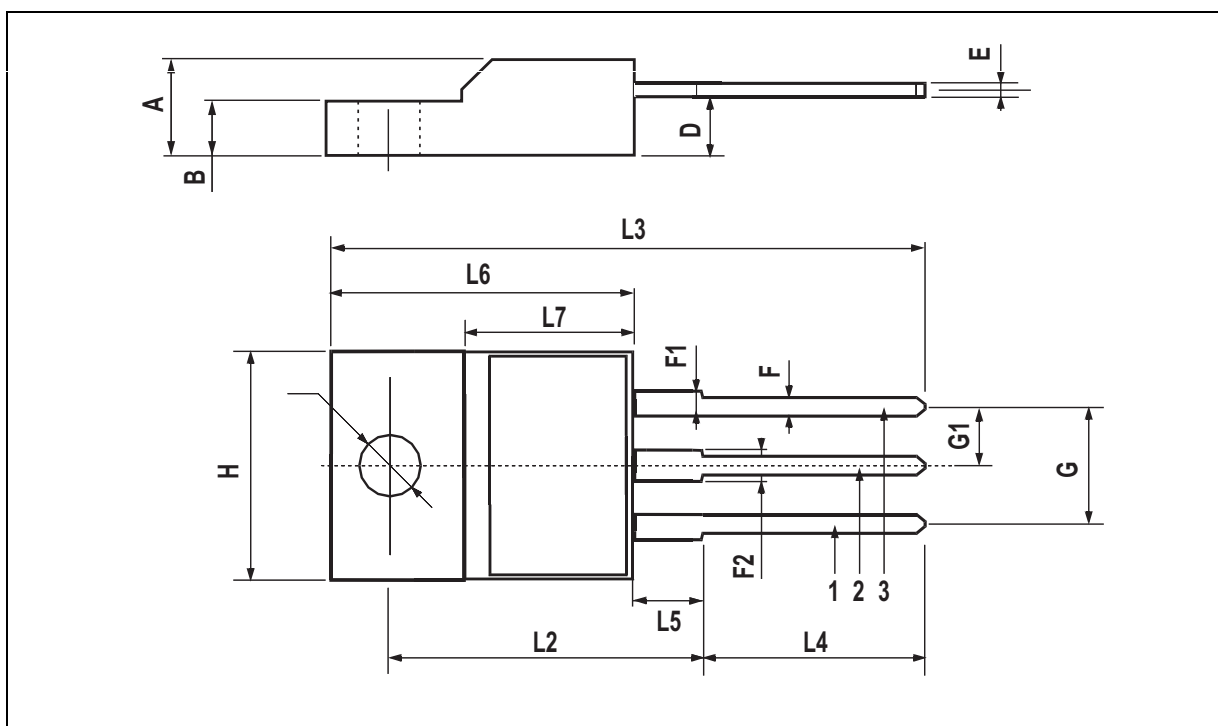




STP4NK80Z - STP4NK80ZFP - STD4NK80Z - STD4NK80Z-1

TO-220FP MECHANICAL DATA

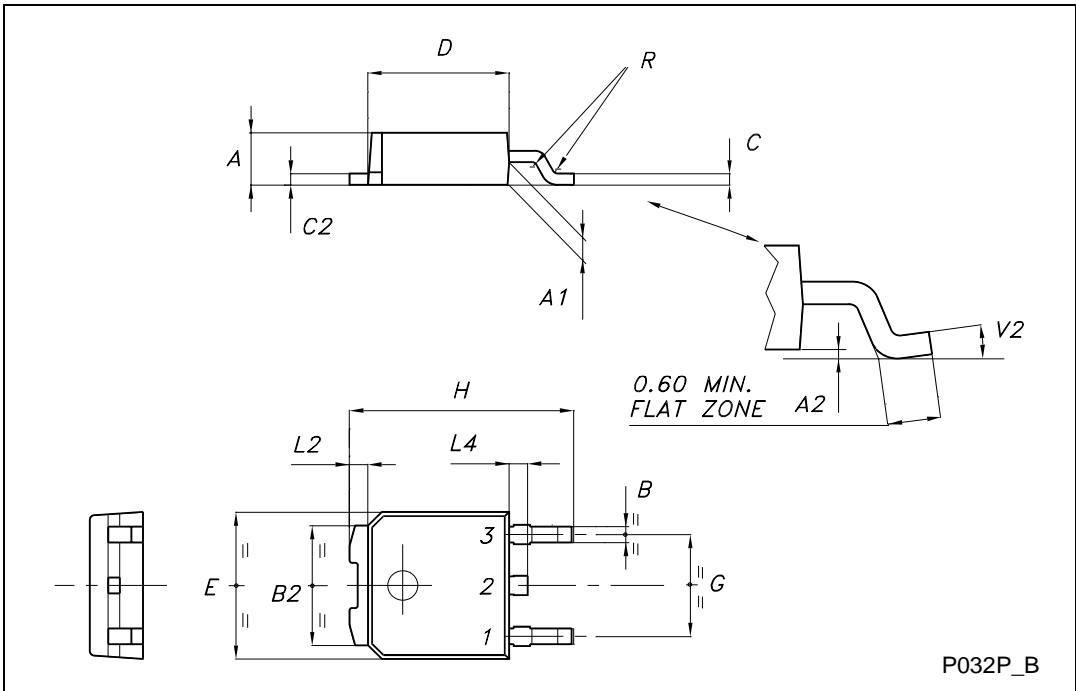
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.5	0.045		0.067
F2	1.15		1.5	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



**STP4NK80Z - STP4NK80ZFP - STD4NK80Z - STD4NK80Z-1**

**TO-252 (DPAK) MECHANICAL DATA**

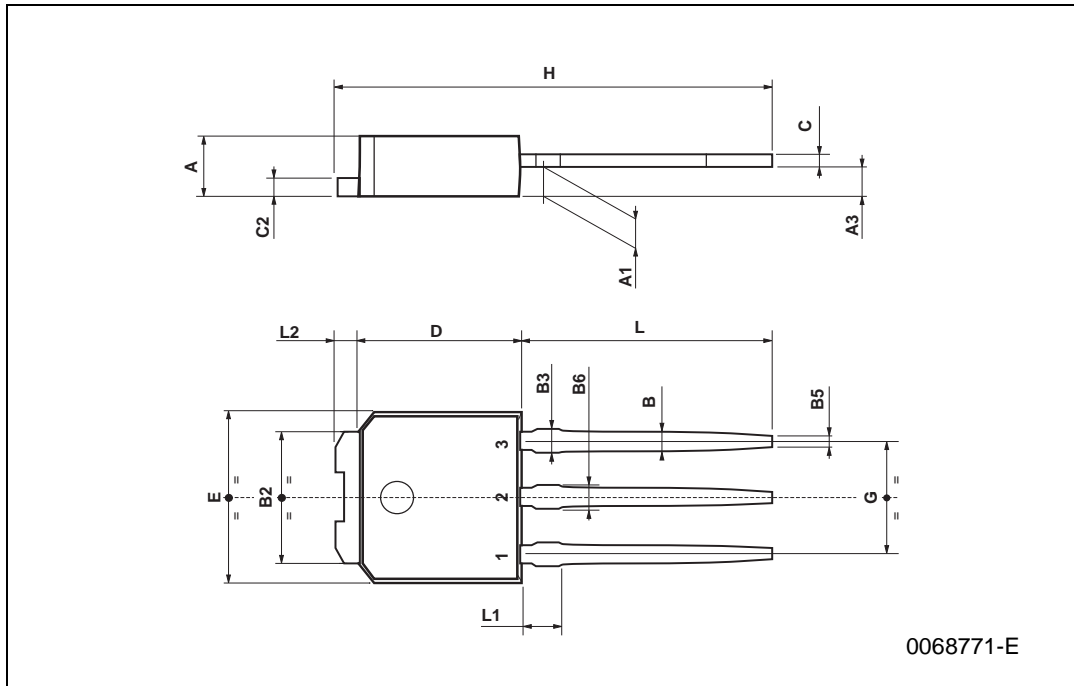
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



**STP4NK80Z - STP4NK80ZFP - STD4NK80Z - STD4NK80Z-1**

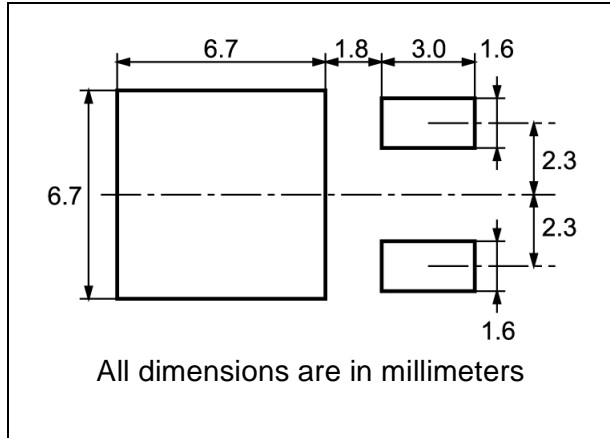
**TO-251 (IPAK) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039

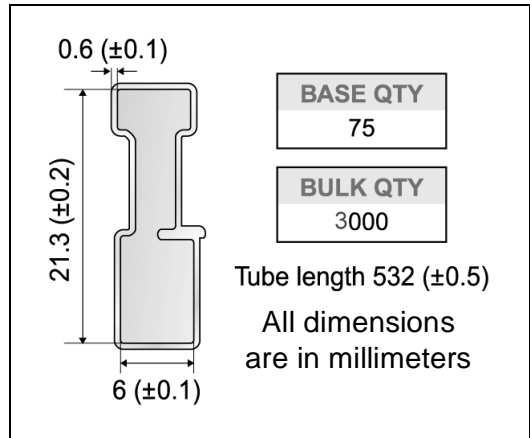


**STP4NK80Z - STP4NK80ZFP - STD4NK80Z - STD4NK80Z-1**

**DPAK FOOTPRINT**



**TUBE SHIPMENT (no suffix)\***



**TAPE AND REEL SHIPMENT (suffix "T4")\***

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

G measured at hub

**REEL MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

**TAPE MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

TOP COVER TAPE

10 pitches cumulative tolerance on tape +/- 0.2 mm

Center line of cavity

User Direction of Feed

Bending radius R min.

FEED DIRECTION

For machine ref. only including draft and radii concentric around B0

\* on sales type

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