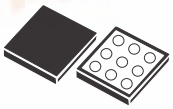
STG3685

LOW VOLTAGE 0.5Ω MAX DUAL SPDT SWITCH, SINGLE ENABLE WITH BREAK BEFORE MAKE FEATURE

PRELIMINARY DATA

- HIGH SPEED:
  t_{PD} = 0.3ns (TYP.) at V_{CC} = 3.0V
  t_{PD} = 0.4ns (TYP.) at V_{CC} = 2.3V
- ULTRA LOW POWER DISSIPATION:
  I_{CC} = 0.2µA (MAX.) at T_A = 85°C
- LOW "ON" RESISTANCE V_I = 0V:
  R_{ON} = 0.4Ω (MAX. T_A = 25°C) at V_{CC} = 4.2V
  R_{ON} = 0.5Ω (MAX. T_A = 25°C) at V_{CC} = 3.0V
  R_{ON} = 0.6Ω (MAX. T_A = 25°C) at V_{CC} = 2.3V
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 1.4V to 4.3V SINGLE SUPPLY
- 4.3V TOLERANT AND 1.8V COMPATIBLE THRESHOLD ON DIGITAL CONTROL INPUT at V_{CC} = 2.3 to 4.3V
- LATCH-UP PERFORMANCE EXCEEDS 300mA (JESD 17)
- ESD PERFORM. (ANALOG CHAN. vs GND): HBM > 4KV (MIL STD 883 method 3015)



Flip-Chip

Table 1: Order Codes

PACKAGE	T & R
Flip-Chip9	STG3685BJR

DESCRIPTION

The STG3685 is an high-speed CMOS DUAL ANALOG S.P.D.T. (Single Pole Dual Throw) SWITCH or DUAL 2:1 Multiplexer/Demultiplexer Bus Switch fabricated in silicon gate C^2MOS technology. It is designed to operate from 1.4V to 4.3V, making this device ideal for portable applications.

It offers very low ON-Resistance (<0.5Ω) at V_{CC}=3.0V. The IN input is provided to control the switches. The switches nS1 are ON (they are connected to common Ports Dn) when the IN input is held high and OFF (high impedance state exists between the two ports) when IN is held low; the switches nS2 are ON (they are connected to common Ports Dn) when the IN input is held low and OFF (high impedance state exists between the two ports) when IN is held high. Additional key features are fast switching speed, Break Before Make Delay Time and Ultra Low Power Consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage. It's available in the commercial temperature range Flip-chip package with Epoxy Protection.

Figure 1: Pin Connection (Top Through View) **And Schematic Circuit**

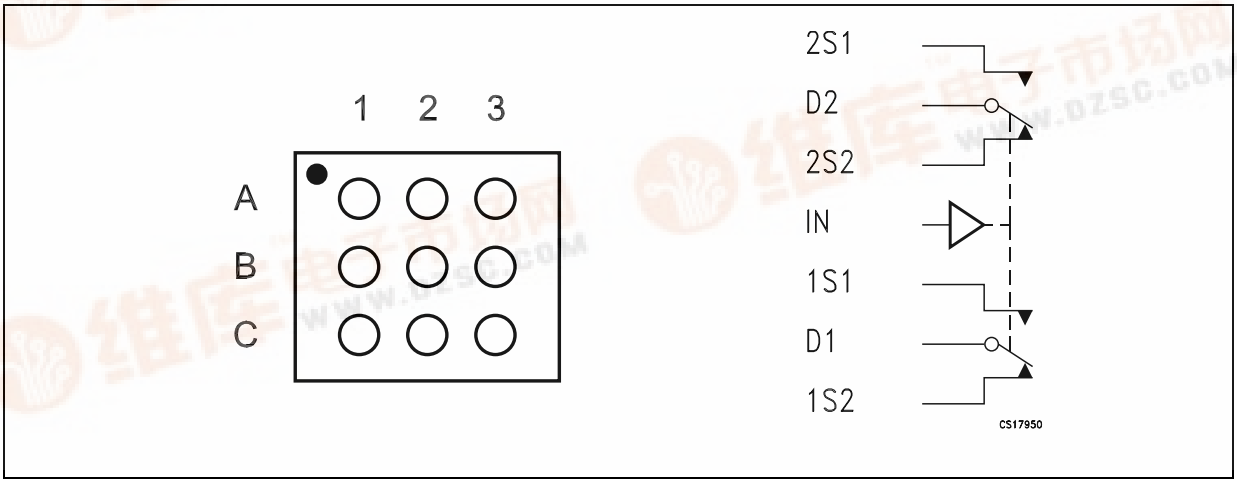


Figure 2: Input Equivalent Circuit

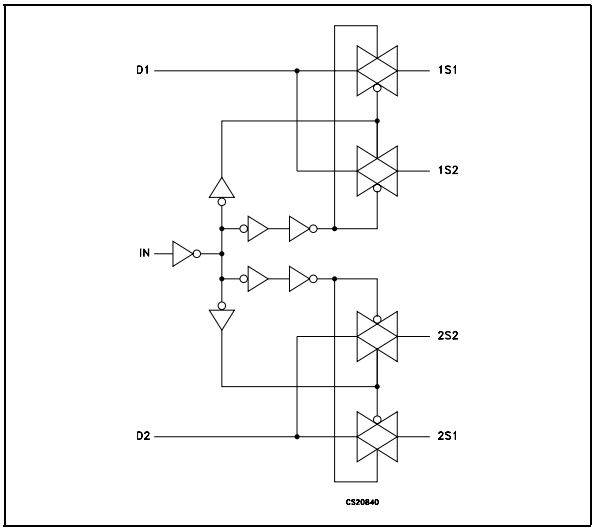


Table 2: Pin Description

PIN N°	SYMBOL	NAME AND FUNCTION
B2	IN	Control
A3, A1 C3, C1	2S1, 1S1 2S2, 1S2	Independent Channels
B3, B1	D2, D1	Common Channels
C2	GND	Ground (0V)
A2	V_{CC}	Positive Supply Voltage

Table 3: Truth Table

IN	SWITCH S1	SWITCH S2
H	ON	OFF(*)
L	OFF(*)	ON

(*) High Impedance

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 4.6	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_{IC}	DC Control Input Voltage	-0.5 to 4.6	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IKC}	DC Input Diode Current on control pin (V_{IN} < 0V)	– 50	mA
I_{IK}	DC Input Diode Current (V_{IN} < 0V)	± 50	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 300	mA
I_{OP}	DC Output Current Peak (pulse at 1ms, 10% duty cycle)	± 500	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 100	mA
P_D	Power Dissipation at T_a=70°C (1)	TBD	mW
T_{stg}	Storage Temperature	-65 to 150	°C
T_L	Lead Temperature (10 sec)	260	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
(1) Derate above 70°C: by 18.5mW/°C.

Table 5: Recommended Operating Conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage (note 1)		1.4 to 4.3	V
V_I	Input Voltage		0 to V_{CC}	V
V_{IC}	Control Input Voltage		0 to 4.3	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
dt/dv	Input Rise and Fall Time Control Input	V_{CC}= 1.4V to 2.7V	0 to 20	ns/V
		V_{CC}= 3.0V to 3.6V	0 to 10	

1) Truth Table guaranteed: 1.2V to 4.3V.

Table 6: DC Specifications

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	1.65-1.95		0.65V_{CC}			0.65V_{CC}		0.65V_{CC}		V
		2.3-2.5		1.4			1.4		1.4		
		2.7-3.0		1.4			1.4		1.4		
		3.3		1.5			1.5		1.5		
		3.6		1.6			1.6		1.6		
		4.3		1.6			1.6		1.6		
V_{IL}	Low Level Input Voltage	1.65-1.95				0.40		0.40		0.40	V
		2.3-2.5				0.50		0.50		0.50	
		2.7-3.6				0.50		0.50		0.50	
		3.3				0.50		0.50		0.50	
		3.6				0.50		0.50		0.50	
		4.3				0.50		0.50		0.50	
R_{ON}	Switch ON Resistance (See Fig. 12)	4.3	V_S=0V to V_{CC} I_S=100mA		250	400		500			mΩ
		3.0			300	500		600			
		2.7			300	500		600			
		2.3			350	600		800			
		1.8			550	2000		4000			
		1.4			1200	2500		5000			
R_{FLAT}	ON Resistance FLATNESS (1)	4.3	V_S=0 to V_{CC} I_S=100mA								Ω
		3.0									
		2.7			0.07	0.15		0.15			
		2.3									
		1.65									
I_{OFF}	OFF State Leakage Current (nSn), (Dn)	4.3	V_S=0.3 or 4V			±10		± 100			nA
I_{IN}	Input Leakage Current	0 - 4.3	V_{IN}=0 to 4.3V			±0.1		± 1			µA
I_{CCL}	Quiescent Supply Current	1.65-4.3	V_{IN}=V_{CC} or GND			±0.05		±0.2		±1	µA
I_{CCH}	Quiescent Supply Current	4.2	V_{IN}=1.65V		415	500					µA
			V_{IN}=1.8V		360	400					
			V_{IN}=2.6V		120	150					

Note 1: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 7: AC Electrical Characteristics (C_L = 35pF, R_L = 50Ω, $t_r = t_f \leq 5$ns)

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay	1.65-1.95			0.45						ns
		2.3-2.7			0.40						
		3.0-3.6			0.30						
		3.6-4.3			0.30						
t_{ON}	TURN-ON time	1.65-1.95	V_S=0.8V		70						ns
		2.3-2.7	V_S=1.5V		32	50		60			
		3.0-3.6			32	50		60			
		3.6-4.3			30	50		60			
t_{OFF}	TURN-OFF time	1.65-1.95	V_S=0.8V		45						ns
		2.3-2.7	V_S=1.5V		25	30		40			
		3.0-3.6			15	30		40			
		3.6-4.3			15	30		40			
t_D	Break Before Make Time Delay	1.65-1.95	C_L=35pF, R_L= 50Ω, V_S=1.5V								ns
		2.3-2.7		2	15						
		3.0-3.6		2	15						
		3.6-4.3		2	15						
Q	Charge injection	1.65-1.95	C_L= 100pF, R_L= 1MΩ, V_{GEN}= 0V, R_{GEN}= 0Ω		50						pC
		2.3-2.7			40						
		3.0-3.6			35						
		3.6-4.3			35						

Table 8: Analog Switch Characteristics (C_L = 5pF, R_L = 50Ω, T_A = 25°C)

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
OIRR	Off Isolation (1)	1.65-4.3	V_S= 1V_{RMS} f= 100KHz		-64						dB
Xtalk	Crosstalk	1.65-4.3	V_S= 1V_{RMS} f= 100KHz		-32						dB
THD	Total Harmonic Distortion	2.3-4.3	R_L= 600Ω, V_I= 2V_{PP}, f = 20Hz to 20kHz		0.03						%
BW	-3dB Bandwidth	1.65-4.3	R_L= 50Ω		50						MHz
C_{IN}	Control Pin Input Capacitance				10						pF
C_{Sn}	Sn Port Capacitance	3.3	f = 1MHz		35						
C_D	D Port Capacitance when Switch is Enabled	3.3	f = 1MHz		91						

Note 1: Off Isolation = 20Log_{10} (V_D/V_S), V_D = output. V_S = input at off switch.

Figure 3: On Resistance

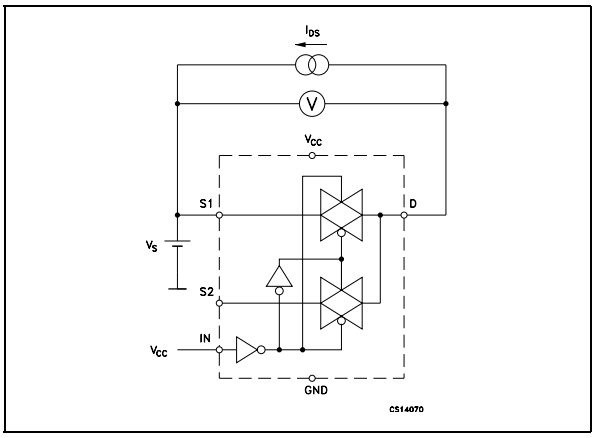


Figure 4: Off Leakage

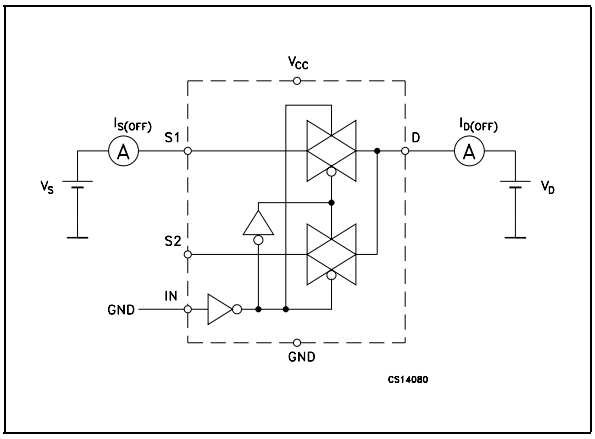


Figure 5: Off Isolation

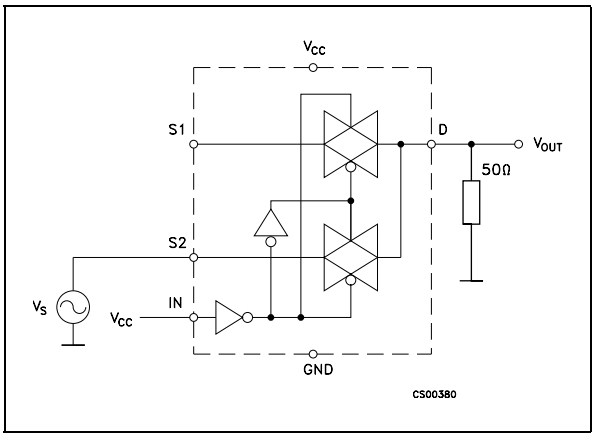


Figure 6: Bandwidth

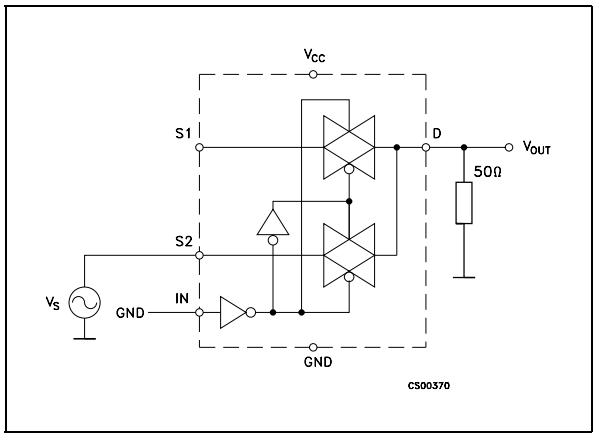


Figure 7: Channel To Channel Crosstalk

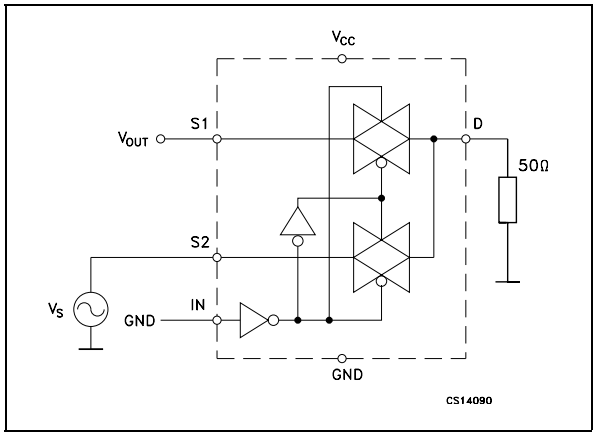
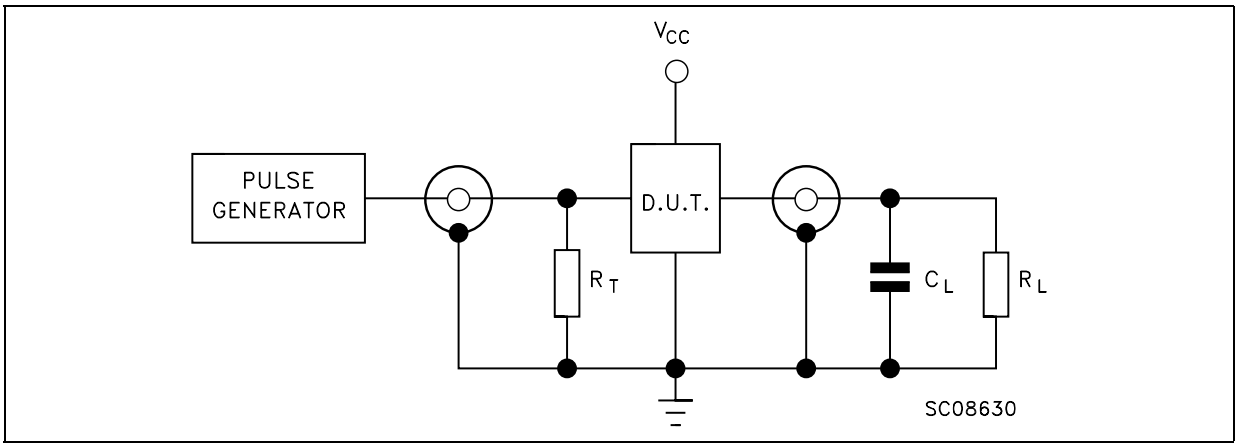


Figure 8: Test Circuit



C_L = 5/35pF or equivalent (includes jig and probe capacitance)
R_L = 50Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 9: Break Before Make Time Delay

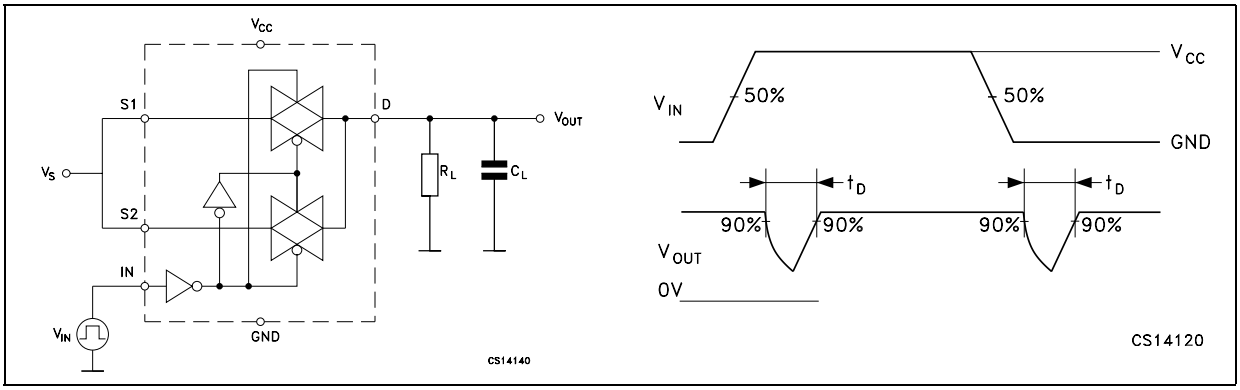


Figure 10: Charge Injection (V_{GEN} = 0V, R_{GEN} = 0Ω, R_L = 1MΩ, C_L = 100pF)

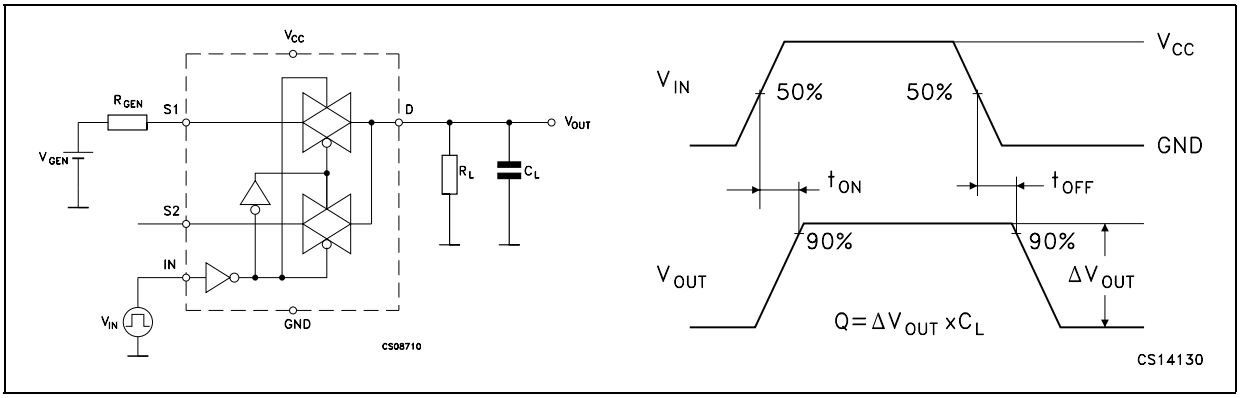
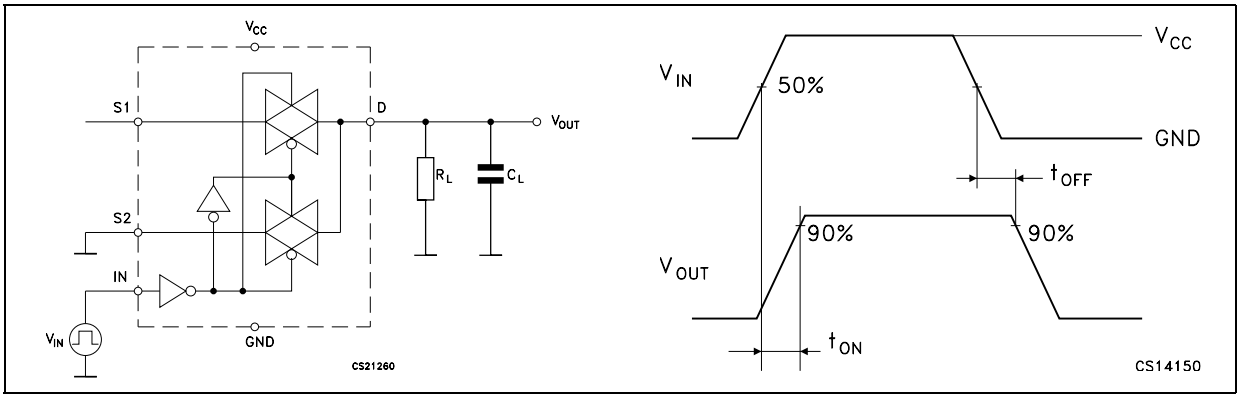
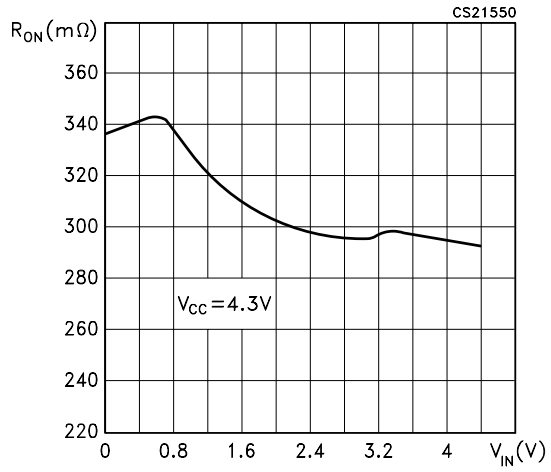


Figure 11: Turn On, Turn Off Delay Time



TYPICAL CHARACTERISTICS

Figure 12: Switch-On R_{ON} vs V_{IN}



Flip-Chip9 MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.59	1.64	1.69	62.6	64.6	66.5
B	1.42	1.47	1.52	55.9	57.9	59.8
C			0.80			31.5
D	0.295	0.32	0.345	11.6	12.6	13.6
E		0.5			19.7	
F	0.35	0.40	0.45	13.8	15.7	17.7
G		0.25			9.8	
H	0.061	0.0635	0.066	2.4	2.5	2.6

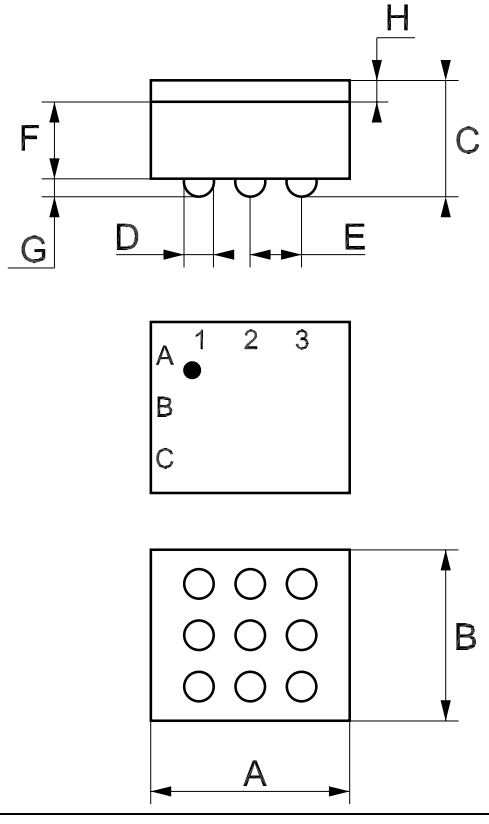


Table 9: Revision History

Date	Revision	Description of Changes
13-Jan-2005	1	First Release.
04-Jul-2005	2	The Q Values on Table 7 has been updated.