



STL35NF3LL

N-CHANNEL 30V - 0.0055Ω - 35A PowerFLAT™
LOW GATE CHARGE STripFET™ MOSFET

TARGET DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STL35NF3LL	30 V	< 0.007 Ω	35 A

- TYPICAL R_{DS(on)} = 0.0055Ω
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE

DESCRIPTION

This Power MOSFET is the second generation of STMicroelectronics unique "STripFET™" technology. The resulting transistor shows extremely low on-resistance and minimal gate charge. The new PowerFLAT™ package allows a significant reduction in board space without compromising performance.

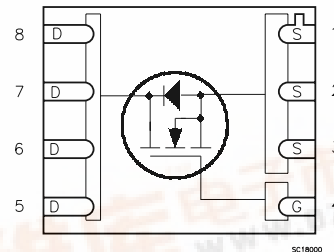
APPLICATIONS

- DC-DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT



PowerFLAT™ (6x5)
(Chip Scale Package)

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	30	V
V _{GS}	Gate- source Voltage	± 15	V
I _D (#)	Drain Current (continuous) at T _C = 25°C Drain Current (continuous) at T _C = 100°C	35 22	A A
I _{DM} (●)	Drain Current (pulsed)	140	A
P _{TOT}	Total Dissipation at T _C = 25°C	80	W
	Derating Factor	0.64	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	TBD	V/ns
E _{AS} (2)	Single Pulse Avalanche Energy	TBD	J
T _{stg}	Storage Temperature	-55 to 150	°C
T _j	Max. Operating Junction Temperature		

(●) Pulse width limited by safe operating area

(#) Limited by Wire Bonding

(1) I_{SD} < 35A, di/dt < 300A/μs, V_{DD} < V(BR)DSS, T_J < T_{JMAX}

(2) Starting T_j = 25°C, I_D = 30A, V_{DD} = 27.5V

STL35NF3LL

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1.56	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	50	°C/W

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 15V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250µA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 17.5 A V _{GS} = 4.5 V, I _D = 17.5A		0.0055 0.007	0.007 0.010	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 17.5 A		TBD		S
C _{iss}	Input Capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		2650		pF
C _{oss}	Output Capacitance			900		pF
C _{rss}	Reverse Transfer Capacitance			150		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 17.5\text{ A}$		TBD		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 3)		TBD		ns
Q_g	Total Gate Charge	$V_{DD} = 15\text{ V}$, $I_D = 35\text{ A}$,		80		nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 10\text{ V}$		TBD		nC
Q_{gd}	Gate-Drain Charge			TBD		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 17.5\text{ A}$,		TBD		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 3)		TBD		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				35	A
I_{SDM} (1)	Source-drain Current (pulsed)				140	A
V_{SD} (2)	Forward On Voltage	$I_{SD} = 35\text{ A}$, $V_{GS} = 0$			1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 35\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,		TBD		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 30\text{ V}$, $T_j = 150^\circ\text{C}$		TBD		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		TBD		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

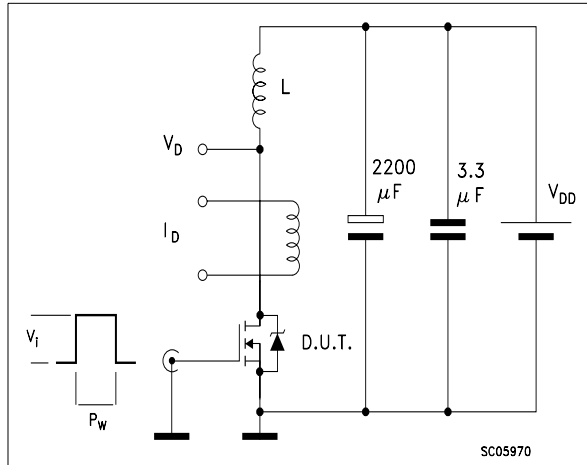


Fig. 2: Unclamped Inductive Waveform

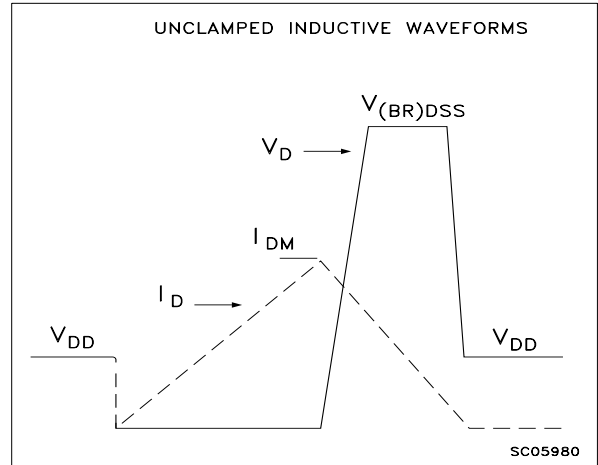


Fig. 3: Switching Times Test Circuit For Resistive Load

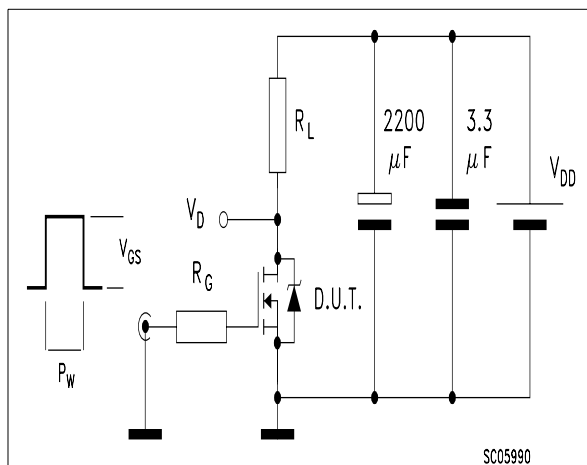


Fig. 4: Gate Charge test Circuit

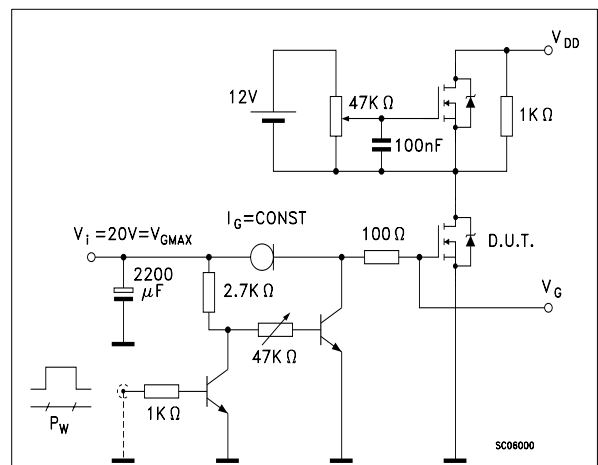
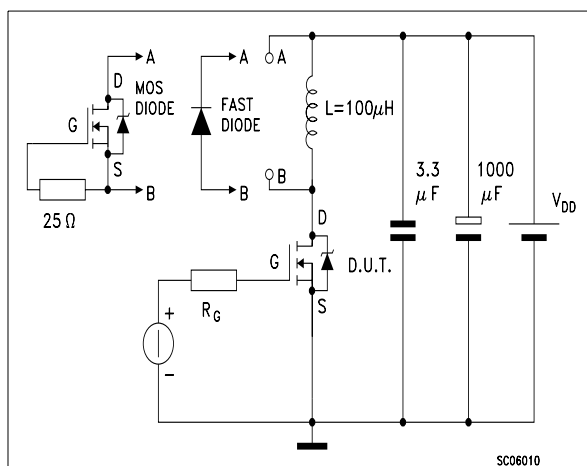
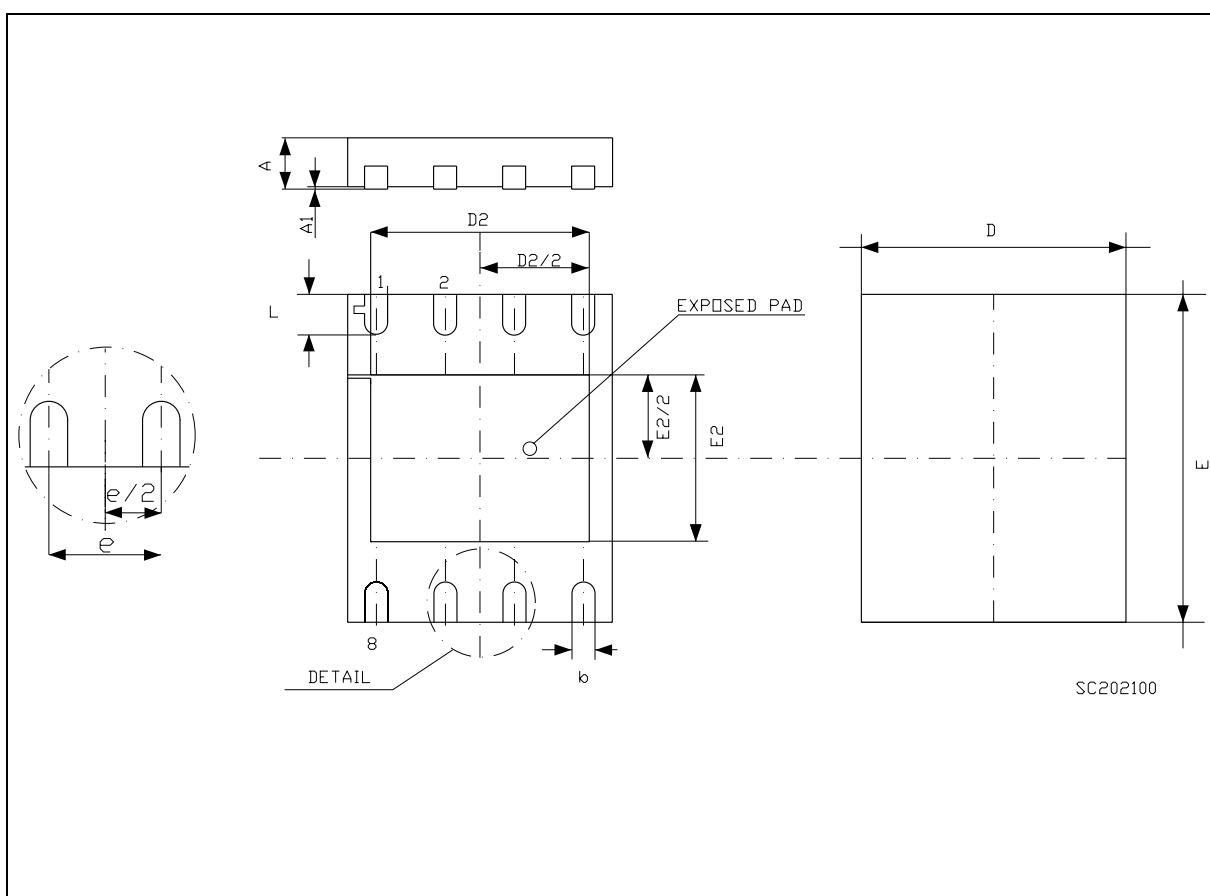


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



PowerFLAT™(6x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80		1.00	0.031		0.039
A1		0.08			0.003	
b	0.36		0.48	0.014		0.018
D		4.89			0.191	
D2	3.95		4.05	0.154		0.158
E		6.00			0.235	
E2	2.95		3.05	0.115		0.119
e		1.27			0.049	
L	0.65		0.85	0.025		0.033



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2001 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>