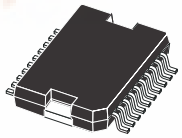
STLC1

LED LAMPS CLUSTER DRIVER

- FULLY MONOLITHIC FIXED FREQUENCY SMPS
- THREE LOW SIDE DRIVERS FOR STOP TAIL AND TURN LED LAMPS ARRAYS DRIVING
- PROGRAMMABLE LOW SIDE DRIVER OVER CURRENT LIMIT PROTECTION
- UNDER CURRENT DIAGNOSTIC
- INPUT OVERVOLTAGE PROTECTION
- VERY LOW STAND-BY CURRENT
- THERMAL PROTECTION WITH HYSTERESIS



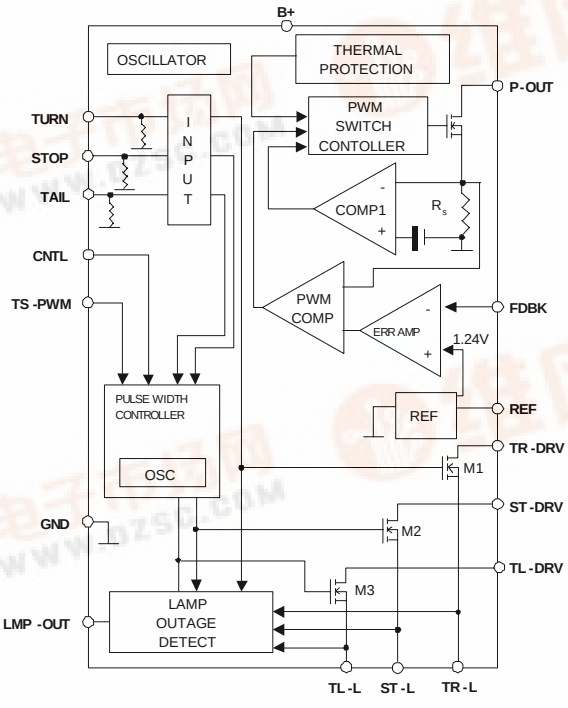
PowerSO-20™

DESCRIPTION

The STLC1, a device realized with the well established BCD technology, is a fixed frequency fully monolithic SMPS, with three independent smart low side driver, primarily intended for automotive rear led lamps driving.

The output voltage is set using a simple resistor divider. Thermal shutdown with hysteresis, input over-voltage and overcurrent protections give robust design solutions.

SCHEMATIC DIAGRAM



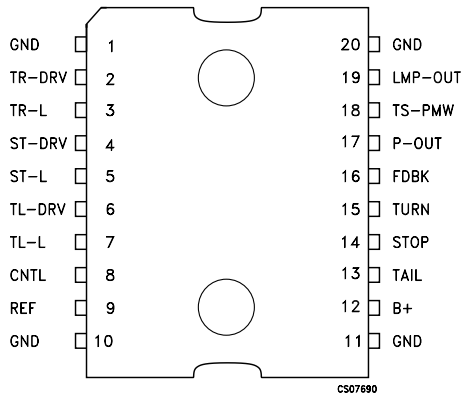
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{B+}	Transient Supply Voltage (load dump)	60	V
V_{B+}	Operating Supply Voltage	24	V
V_{TURN}, V_{STOP}, V_{TAIL}	TURN, STOP and TAIL input pins voltage	V_{B+} + 0.3	V
I_{TURN}, I_{STOP}, I_{TAIL}	TURN, STOP and TAIL pins current	± 10	mA
I_{TR-DRV}, I_{TL-DRV}, I_{ST-DRV}	TR-DRV, TL-DRV and ST-DRV pins sink current	1.5	A
$I_{LMP-OUT}$	LMP-OUT pin sink current	120	mA
V_{P-OUT}	P-OUT DC Voltage	60	V
I_{P-OUT}	P-OUT pin sink current	Internally Limited	A
T_{stg}	Storage Temperature Range	-55 to +150	°C
T_J	Operating Junction Temperature Range	-40 to +125	°C

THERMAL DATA

Symbol	Parameter	PowerSO-20™	Unit
$R_{thj-case}$	Thermal Resistance Junction-case	2	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-Ambient	50	°C/W

CONNECTION DIAGRAM (top view)



PowerSO-20™

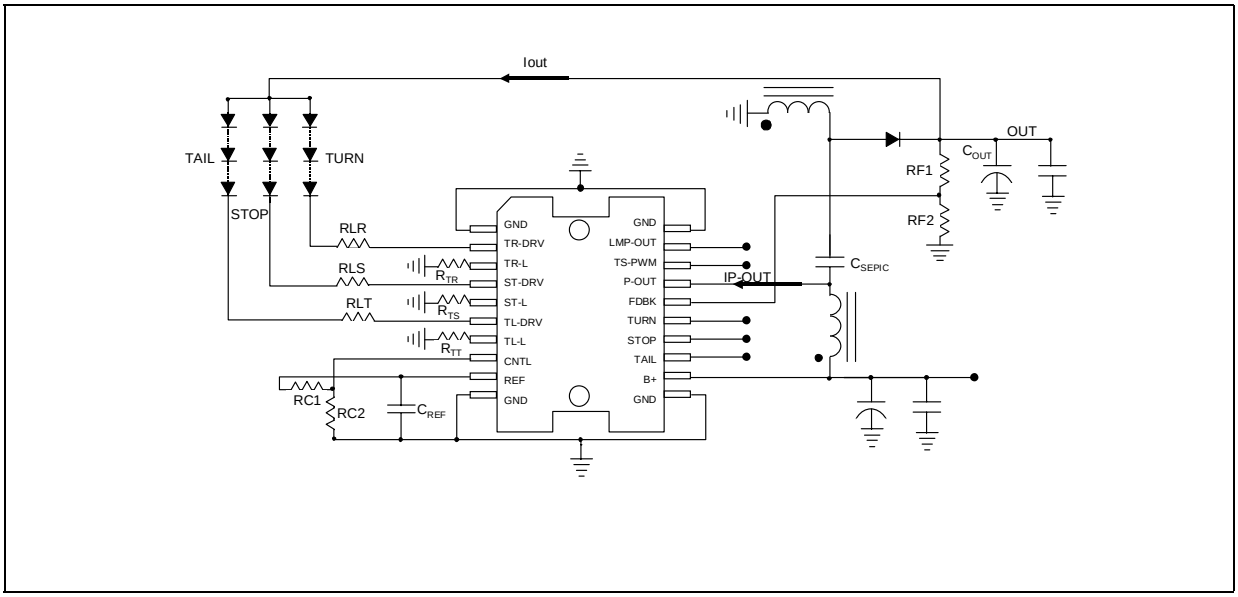
PIN DESCRIPTION

Pin N°	Symbol	Name and Function
1	GND	Ground
2	TR-DRV	The Low Side Driver drain pin for the TURN LED array
3	TR-L	The Low Side Driver source pin, used to detect either a lamp outage or an over-current condition for the TURN LED array
4	ST-DRV	The Low Side Driver drain pin for the STOP LED array
5	ST-L	The Low Side Driver source pin, used to detect either a lamp outage or an over-current condition for the STOP LED array
6	TL-DRV	The Low Side Driver drain pin for the TAIL LED array
7	TL-L	The Low Side Driver source pin, used to detect either a lamp outage or an over-current condition for the TAIL LED array
8	CNTL	Determines, according to a percentange of VREF, the Pulse Width Controller internal oscillator duty cycle
9	REF	Stable Reference Voltage
10	GND	Ground
11	GND	Ground
12	B+	Power Supply
13	TAIL	TAIL input pin. When brought high, TAIL activates the IC and drives the TAIL led array.
14	STOP	STOP input pin. When brought high, STOP activates the IC and drives the STOP led array.
15	TURN	TURN input pin. When brought high, TURN activates the IC and drives the TURN led array.
16	FDBK	Internal Error Amplifier Inverting Pin
17	P-OUT	Power MOSFET drain pin
18	TS-PWM	A Three State Input. It determine the control logic for TAIL and STOP Low Side Drivers.
19	LMP-OUT	A weak pulled up signal during lamps No Fault condition and an active pulldown when a Fault condition is detected.
20	GND	Ground

ORDERING INFORMATION

TYPE	PowerSO-20™
STLC1	STLC1PD

TYPICAL APPLICATION CIRCUIT



ELECTRICAL CHARACTERISTICS FOR SMPD SECTION (T_J=-40 to 125°C unless otherwise specified. Typical values are referred at T_J=25°C, V_{B+}=14V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{B+}	Supply Operating Voltage	Normal Operating Range	9		24	V
		Normal Operating Range - TAIL only	6		24	
V_{SD}	B+ Input Overvoltage Shutdown		28	30	32	V
I_{SQ}	Total Off State Quiescent Current	V_{B+} = 14V, V_{TURN} = V_{STOP} = V_{TAIL} =0V		120	180	µA
f_{osc}	PWM Oscillator Frequency	V_{B+} = 14V	140	180	240	kHz
$R_{P(on)}$	Static drain to ground SMPS N-channel switch on resistance	V_{B+} = 9V, I_{P-OUT}=4A		180		mΩ
		V_{B+} = 14V, I_{P-OUT}=4A		170		mΩ
$I_{D(off)}$	P-OUT Off State leakage Current	V_{B+} = 16V,			20	µA
I_{LIMIT}	I_{P-OUT} Current Limit	V_{B+} = 14V, V_{FDBK} = 1V	8	12	16	A
$t_{SMPS-ON}$	SMPS Turn On Delay	C_{REF} = 1µF (see note 1,4 and Fig 1, 2)		1.6		ms
V_{LOAD}	Load Regulation	V_{B+} = 14V, I_{OUT} = 0.6 to 3A V_{OUT} = 10V		60		mV
V_{LINE}	Line Regulation	V_{B+} = 9 to 16V, I_{OUT} = 1.5A V_{OUT} = 10V		15		mV

ELECTRICAL CHARACTERISTICS FOR LOW SIDE DRIVER SECTION (T_J=-40 to 125°C unless otherwise specified. Typical values are referred at T_J=25°C, V_{B+}=14V)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$R_{(on)}$	Static drain to source LSD N-channel switch on resistance	V_{B+} = 9V,	$V_{TURN} = V_{B+}$ V_{TR-L} = 0V I_{TR-DRV}=1A		500		mΩ
			$V_{STOP} = V_{B+}$ V_{ST-L} = 0V I_{ST-DRV}=1A		500		mΩ
			$V_{TAIL} = V_{B+}$ V_{TL-L} = 0V I_{TL-DRV}=1A		500		mΩ
$I_{LSD(off)}$	OFF State LSD'S leakage current	$V_{TURN} = V_{STOP} = V_{TAIL}$ =0V $V_{TR-DRV} = V_{ST-DRV} = V_{TL-DRV} = V_{B+}$				10	µA
t_{LSD-ON}	LSD Turn On Delay	C_{REF} = 1µF C_{OUT} = 220µF (see note 2,4 and Fig 1, 2)			2		ms
V_{LS-ON}	FDBK Voltage over which LSD's are enabled				$0.95V_{FB}$		V
V_{LS-OFF}	FDBK Voltage over which LSD's are disabled				$0.5V_{FB}$		V
f_{LSD}	Pulse Width Controller Internal Oscillator Frequency	$V_{TAIL} = V_{B+}$ $V_{TS-PWM} = V_{REF}/2$		200	380	500	Hz
$V_{IN(ON)}$	Input Threshold voltage to enable LSD	V_{B+} = 9 to 16V			$0.6V_{B+}$		V
$V_{IN(OFF)}$	Input Threshold voltage to disable LSD	V_{B+} = 9 to 16V			$0.4V_{B+}$		V

ELECTRICAL CHARACTERISTICS FOR FEEDBACK AND CONTROL (T_J=-40 to 125°C unless otherwise specified. Typical values are referred at T_J=25°C, V_{B+}=14V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{LOUT}	Lamp Outage Detect Threshold Voltage	T_J=25°C	150	200	250	mV
$V_{H-SHORT}$	Output Overcurrent Threshold Voltage	T_J=25°C	1.2	1.3	1.6	V
V_{REF}	External Voltage Reference	$V_{TURN} = V_{STOP} = V_{TAIL} = V_{B+}$ I_{REF} = 500µA	3.6	3.8	4	V
V_{FB}	Internal Band-gap Voltage Reference (see schematic diagram)	$V_{TURN} = V_{STOP} = V_{TAIL} = V_{B+}$	1.15	1.24	1.3	V
$V_{LH(en)}$	Device Enabled Lamp Outage no fault High Voltage	V_{B+} = 9 to 16V, $I_{LMP-OUT}$ < -4mA At least one input enabled. No fault condition.	V_{B+}-2		V_{B+}	V
$V_{LH(dis)}$	Device Disabled Lamp Outage no fault High Voltage	V_{B+} = 9 to 16V, $I_{LMP-OUT}$ < -2mA $V_{TURN} = V_{STOP} = V_{TAIL}$ = 0V	V_{B+}-2		V_{B+}	V
V_{LL}	Lamp Outage fault Low Voltage	V_{B+} = 9 to 16V $I_{LMP-OUT}$ < 100mA At least one input enabled. Fault condition.		1.5		V
$R_{(IN)}$	TURN, STOP and TAIL Input Resistance	V_{B+} = 12V,		18.5		kΩ
T_{SHDN}	Thermal Shutdown Threshold	(see Note 4)		150		°C
T_{HYST}	Thermal Shutdown Hysteresis	(see Note 4)		10		°C
$t_{F(on)}$	Time to Fault Indication ON			60		µs
$t_{F(off)}$	Time to Fault Indication OFF			8		ms
$V_{TS-PWM(L)}$	TS-PWM Low State Voltage (see table 1)				$0.1V_{REF}$	V
$V_{TS-PWM(M)}$	TS-PWM Mid State Voltage (see table 1)		$0.21V_{REF}$		$0.79V_{REF}$	V
$V_{TS-PWM(H)}$	TS-PWM High State Voltage (see table 1)		$0.98V_{REF}$			V

Note 1: The device is powered. If only one of the three inputs is enabled (the remaining inputs are shorted to ground), $t_{SMPS-ON}$ is the time required for the OUT voltage to reach the10% of its own steady state value

Note 2: The device is powered. If only one of the three inputs is brought high (the remaining inputs are shorted to ground), T_{LSD-ON} is the time required for the current to flow in the enabled LSD

Note 3: The device is powered and at least one input is enabled. If this input is disabled, $T_{LSD-OFF}$ is the time required for the current to become zero in the previously enabled LSD.

Note 4: Guaranteed by design, not tested in production.

FUNCTIONAL DESCRIPTION

SMPS

The N-channel Power MOSFET is source grounded, thus it is possible to use any converter configuration with the power switch connected to ground. A SEPIC topology (Single Ended Primary Inductor Current) is shown in the typical application schematic.

INPUTS PINS

The IC's inputs are TURN, STOP and TAIL. If all inputs are disabled, SMPS and most of the internal control and diagnostic circuitry are not active. This is done in order to maintain the stand-by quiescent current at very low values.

When only one of these inputs is put high (e.g connected to V_{B+}), a device start-up phase begins. First the C_{REF} capacitor is charged and, once the voltage on it has reached about 95% of its steady state value (V_{REF}), the SMPS is enabled. In order to allow the output to reach the regulated voltage value faster, the LSD corresponding to the input enabled will conduct

only when the OUT voltage is about 95% of its final value. Such a start-up phase takes place when only one input is enabled.

LOW SIDE DRIVER:

The purpose of the low side drivers is to connect the LED cluster to ground, creating a path for the current. Using external resistors, current flowing into the LED cluster is set according to the following formula:

$$I_{ARRAY} = \frac{V_{OUT} - V_{ARRAY}}{R_T + R_L + R_{(on)}}$$

where (see typical application schematic):
$R_L = R_{LT}$, R_{LS}, or R_{LR}
$R_T = R_{TT}$, R_{TS}, or R_{TR}
$R_{(on)}$ = Static drain to source LSD on resistance
V_{OUT} = Output Voltage
V_{ARRAY} = Expected LED array voltage drop.
LSD over-current protection and under-current diagnostic (see LAMP OUTAGE DETECTION section) is performed by sensing the voltage on resistors, when the corresponding LSD are enabled.
If the voltage on exceeds $V_{H\text{-}SHORT}$, the over-current protection acts by reducing the LSD average current by switching ON and OFF the LSD itself.

LAMP OUTAGE DETECTION

Resistors are used to sense the LED array current. In case one or more LEDs fail (open circuit) the current on the corresponding resistor will drop due to the increased LED array resistance. As soon as the voltage drop on is lower than V_{LOUT}, a LED lamp fault condition is detected and the LMP-OUT pin becomes active (low). The LAMP-OUTAGE functionality is AND-ed with each input, that is a fault condition can be detected only when the LED arrays are enabled.

DIMMING

The dimming of the LED lamps can be obtained by using the internal PULSE WIDTH controller (it drives the LSD TAIL and STOP gates). The duty cycle of this internal oscillator (whose frequency is 380Hz typical) can be set, forcing the voltage of the CNTL pin to be a fraction of V_{REF}, by using a simple resistor divider (as shown in the typical application scheme).

In this case the duty cycle percentage can be calculated with the following approximated formula:

$$DC\% \cong \begin{cases} 3.8 \text{ if } \dfrac{R_{C1}}{R_{C1}+R_{C2}} \le \dfrac{0.2}{V_{REF}} \\ \dfrac{R_{C1}}{R_{C1}+R_{C2}} \bullet 100 \quad \text{Elsewhere} \end{cases}$$

The TS-PWM pin voltage, according to the TABLE1 determines which LSD is PULSE WIDTH CONTROLLER driven. Internal dimming can only be performed on the TAIL and STOP arrays. The TURN array can be externally dimmed (as well as TAIL and STOP) by driving the corresponding input witha a square pulse signal whose maximum frequency must be 200Hz.

TS-PWM ENCODING TABLE

TYPE	INPUTS ACTIVATED	DRIVE TYPE	
		TAIL ARRAY	STOP ARRY
LOW (V_{TS-PWM}<0.1V_{REF})	TAIL	PWM	PWM
	STOP	OFF	ON
	TAIL AND STOP	PWM	ON
MID (V_{TS-PWM}<0.1V_{REF}/2 or floating)	TAIL	PWM	OFF
	STOP	OFF	ON
	TAIL AND STOP	PWM	ON
HIGH (V_{TS-PWM}>0.98V_{REF})	TAIL	PWM	PWM
	STOP	ON	ON
	TAIL AND STOP	ON	ON

Figure 1 : Start-up phase and input signal timing diagram (with TS-PWM floating)

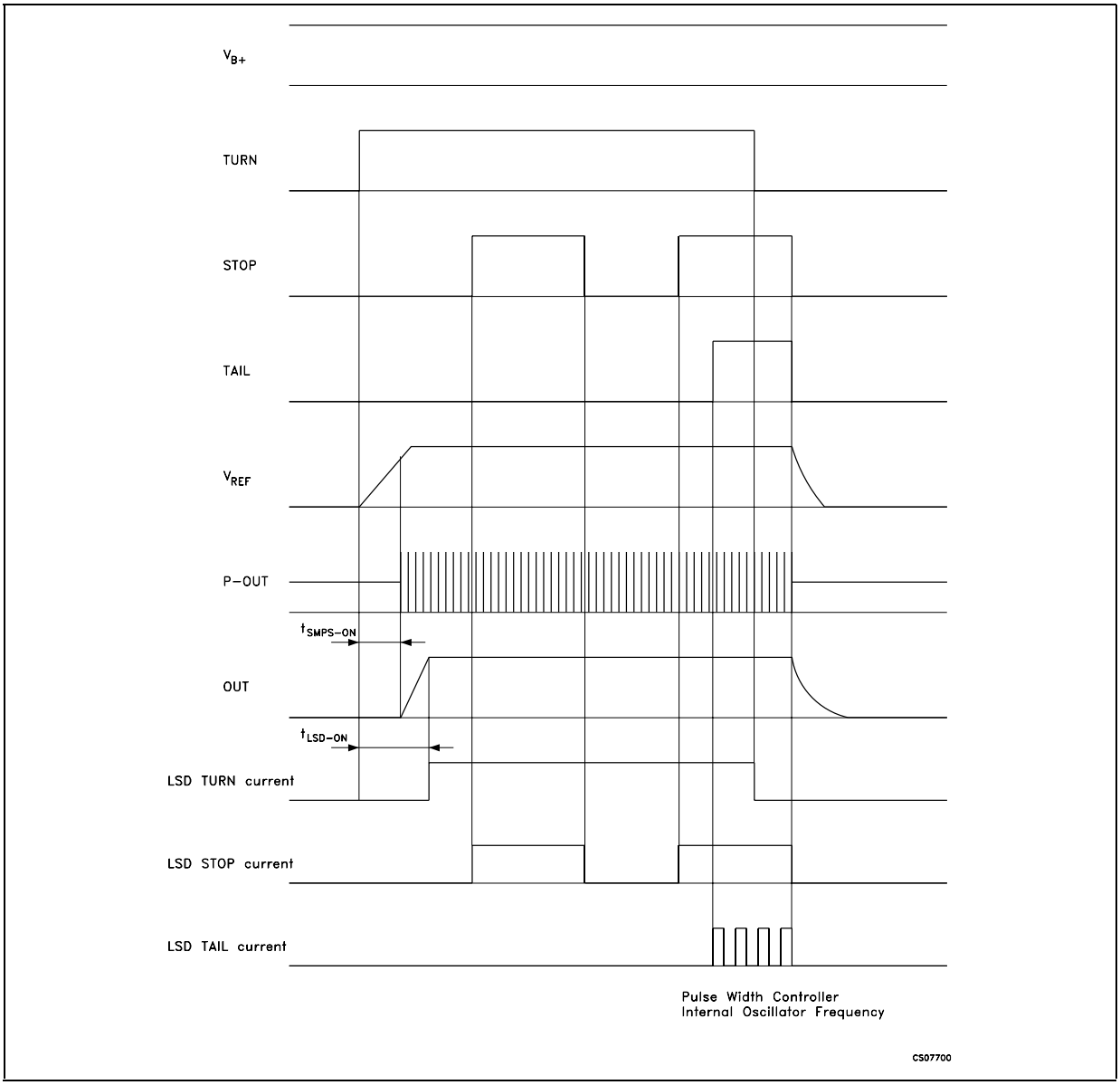


Figure 2 : Magnified start-up phase timing diagram

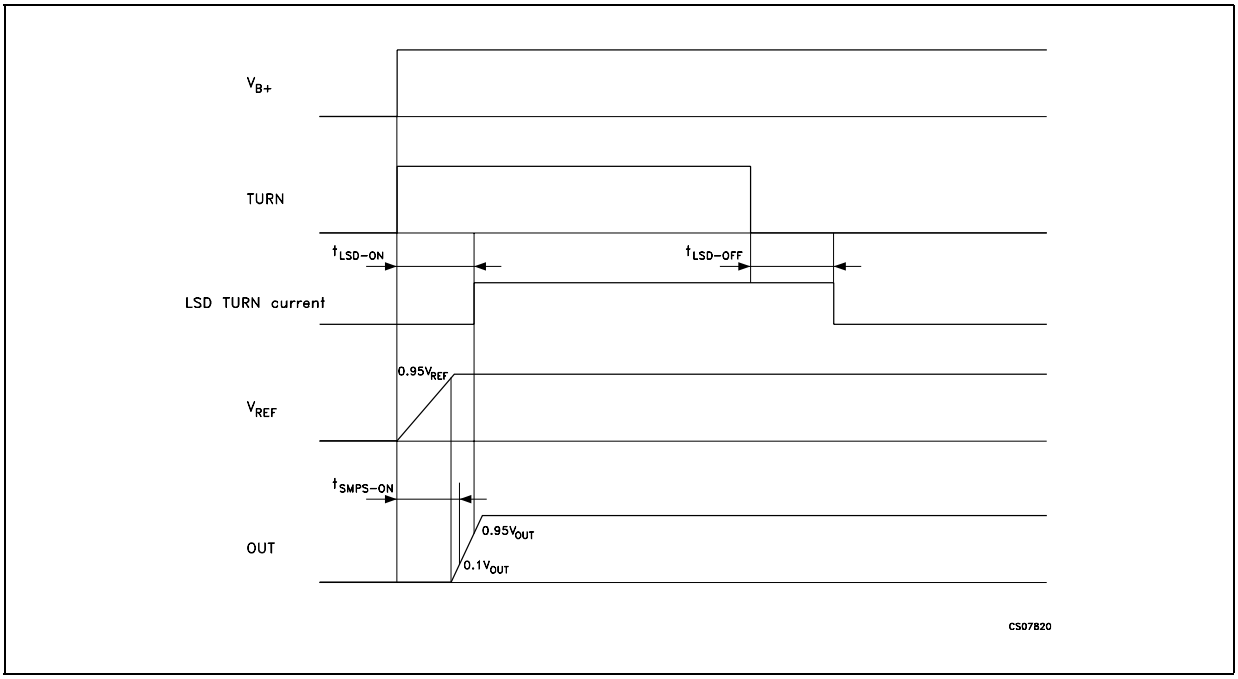
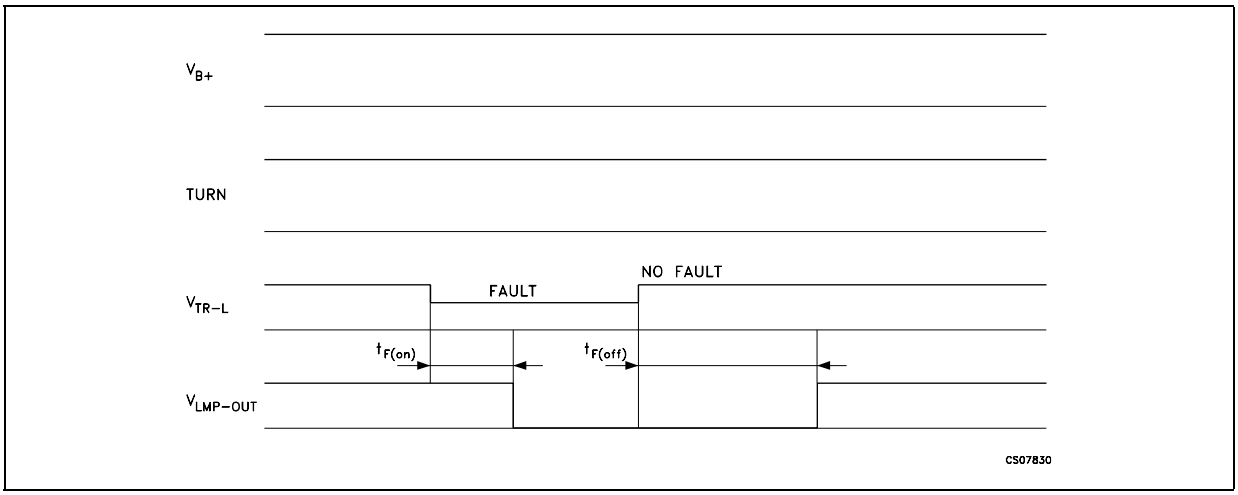


Figure 3 : Fault indication on and off timing diagram



TYPICAL CHARACTERISTICS (See PCB BOM)

Figure 4 : Output Voltage vs Output Current

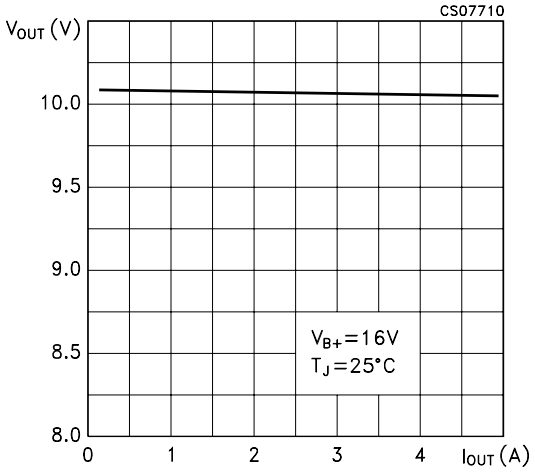


Figure 5 : Output Voltage vs Output Current

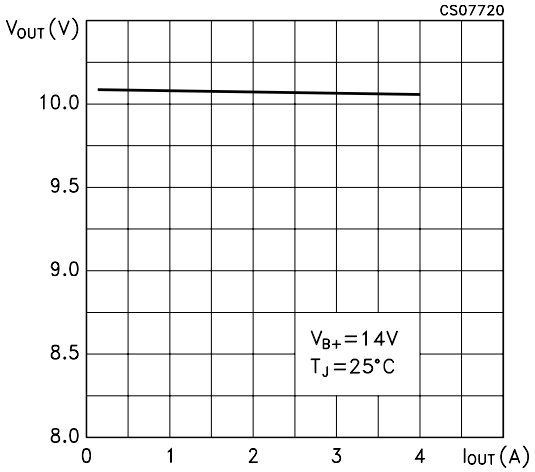


Figure 6 : Output Voltage vs Output Current

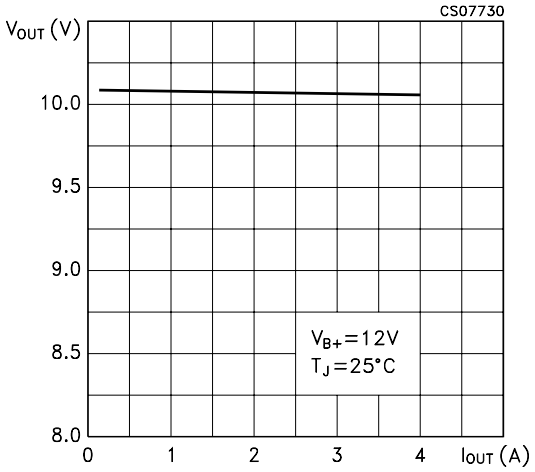


Figure 7 : Output Voltage vs Output Current

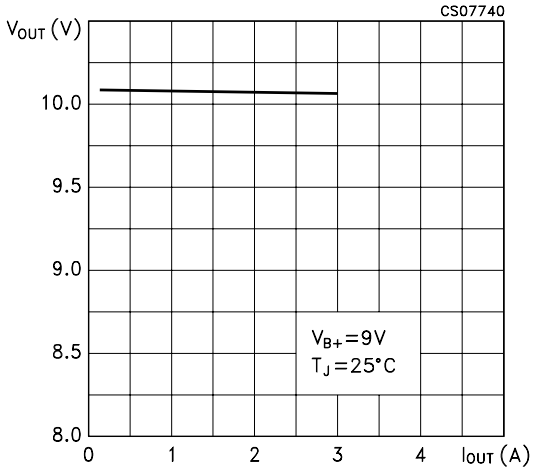


Figure 8 : Duty Cycle Oscillator Frequency vs CNTL Voltage

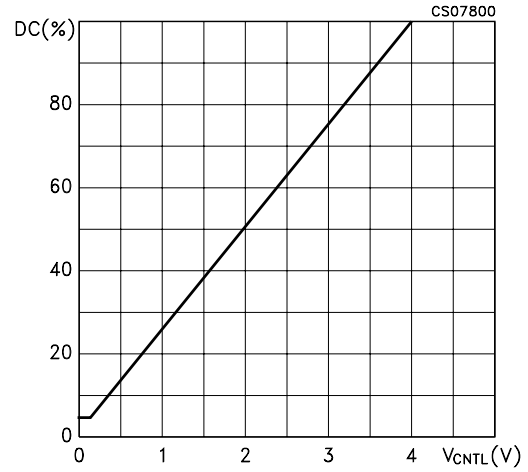


Figure 9 : LMP-OUT Voltage (Fault Condition) vs LMP-OUT Sinked Current

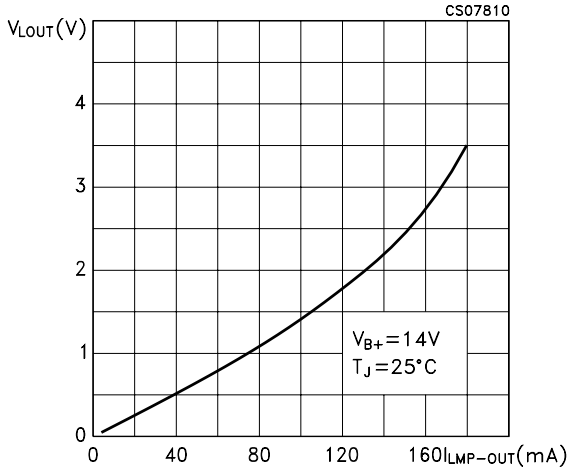


Figure 10 : Total OFF State Quiescent Current vs Temperature

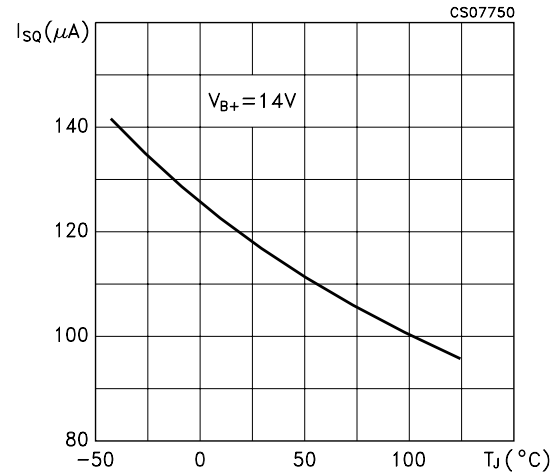


Figure 11 : Time to Fault Indication ON vs Temperature

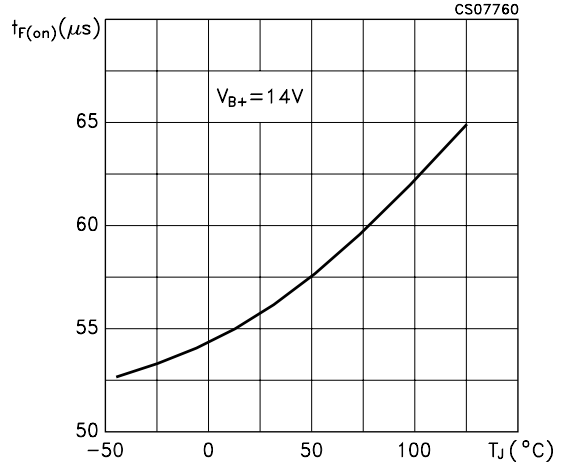


Figure 12 : Time to Fault Indication OFF vs Temperature

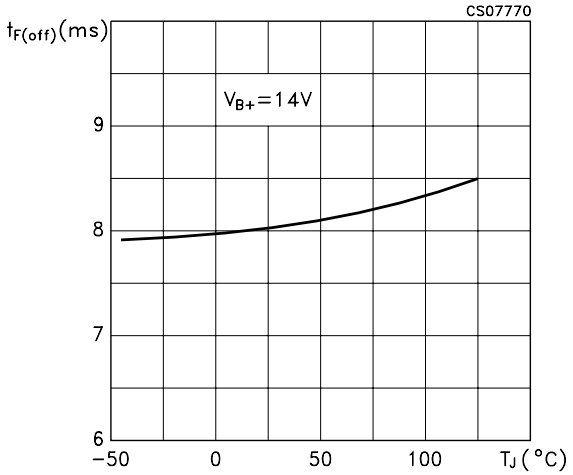


Figure 13 : External Reference Voltage vs Temperature

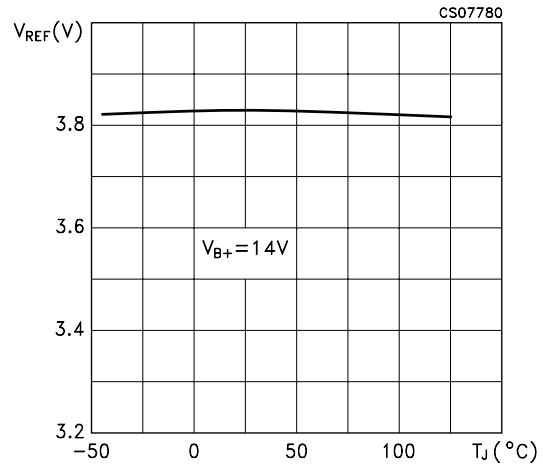


Figure 14 : V_{FB} Voltage vs Temperature

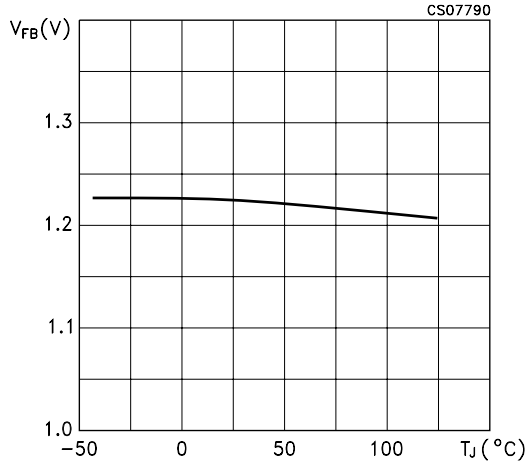


Figure 15 : Demoboard Schematic

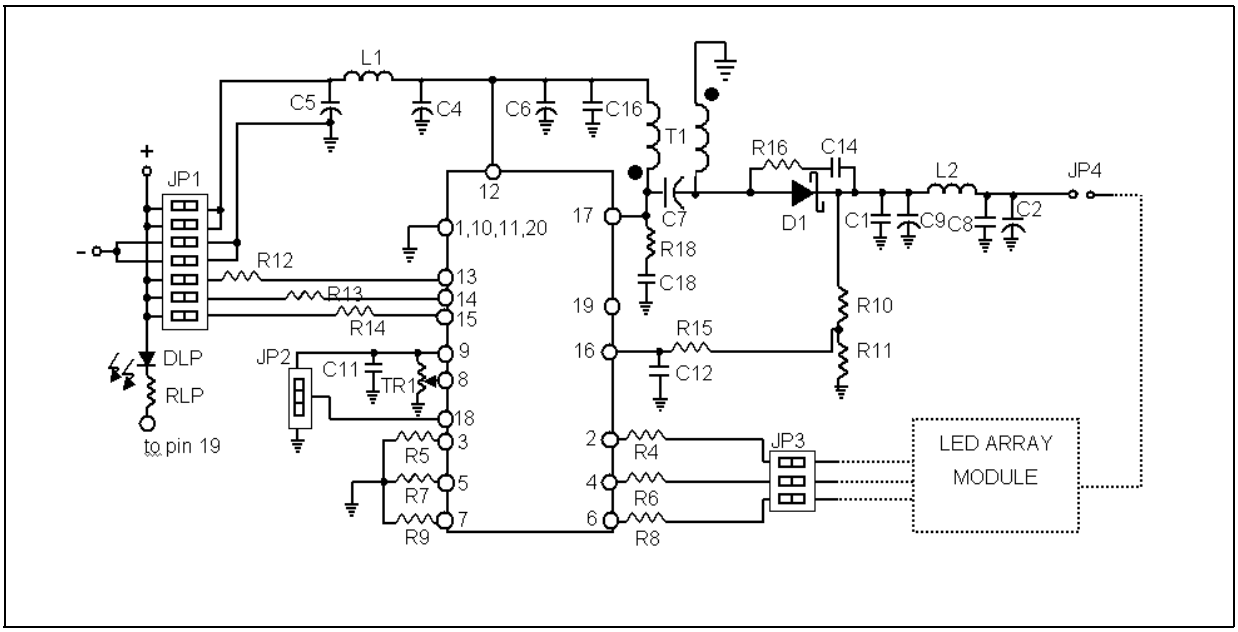


Figure 16 : PCB Components outline

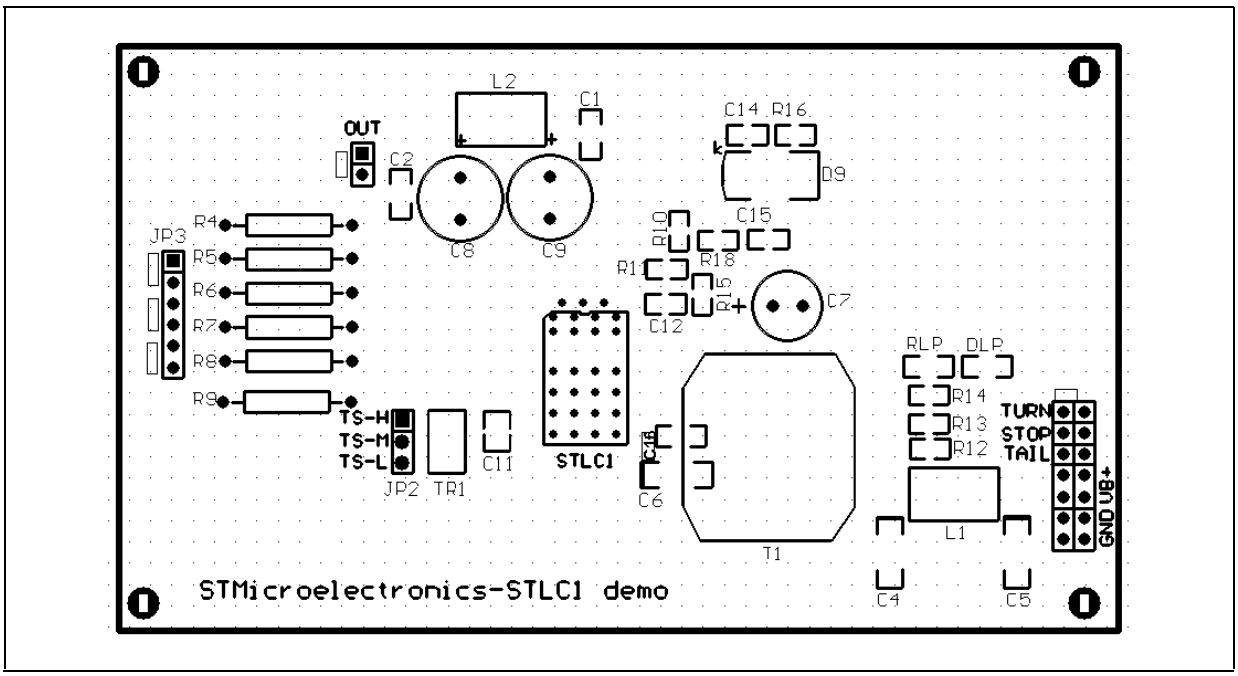


Figure 17 : PBC Top Layer

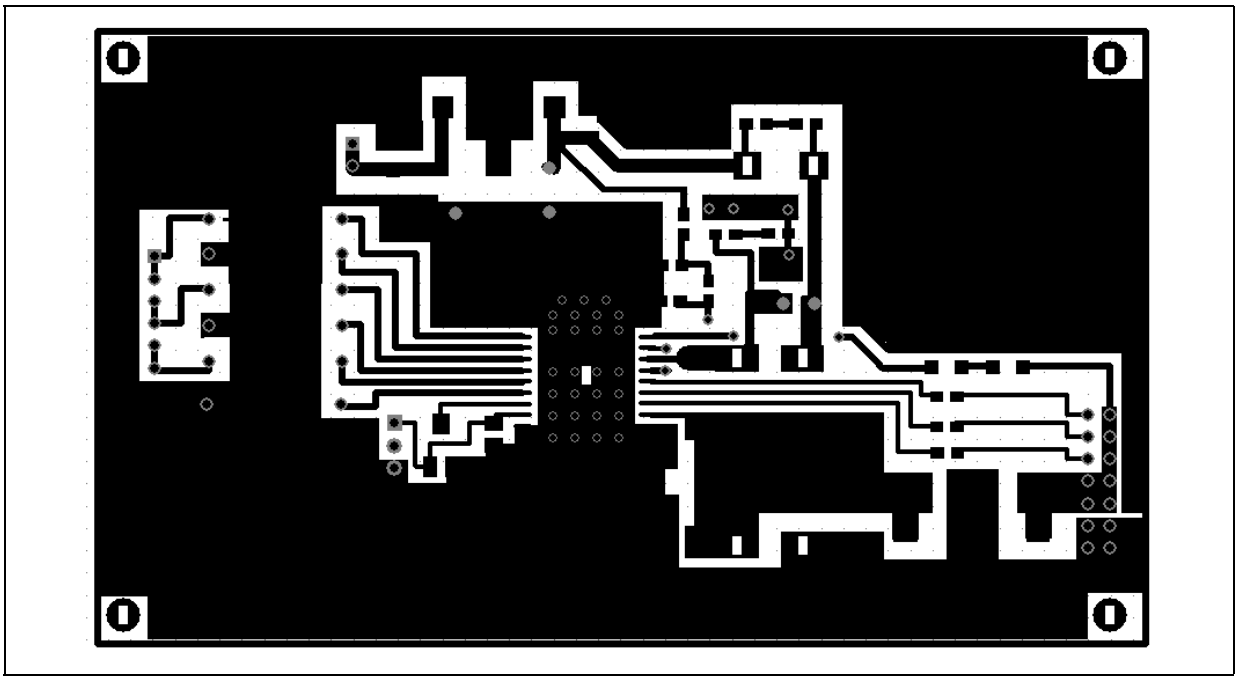
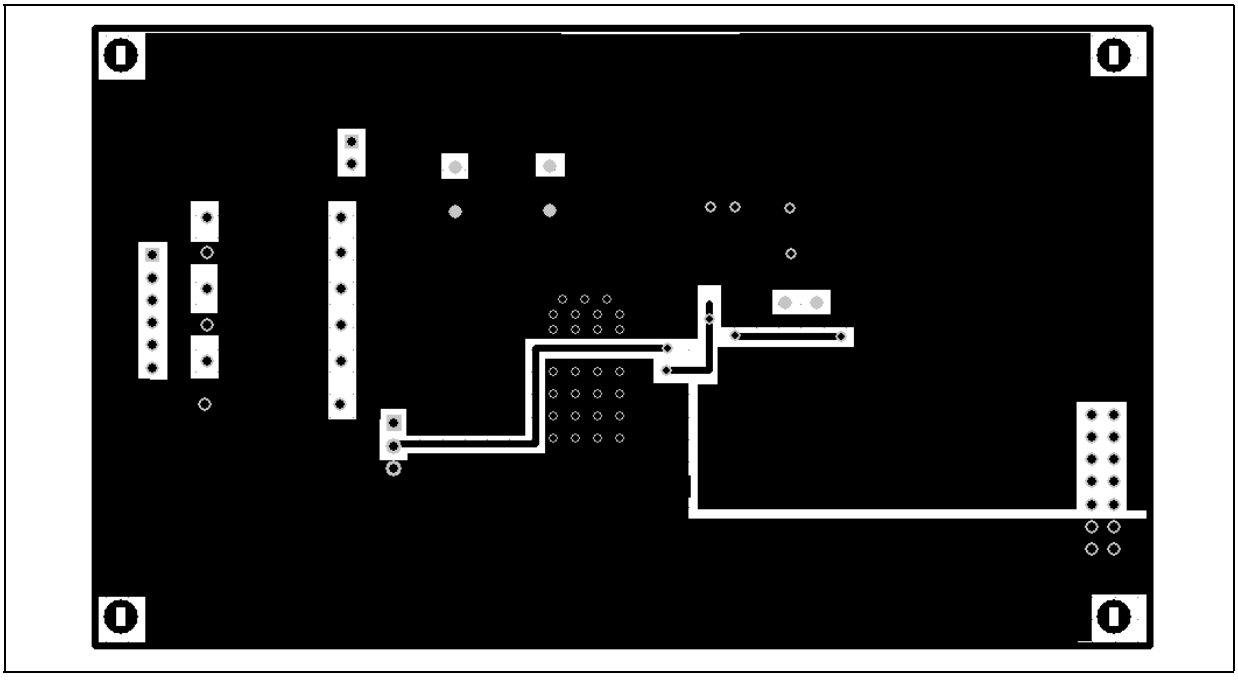


Figure 18 : PBC Bottom Layer



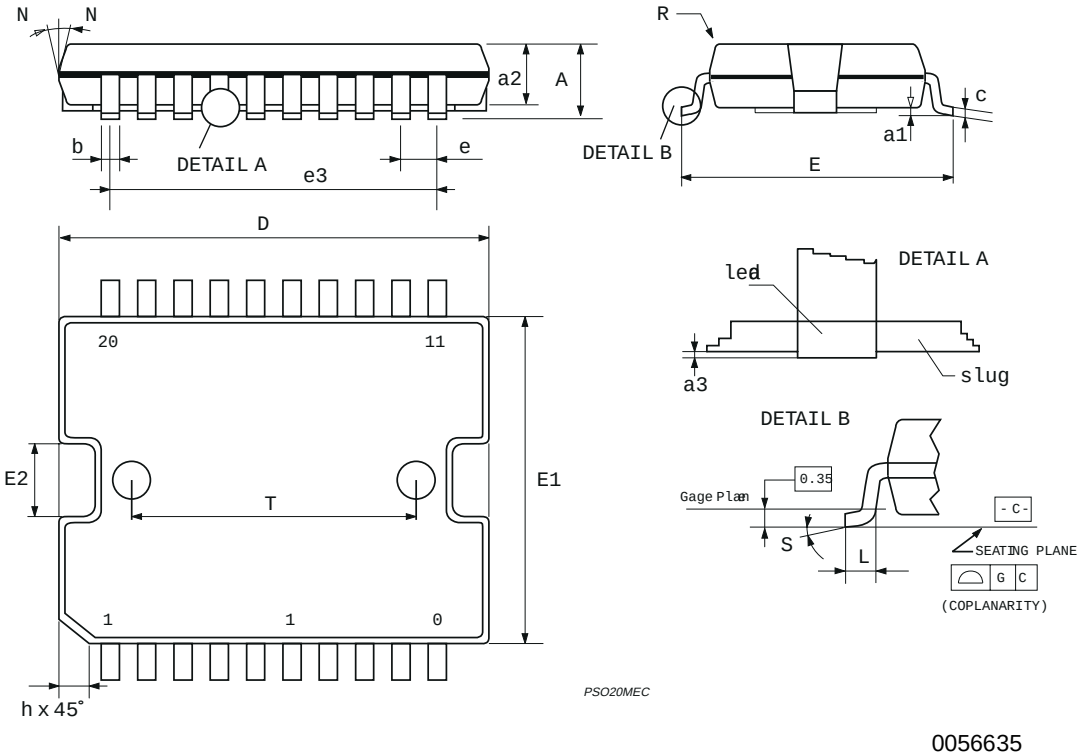
PCB BOM

REFERENCE	DESCRIPTION
L1, L2	VK200
C4, C5, C6	22µF-35V Electrolytic Capacitor Low ESR
C16	220nF-35V Ceramic Capacitor X7R Dielectric
C7	47µF-35V Electrolytic Capacitor
C1, C2	4.7nF-35V Ceramic Capacitor X7R Dielectric
C8, C9	220µF-35V Electrolytic Capacitor Low ESR
C14	560pF
C18	560pF-50V
C11	1µF-35V Tantalium Capacitor
C12	220pF Ceramic Capacitor
R10	9.1kΩ Resistor 125mW 0.1%
R11	1.3kΩ Resistor 125mW 0.1%
R15	4.7kΩ Resistor 125mW 5%
R16	56Ω Resistor 125mW 5%
R18	10Ω Resistor 250mW 5%
R12, R13, R14	1.2kΩ Resistor 125mW 5%
R4, R6, R8	2.2Ω Resistor 1W 5%
R5, R7, R9	1Ω Resistor 1W 5%
TR1	10kΩ Trimmer
RLP	1.5kΩ Resistor 125mW 5%
D1	Schottky Diode STPS3L40S
DLP	Led Diode
T1	SEPIC inductor, Toroid Horizontal THT 20µH@10ADC, 200-250KHz
JP1, JP2, JP3	Jumper

PowerSO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10	0		0.0039
b	0.40		0.53	0.0157		0.0209
c	0.23		0.32	0.0090		0.0013
D (1)	15.80		16.00	0.6220		0.630
E	13.90		14.50	0.5472		0.5710
e		1.27			0.0500	
e3		11.43			0.4500	
E1 (1)	10.90		11.10	0.4291		0.4370
E2			2.90			0.1141
G	0		0.10	0.0000		0.0039
h			1.10			0.0433
L	0.80		1.10	0.0314		0.0433
N			10°			10°
S	0°		8°	0°		8°
T		10.0			0.3937	

(1) “D and E1” do not include mold flash or protusions - Mold flash or protusions shall not exceed 0.15mm (0.006”)



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