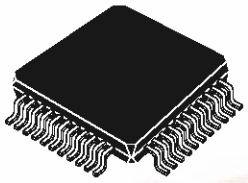
SGS-THOMSON MICROELECTRONICS

STLC5432

2Mbit CEPT & PRIMARY RATE CONTROLLER DEVICE

PRELIMINARY DATA

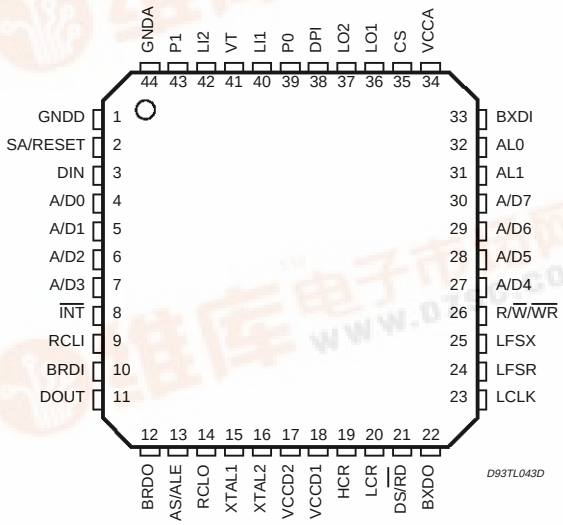
- ONE CHIP SOLUTION FROM PCM BUS TO TRANSFORMER (CEPT STANDARD)
- ISDN PRIMARY ACCESS CONTROLLER (COMPATIBLE WITH ETSI, OPTION 1 AND 2)
- HDB3/BIN ENCODER AND DECODER ON CHIP
- MULTIFRAME STRUCTURE HANDLING
- BUILT IN CRC4
- EASY LINK TO ST5451/MK50H25/MK5027 LINK CONTROLLERS.
- DATA RATE: 2048, 4096 AND 8192 Kb/s FOR MULTIPLEXED APPLICATIONS
- FOUR LOOPBACK MODES FOR TESTING
- PSEUDO RANDOM SEQUENCE GENERATOR AND ANALYZER FOR ON-LINE, OFF-LINE AND AUTOTEST
- CLOCK RECOVERY CIRCUITRY ON CHIP
- 64 BYTE ELASTIC MEMORY FOR TIME COMPENSATION AND AUTOMATIC FRAME AND SUPERFRAME ALIGNMENT
- 32 ON CHIP REGISTERS FOR CONFIGURATIONS, TESTING, ALARMS, FAULT AND ERROR RATE CONTROL.
- AUTO ADAPTATIVE DETECTION THRESHOLD
- AUTOMATIC EQUALIZER OPTION
- 5V POWER SUPPLY
- AMI OR HDB3 CODE SELECTION
- PARALLEL OR SERIAL MICROPROCESSOR INTERFACE OPTION
- BOTH µp AND STAND ALONE MODE AVAILABLE



TQFP44 (10 x 10)

ORDERING NUMBER: STLC5432Q

PIN CONNECTION (Top view)



DESCRIPTION

STLC5432, CMOS device, interfaces the multiplex system to the physical CEPT Transmission link at 2048Kb/s. Furthermore, thanks to its flexibility, it is the optimum solution also for the ISDN application as PRIMARY RATE CONTROLLER. The receive circuit performances exceed CCITT recommendation and the line driver outputs meet the G.703 specifications.
STLC5432 is the real single chip solution that allows the best system flexibility and easy design. STLC5432 can work either in 2048 or 4096 or 8192 Kbit/s systems programming the CR4 register (when parallel micro interface selected).

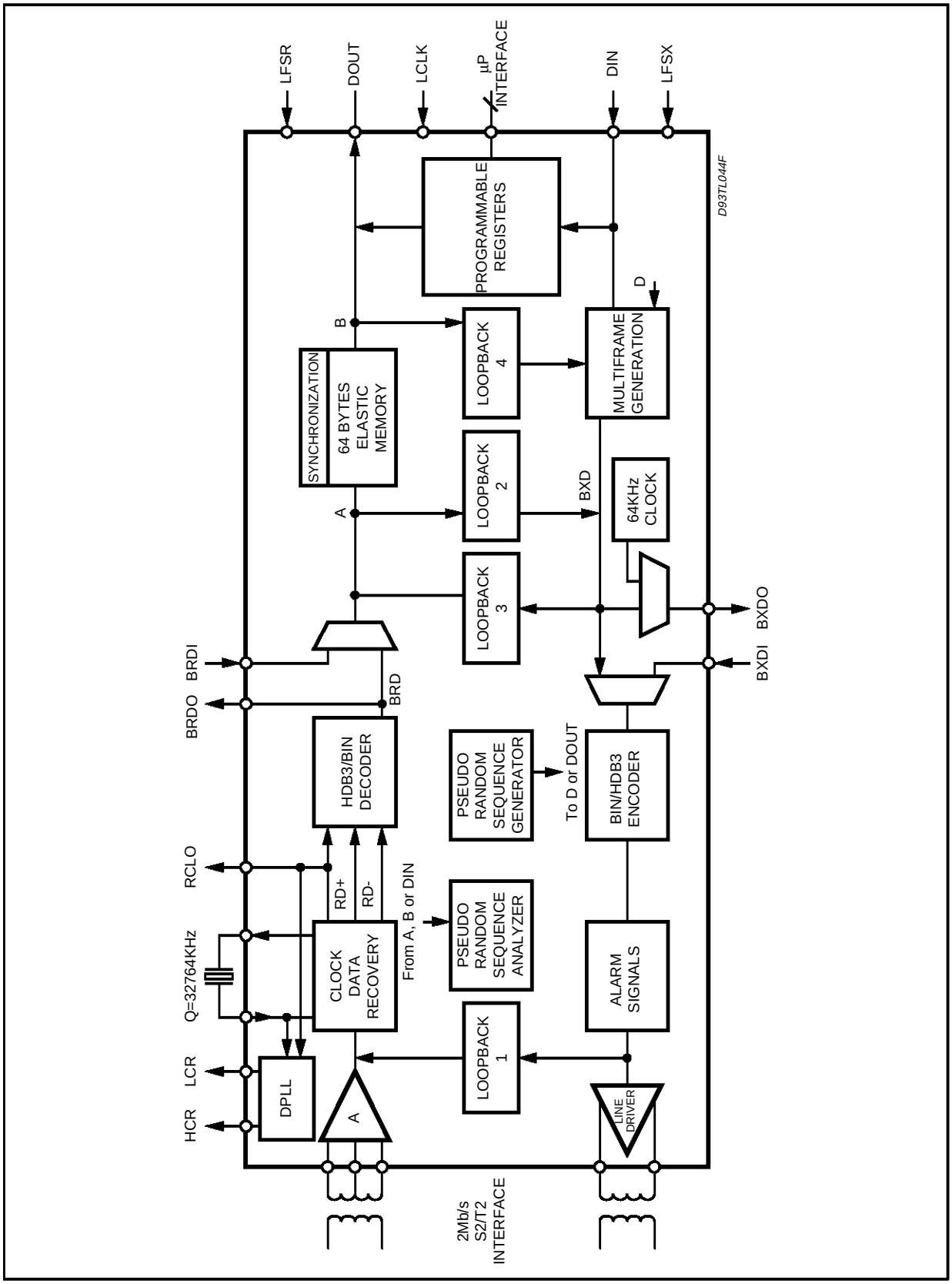
PIN DESCRIPTION

Name	Pin	Type	Function
VCCD1 VCCD2 VCCA	18 17 34	I I I	Positive power supply inputs for the digital (V_{CCD1}) and analog (V_{CCA}) sections and for microprocessor interface signals (V_{CCD2}). They must be +5 Volts and must be directly connected together.
GNDD GNDA	1 44	I I	Negative power supply pins which must be connected together close to the device. All digital and analog signals are referred to these pins, which are normally at the system ground.
LI1 LI2	40 42	I I	Receive HDB3 signal differential inputs from the line transformer.
VT	41	O	Positive power supply output for fixing reference voltage to the receive transformer. Typical value is 2.375V
L01 L02	36 37	O O	Transmit HDB3 signal differential outputs to the line transformer.When used with an appropriate transformer, the line signal conforms to the output specifications in CCITT with a nominal pulse amplitude of 3 volts for a 120Ω load on line side.
XTAL1	15	I	The master clock input which requires either a parallel resonance crystal to be tied between this pin and XTAL2, or a clock input from a stable source. This clock does not need to be synchronized to the system clock. Crystal specifications = 32764 kHz ± 50 ppm parallel resonant; RS ≤ 20Ω loaded with 33pF to GND each side.
XTAL2	16	O	The output of the crystal oscillator, which should be connected to one end of the crystal if used.
HCR	19	O	High clock received, bit clock. When the device has recovered the clock from the HDB3 signal, HCR signal is synchronized to the remote circuit. The HCR frequency is either 8192kHz if 8MCR bit of CR1 Register is put to 1 or 4096 kHz if 8MCR is set to 0.
LCR	20	O	Low clock received, frame clock. When the device has recovered the clock from the HDB3 signal, LCR signal is synchronized to the remote entity. The LCR frequency is 8 kHz if 8KCR bit is set to 1, or 4 kHz if 8KCR bit is set to 0. When the remote clock is not recovered, HCR and LCR frequency are synchronized to master clock (16384 kHz). HCR and LCR can be used by the system in Terminal Mode.These two clocks can be used by the transmit function of the device.
BRDO RCLO	12 14	O O	Binary Receive Data Output, 2048 kbit/s or 64kbit/s. Receive Clock output, 2048 kHz or 64kHz. After decoding, Binary Data and clock associated are provided for different applications.
BRDI RCLI	10 9	I I	Binary Receive Data Input. 2048 kbit/s. Receive Clock Input 2048 kHz.
BXDO	22	O	Binary Transmit Data Output, 2048 kbit/s or output clock at 64kHz. Before encoding Binary Data is provided to different applications (Optical Interface for instance). Local clock is associated to this data.
BXDI	33	I	This binary signal can replace BXD internal signal to be encoded if SELEX bit (CR1 Register) is set to 1.
DOUT	11	O	Data Output. 30 B+D primary access data received from the line.Data can be shifted out from the tristate output DOUT at the LCLK frequency on the rising edges during all the time slots,except Time Slot Zero in accordance with TSOE bit (CR1Register). NB : If parallel micro-interface is selected, DOUT is at high impedance after Reset. DOUT is at low impedance after writing CR4 register.
DIN	3	I	Data Input : 30B+D primary access data to transmit to the line.Data can be shifted in at the LCLK frequency on the falling edges during all the time slots, except Time Slot Zero, in accordance with TSOE bit (CR1 Register).

PIN DESCRIPTION (continued)

Name	Pin	Type	Function
LCLK	23	I	Local Clock : this clock input determines the data shift rate on the two digital multiplexes. This clock frequency can be indifferently 2048, 4096, 8192 or 16384kHz. Data Out and Data In rate is always 2048 kbit/s when Serial Interface microprocessor: an internal automatic mechanism divides by two the frequency if 4096 kHz.
LFSR	24	I	Local Frame Synchronization for the Receiver. This clock input defines the start of the frame on the digital multiplex Data (pin DOUT). This clock frequency can be indifferently 8 kHz or a submultiple of 8 kHz.
LFSX	25	I	Local Frame Synchronization for the Transmitter. This clock input defines the start of the frame on the digital multiplex Data (pin DIN). This clock frequency can be indifferently 8 kHz or a submultiple of 8 kHz. If submultiple of 8 kHz, LFSX defines the start of even frame on DIN. The TSO of this even frame will contain the Frame Alignment Signal (FAS) on the line.
AL0, AL1	32 31	O O	Alarm 0 Output, alarm 1 Output. These pins are open drain outputs which are normally in high impedance state. **AL1** / **AL0** / **Alarm definitions** Z / Z / Frame or Multiframe recovered, A bit received is 0. 0Volt / Z / Frame or Multiframe recovered, A bit received is 1 Z / 0Volt / Frame and Multiframe lost, AIS Alarm Indication Signal is detected. 0Volt / 0Volt / Frame and Multiframe lost, AIS Alarm Indication Signal is not detected.
DPI	38	I	DPI input: The internal DPLL is synchronized either by the signal applied on DPI input (if DPIS bit of CR5 register is = 0) or by the 2MHz clock recovered from the line.
SA/RESET	2	I	**Stand Alone** : When this pin is connected to 5 Volts, the device works without microprocessor. The configuration is given by the values per default of programmable registers. BRDI and BXDI must not be used. **RESET**: When this pin is put to 5 Volts during 100 ns at least every programmable register is reset (value per default). When this pin is set at zero Volt, the type of microprocessor is selected by P0, P1 pins.
P0, P1	39, 43	I	Processor interface. These two input pins define the microprocessor interface chosen. P1 / P0 / Microprocessor Interface 0 / 0 / Serial Microprocessor Interface 0 / 1 / ST9 Microprocessor Interface 1 / 0 / Multiplexed Motorola processor interface 1 / 1 / Multiplexed Intel processor interface
AS/ALE	13	I	Address Strobe/Address Latch Enable. Input
CS	35	I	Chip Select. A high level on this input selects the PRCD for a read write operation.
R/$\overline{W}$/$\overline{WR}$	26	I	Read/Write/Write Data. Input.
DS/$\overline{RD}$	21	I	Data Strobe/Read Data. Input.
A/D0 to A/D7	4 to 7; 27 to 30	I/O	Address/Data 0 to 7. Input-Output.
$\overline{INT}$	8	O	Interrupt Request. The signal is activated low when the PRCD requests an interrupt. It is an open drain output.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC} to GND	Supply Voltage to Ground	7	V
V_I	Voltage at any digital or analog input	V_{CC}+1 to GND-1	V
I_{LO1}, I_{OL2}	Current at LO1 and LO2	±100	mA
I_C	Current at any digital or analog input	±30	mA
T_{stg}	Storage temperature range	-65 to +150	°C
T_L	Lead Temperature (soldering, 10s)	+300	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{thj\text{-}amb}$	Thermal Resistance Junction to ambient	Max.	50	°C/W

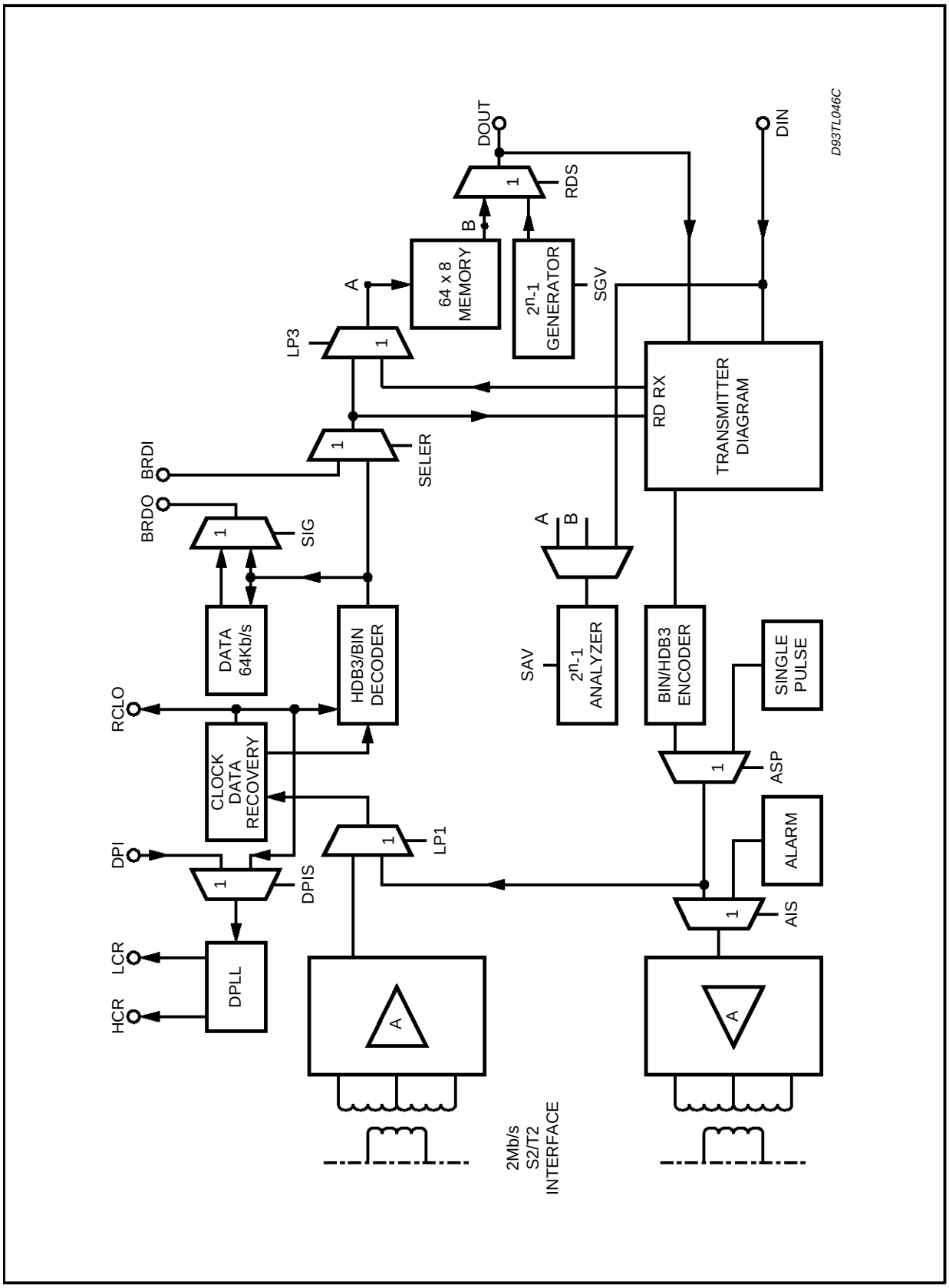
ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±5%, T_{amb} = 0 to 70°C; Typical characteristics are specified at V_{CC} = 5V, T_{amb} = 25°C; all signal are referenced to GND, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DIGITAL INTERFACE						
Vil	Input Low Voltage	All digital inputs			0.8	V
Vih	Input High Voltage	All digital inputs	2.2			V
Vilx	Input Low Voltage	XTAL1 input			0.5	V
Vihx	Input High Voltage	XTAL1 input	V_{CC}-0.5			V
Vol	Output Low Voltage	I_L = 7mA for pins AL0, AL1, INT, DOUT, HCR, LCR. All other digital outputs: I_L = 1mA			0.4 0.4	V V
Voh	Output High Voltage	I_L = 7mA for pins AL0, AL1, INT, DOUT, HCR, LCR. All other digital outputs: I_L = 1mA	2.4 2.4			V V
Iil	Input Low Current	Any digital input, Gnd < Vin < Vil			10	µA
Iih	Input High Current	Any digital input, Gnd < Vin < V_{CC}			10	µA
Ioz	Output Current in High Impedance (tri-state)	All digital tri-state I/Os without internal pull-up or pull-down resistor.			10	µA
LINE INTERFACE FEATURES						
Zin	Differential Input Resistance	DC measurement between LI1 and LI2 with the equalizer not connected		200		KΩ
Vin	Rx sensitivity	Relative to LI1/LI2 pins with fixed detection threshold	0.6			Vpk
Vpk75	Transmit amplitude	75Ω at transformer secondary	2.14	2.37	2.60	Vpk
Vpk120	Transmit Amplitude	120Ω at transformer secondary	2.7	3	3.30	Vpk
Sym	Pulses Symetry	75Ω or 120Ω at transformer secondary			5	%
Zero	Zero level	% nominal amplitude			10	%
Pwdth	Tx pulses width	at 50% of peak amplitude	219	244	269	ns
Zout	Differential Output Resistance			1		Ω
MASTERCLOCK						
MCLK	MCLK Frequency			32.764		MHz
	MCLK Frequency tolerance		–50		50	ppm
JITTER PERFORMANCES (for jitter transfer function and admissible jitter please report to the corresponding characteristics plotted in following page).						
	Intrinsic jitter	Filter 20Hz - 100KHz			0.125	UI
	Intrinsic jitter	Filter 700Hz - 100KHz			0.12	UI

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
POWER CONSUMPTION						
Icc75	Active Current (including line current)	random output (50% of ones)		40		mA
Icc120	Active Current (including line current)	random output (50% of ones)		40		mA
TRANSFORMER SPECIFICATION FOR 75Ω						
L:M:N:	Turns ratioes			1.57:1:1		
RL	L Windings Resistance			0.23		Ω
RMN	M and N winding resistances			0.11		Ω
LL	Inductance of winding L	F = 100KHz, Vrms = 100mV	2			mH
Ls	Leakage inductange of a winding, the other being short circuited	F = 100KHz, Vrms = 100V			0.3	µH
Ck	Inter winding capacitance	F = 100KHz, Vrms = 100mV			15	pF
TRANSFORMER SPECIFICATION FOR120Ω						
L:M:N:	Turns ratioes			2:1:1		
RL	L Windings Resistance			0.2		Ω
RMN	M and N winding resistances			0.1		Ω
LL	Inductance of winding L	F = 100KHz, Vrms = 100mV	2			mH
Ls	Leakage inductange of a winding, the other being short circuited	F = 100KHz, Vrms = 100mV			0.2	µH
Ck	Inter winding capacitance	F = 100KHz, Vrms = 100mV			15	pF
XTALL SPECIFICATIONS						
Co	Motional capacitance			0.2		pF
Cc	Shunt capacitance			6		pF
Lo	Inductance			4.718		mH
Rs	Serial resistance			15		Ω
CL	Load (corresponding to two 33pF capacitors connected to XTAL1 and XTAL2 pins on the application schematic)			20		pF
DYNAMIC CHARACTERISTICS						
tpd	LCLK high to DOUT valid LCLK high to BXDO valid XTAL1 high to HCR high or low	150pF; 7mA 50pF; 1mA 150pF; 7mA			50	ns
tpdz	LCLK high to DOUT HZ	150pF; 7mA			50	ns
td	HCR high to LCR high or low RCLO high to BDRO high or low	150pF; 7mA 50pF; 1mA	–20		20	ns
ts	All data inputs to clock low		10			ns
th	Clock low to all data inputs		10			ns

Figure 1: Receiver Diagram



INTRODUCTION

This single chip CMOS Device interfaces the physical multiplex of the application to the physical CEPT transmission link at 2048kb/s.

STLC5432 contains analog and digital functions to implement line interface function and frame synchronization. It meets pulse shape and jitter specifications in accordance with CCITT Recommendations and CEPT standards.

FUNCTIONAL DESCRIPTION

1. LINE INTERFACE

1.1 Receiver

The receive input signal should be derived via a transformer of the same type used for the transmit direction. The suggested transformer is the VAC L4097-X004 or equivalent for the 75 ohms case and the VAC 4097-X012 or equivalent for the 120 ohms case. The electrical models of the transformers are summarized in the following table :

Loads (Ω)	n	Ls (μH)	Ck (pF)	Lh (mH)	Rcul (Ω)	RculII (Ω)
75	1.57:1:1	≤0.3	≤15	≥2	0.11	0.23
120	2:1:1	≤0.2	≤15	≥2	0.10	0.20

with:

n:	Winding ratioes
Ls:	Leakage inductance
Ck:	Inter winding capacitance
Lh:	Principal inductance of windings
RcuI and RcuIII :	DC resistances of winding I and III.

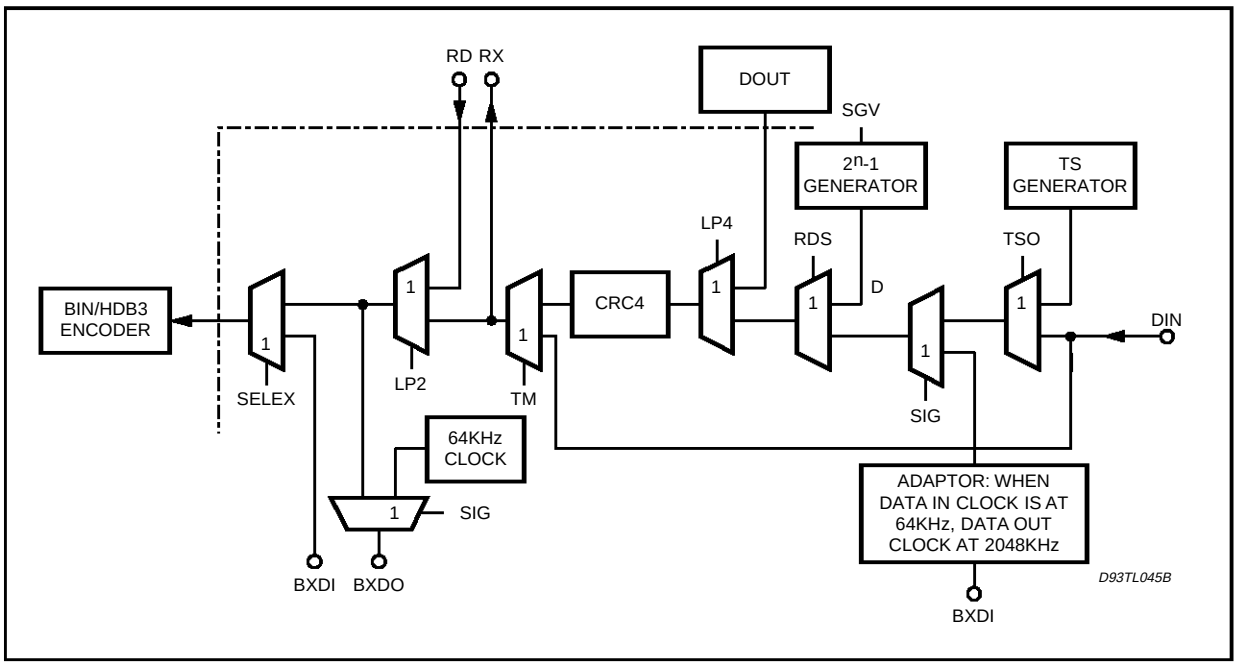
Wiring between the transformer and the circuit should respect the application schematic given in annex. (see fig 4).

The internal fixed threshold is set to 200 mV over the common mode voltage VCM (VCM = 2.375 V nominal) to insure the specified transmission range with a good noise immunity.

Two options are provided for special applications requiring improved transmission ranges:

- AUTO-ADAPTATIVE THRESHOLD:
  Using the configuration register CR4 (AVT), a peak amplitude detector circuit is connected to the received signal and after digital processing, an adaptative threshold value equal to 3/8 of the peak value is obtained at the output of a D to A converter and used for data detection.
- AUTOMATIC EQUALIZER: connecting two external capacitors of 100pF in series between the transformer and the circuits inputs, and using the configuration register CR4 (EQV), the circuit will select automatically a pre-compensation filter for long line configuration (see application schematic on figure 3 and 4 given in annex).

Figure 2: Transmitter Diagram



Using both options allow the reception of a signal attenuated up to 12dB at 1024kHz.

The Clock recovery is performed by a first PLL that guaranties the CCITT I431 requirements for the allowed Jitter, see Figure 23, this clock, RCL, is used internally and as local clock.
A second DPLL starting from this RCL clock attenuate the Jitter, to fulfil the CCITT I431, see figure 8, this DPLL generate HCR, bit clock, and LCR frame clock, practically without Jitter.

1.2 Transmitter

The line driver outputs are designed to drive the suitable transformer mentioned in the previous section. The transformer results in a signal amplitude of 3 volts on the line which meet G.703 pulse shape for a 120 ohm load (2.37 volt for a 75 ohms load).

A special test mode is provided to check the pulse template according to the CCITT mask by using the configuration register CR3 (ASP).

When the ALS command is valid, consecutive logical "ones" are transmitted on the line.

When APS command is valid, consecutive 1, 0, 1... 1, 0, 1, 0... are transmitted on the line.

2 CODING

2.1 HDB3/BIN DECODING

The two constituents of the data signal are decoded and the binary Receive Data Signal (BRD) is processed by the next functions.

2.2 BIN/HDB3 ENCODING

The binary transmit data signal (BXD) is encoded. The entire data stream, including all the time slots, is scanned for an occurence of four consecutive zeros.

Such occurence is replaced by the appropriate HDB3 code.

3. BINARY INPUT-OUTPUT

STLC5432 can directly interface binary data stream by means of the 6 dedicated pins:
BRDO, RCLO, BRDI, RCLI, BXDO and BXDI.
This allows the use of STLC5432 also for particular cases as for optical fiber or for different purposes. The functions of these 6 pins are defined by the SIG bit (SIGR register).

3.1 SIG = 0

When the bit SIG = 0 the binary data are exchanged at 2048KHz and the 6 extra pins are defined hereafter.

3.1.1 Extra pins for receive data

The BRDO and RCLO output pins deliver respectively BRD binary receive data at 2048kb/s and the remote clock recovered at 2048kHz.

Two BRDI and RCLI input pins can receive external binary receive data at 2048kb/s and the receive clock associated at 2048kHz.

The SELER command replaces BRD internal signal with BRDI signal.

3.1.2 Extra pins for transmit data

The transmit binary data output pin BXDO delivers transmit binary data BXD.

Input pin BXDI can receive external binary transmit data.

The SELEX command replaces BXD internal signal with BXDI signal.

3.2 SIG = 1

When SIG = 1, a signaling channel at 64 kb/s is implemented.

3.2.1 Extra pins for Receive data

BRDO and RCLO output pins deliver respectively receive data at 64kb/s selected by an internal Time Slot Assigner and the receive clock associated at 64kHz. In this case, BRDI and RCLI are not used.

3.2.2 Extra pins for Transmit Data

Output BXDO delivers the 64kHz clock for an external application. This external entity delivers data at 64kb/s on the rise edge of the clock.

Input BXDI shifts data at 64 kb/s on the fall edge of the 64kHz clock.

The same Time Slot Assigner is used by transmitter and receiver (See SIGR Register).

4 LOOPBACK

4.1 LOOPBACK 1

When LP1 Command is valid (LP1 bit high, see CRC3 register), output data signal replaces input data signal. Then, the recovery clock function provides the local clock. The loopback is transparent if AIS is at 0. If AISX is at 1, consecutive logical "ones" are transmitted on the line.

4.2 LOOPBACK 2

LP2 Command (LP2 bit high, CR3 register) replaces BXD and XCLK signals (respectively Binary Transmit Data and transmit clock) with BRD and RCLK (respectively Binary Receive data and its clock recovered).

4.3 LOOPBACK 3

LP3 Command (LP3 bit high, CR3 register) replaces BRD and RCLK (respectively Binary Receive Data and its clock recovered) with BXD and

XCLK (respectively Transmit Data and its clock associated). Frame and multiframe generated by the transmitter of the circuit are processed by the receiver of the circuit, without encoding and decoding.

4.4 LOOPBACK 4

LP4 Command replaces Data in with Data out near of DIN and DOUT pins (See LP4R register).

5 FRAME ALIGNMENT

Time slot 0 is used for the synchronization (G.706). At software Reset Frame and Multiframe are lost and a new research of FAS and MFAS is launched.

5.1 LOSS OF FRAME ALIGNMENT

Frame alignment will be assumed to have been lost :

– either when three consecutive incorrect frame alignment signals have been received,
– or when bit 2 in time slot 0 in odd frames has been received with an error, i.e. at 0, on three consecutive occasions,
– or when 915 errored CRC blocks out of 1000 have been detected.

5.2 FRAME ALIGNMENT RECOVERY

Frame alignment will be assumed recovered when the following sequence is detected:

– Detection of the correct Frame Alignment Signal, FAS
– detection of bit 2 of 32nd byte after FAS, at 1.
– detection of the correct Frame Alignment signal in the 64th byte after the first FAS detected.

5.3 MULTIFRAME ALIGNMENT RECOVERY

Multiframe Alignment will be assumed recovered when at least two valid multiframe alignment signals MFAS have been detected within 8 ms.

Table 1: CRC4 Multiframe Structure G.704

Sub Multiframe	Frame	TIME SLOT ZERO BIT NUMBERS							
		1	2	3	4	5	6	7	8
I	0	C1	0	0	1	1	0	1	1
	1	0	1	A	Sa4	Sa5	Sa61	Sa7	Sa8
	2	C2			F	A	S		
	3	0	1	A	Sa4	Sa5	Sa62	Sa7	Sa8
	4	C3			F	A	S		
	5	1	1	A	Sa4	Sa5	Sa63	Sa7	Sa8
	6	C4			F	A	S		
	7	0	1	A	Sa4	Sa5	Sa64	Sa7	Sa8
II	8	C1			F	A	S		
	9	1	1	A	Sa4	Sa5	Sa61	Sa7	Sa8
	10	C2			F	A	S		
	11	1	1	A	Sa4	Sa5	Sa62	Sa7	Sa8
	12	C3			F	A	S		
	13	E1	1	A	Sa4	Sa5	Sa63	Sa7	Sa8
	14	C4			F	A	S		
	15	E2	1	A	Sa4	Sa5	Sa64	Sa7	Sa8

FAS: Frame Alignment Signal in each even Time Slot.
MFAS: Multi Frame Alignment Signal 0 0 1 0 1 1
E1–E2: CRC4 error Indication bits
C1 to C4: Cyclic Redundancy Check 4 (CRC4) bits
A: Remote Alarm Indication
Sa4 to Sa8: Five bits in each odd Time Slot
Sa61 to Sa64: ETSI bits

5.3.1 Typical case

Remote entity transmits Frame Alignment Signal (FAS) and Multiframe Alignment Signal (MFAS).

As soon as lost of Frame Alignment is occured (LOF = 1), the local receiver recovers FAS from 254 up to 500µs after. As soon as FAS is recovered (LOF = 0), the local receiver recovers MFAS from 4 up to 6ms after.

5.3.2 Old Existing Equipment Case

Remote entity transmits Frame Alignment Signal (FAS) without Multiframe Alignment Signal (MFAS).
As soon as lost of Frame Alignment is occured (LOF=1), the local receiver recovers FAS from 254 up to 500µs after. Then LOF = 0, and 400ms after the local receiver indicates that the Multiframe Alignement Signal has not been recovered (MFNR = 1).

5.3.3 Particular Case: Spurious Frame Alignment Signal

Local receiver receives true FAS and true MFAS among several spurious FAS.

Multiframe Alignment signal (MFR=1) is recovered from 8 to 400ms after the Frame Alignment signal is recovered (LOF=0). Then, this FAS is either a spurious one (the "Spurious Time slot Zero" is carrying FAS without MFAS), or true FAS.

Anyway, when the Multiframe Alignment has been recovered (MFR=1), the good Frame Alignment Signal is taken into account and data are loaded into the Frame Memory at the good location.
See Fig. 13 synchronization algorithm.

5.3.4 Worst Case

Local receiver receives true FAS and true MFAS among several spurious FAS and several spurious MFAS.

In this case, if the circuit has recovered a spurious FAS and MFAS, the CRC blocks will be detected with an high error rate. As soon as 915 errored CRC block within 1000 will be detcted, the MFAS will be assumed as spurious and a new research starts at the point just after the location of the assumed spurious Frame Alignement Signal.

5.4 Transmitter SIDE

The Frame Alignement Signal is transmitted continuously on the transmitter side, with bit 1 of TS0 at logical 1. The MFAS signal is transmitted in accordance with NMF bit register (CR5 Register): if NMF is programmed to "1" Logic, no MFAS is transmitted; if NMF is programmed to "0" Logic the MFAS signal is transmitted continuously.

Table 2.

LOF	MFR	MFNR	RECEIVER STATE
1	0	0	FAS or MFAS has been lost. State: Research of FAS
0	0	0	FAS has been recovered. State: Research of MFAS
0	1	0	Frame and Multiframe recovered State: Good working.
0	0	1	Frame recovered. State: Good working without multiframe received from transmitting side.

6 Interfacing with the microprocessor

The device can work in one of the 3 following modes :

– Parallel microprocessor Interface Mode
– Serial microprocessor Interface Mode
– Without microprocessor : Stand Alone Mode.

The choice is done by means of the SA/Reset, P0 and P1 pins.

6.1 Parallel Microprocessor Interface Mode

The microprocessor can read (or write) the registers of the STLC5432 using the fifteen parallel Interface pins.

The use of TSO (Time Slot Zero) of DIN and DOUT digital multiplex is defined by TSOE bit of CR5 Register.

– If TSOE = 1, TSO on DIN multiplex Input is used to transfer Sa4 to Sa8 bits to the line and TSO on DOUT multiplex output is used to transfer Sa4 to Sa8 bits from the line.
– If TSOE = 0, DOUT output is high impedance during TSO, and DIN Input ignores data during TSO.

6.2 Serial Microprocessor Interface Mode

Fifteen parallel Interface pins are ignored, they are tied to ground. In this mode, the time slots 0 of internal multiplexes are considered like a channel used by the devices and the control entity located in the system to communicate. This channel can be switched across a switching network -or not- before its final destination.
The message is constituted by two bytes which are transmitted on two consecutive Time Slots Zero.
The bits of word are numbered 0 to 7, bit 0 is transmitted first. When the bit 7 of a byte is 0, this byte is the first word of the message.
The bit 6, of the first word, is R/W bit:
R/W = 1. Message to read a register whose address is designated by the following bits of the word (A 0/5).

R/W = 0. Message to write a register, addressed by the bits A0/5.
The bit 7 of following byte is 1 and the seven D 0/6 bits are data to load into register.
To transfer one message, 250µs are necessary.
Between two messages, the bits are 1 during TS0. See fig.7 for details.

6.2.1 Reading of a register

The remote entity connected to the DIN and DOUT multiplexes can request reading of a register if it transmits, during TSO, on DIN the address bit A0/5, the R/W bit at 1 and the last bit at 0. The following word, ending with 1, is not taken into account by the device. The device returns two words during TSO of DOUT :

–The first word begins with 0, R/W bit is put to 1, the address bits of the register are transmitted.

–The second word begins with 1, then seven data bits of the register are transmitted.

6.2.2 Writing of a register

The remote entity connected to the DIN and DOUT multiplexes can request writing, then it transmits the first bit at 0, the second bit at 0 and the register address A 0/5 during TSO of DIN. The following word begins with 1 and seven next bits are Data to load into register. There is no acknowledge after writing. The writing messages can be transmitted consecutively.

6.3 Stand Alone Mode

Whatever the received frequency on LCLK pin (2.048kHz or 4.096kHz), the device automatically fits and always works at 2.048kHz. When SA pin is at 1, the multiframe research is automatically launched after each lost of frame and the device provides the following alarms on DOUT during the Time Slot 0:

7							
F/S	SKIP	AR	MFNR	LOF	B	AIS	LOS

LOS	Loss of signal
AIS	Alarm Indication Signal
B	If LOF = 1, then B = 915 If LOF = 0, then B = WER
LOF	Loss of Frame
MFNR	Multi Frame Not Recovered
AR	A Bit Received
SKIP	Jump
F/S	Fast/Slow.

Bits definitions are the same than bits definitions of ALR, CAR1 and CAR2 Registers. These bits represent the current state of the line; DIN is ignored during Time Slot Zero.

7 RESET

During Hardware Reset (Pin : SA/RESET) :

– All the programmable registers are configurated with the default value.

– Interrupts are not generated ($\overline{INT}$ PIN is high impedance).

– The research of Multiframe is always active.

At Software Reset (addressing the Reset register):

– The registers are configurated with the default value only.

After Reset :

– The registers may be configurated with any value.

8 INTERRUPT

All the bits of Alarm Registers generate an interrupt if they are not masked, except SLC (CAR2).

An alarm generates an interrupt if the mask bit associated is 0. If a temporary event is detected from the line. ALR Alarm Register, CAR1 and CAR2 Complementary Alarm Registers can be read after interrupt or by polling.

In this last case, these Alarm Registers can be considered like particular status registers.

If a temporary event is detected from the line, then the appropriate bit is put to one. After reading by the microprocessor, this bit is put to zero until new event.

If a permanent state occurs, then the appropriate bit is put to one. After reading by the microprocessor, this bit remains at one until disappearance of the cause.

8.1 Parallel Interface Mode

ALR Alarm Register, CAR1 and CAR2 Complementary Alarm Registers can be read after interrupt or by polling.

In this last case, these Alarm Registers can be considered like particular status registers.

$\overline{INT}$ pin is put to 0 volt. The microprocessor reads Alarm Register.
For example, after reading the ALR and CAR1 registers the microprocessor could act as follows:

– If SC bit (clock 1 second) is 1, then the microprocessor reads fault counter registers.

– If EXT1 bit (EXTENSION 1) is 1, then the microprocessor reads Complementary Alarm Register 1.

– If TSOR (or Sa6R) bit of CAR1 is 1, the microprocessor reads TSORR (or Sa6RR) Register

8.2 Serial Interface Mode

When an Alarm bit is put to 1 in ALR (Alarm Register), this bit generates automatically the transmission of two bytes message onto DOUT during Time slot 0 with :

- The first bit of the first byte at 0; the second bit is at 0 and after the address bits of Alarm Register.
- The data of the ALR (Alarm Register) is the second byte.

NB : When TSOR or Sa6R bit of the CAR1 (Complementary Alarm Register 1) is put to "1", it generates a message in which there are address and data of TSORR Register (if TSOR bit is not masked), or address and data of Sa6RR register (if Sa6R is not masked).

If the four occurences to transmit a message are simultaneous, the priority order is:

Priority 1 :	Transmission of Alarm Register data if an alarm has been detected.
Priority 2 :	Transmission of Register data after reading message from remote entity.
Priority 3 :	Transmission of TSORR data after loading of this register.
Priority 4 :	Transmission of Sa6RR data after loading of this register.

8.3 Stand Alone Mode

Interrupts are not generated.
AL0, AL1 pins indicate the current state of three alarms : LOF, AIS, A bit received and DOUT pin indicates the current state of nine alarms during time-slot zero (See Par. 6.3).

Table 3: The registers and their bits.

ADD (Dec.)	After Reset (Hexa)	Register Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read/ Write	Page
0			NOT USED									
1		RESET	1	DUMMY REGISTER							W	15
2	88	ALR	1	EXT1	AR	SC	LOF	915	AIS	LOS	R	15
3	FF	AMR	1	MEXT1	MAR	MSC	MLOF	M915	MAIS	MLOS	R - W	15
4	80	CAR1	1	EXT2	0	Sa6R	TS0R	ER	CRCF	WER	R	15
5	FF	CAMR1	1	MEXT2	Nu	MSa6R	MTS0R	MER	MCRCF	MWER	R - W	15
6	80	CAR2	1	PRSL	PRSR	MFNR	MFR	0	SLC	SKIP	R	16
7	FF	CAMR2	1	MPRSL	MPRSR	MMFNR	MMFR	Nu	1	MSKIP	R - W	16
8	80	FCR1	1	F6	F5	F4	F3	F2	F1	F0	R	16
9	80	FCR2	1	F13	F12	F11	F10	F9	F8	F7	R	16
10	80	ECR1	1	E6	E5	E4	E3	E2	E1	E0	R	16
11	80	ECR2	1	E13	E12	E11	E10	E9	E8	E7	R	16
12	80	PCR1	1	P6	P5	P4	P3	P2	P1	P0	R	17
13	80	PCR2	1	P13	P12	P11	P10	P9	P8	P7	R	17
14	B8	ERTR	1	IT2	IT1	IT0	VT3	VT2	VT1	VT0	R - W	17
15	80	TS0RR	1	0	0	Sa4R	Sa5R	Sa6R	Sa7R	Sa8R	R	17
16	9F	Sa6RR	1	0	AR	Sa5R	Sa61R	Sa62R	Sa63R	Sa64R	R	17
17	X	RES	RESERVED: Avoid Addressing									
18	9F	TS0XR	1	WT	AE	Sa4X	Sa5X	Sa6X	Sa7X	Sa8X	R - W	18
19	8F	Sa6XR	1	WT	Nu	Nu	Sa61X	Sa62X	Sa63X	Sa64X	R - W	18
20	X	RES	RESERVED: Avoid Addressing									
21	90	SIGR	1	SHCR	SIG	STS4	STS3	STS2	STS1	STS0	R - W	18
22	80	LP4R	1	SLCR	LP4	LTS4	LTS3	LTS2	LTS1	LTS0	R - W	18
23	84	CR1	1	MERA	LTM	8KCR	MCR1	MCR0	SELEX	SELER	R - W	20
24	80	CR2	1	DOHZ	RDS1	RDS0	POL	NR	NX	TM	R - W	20
25	80	CR3	1	ASP	Nu	AISX	ALS	LP3	LP2	LP1	R - W	21
26	80	CR4	1	EQV	AVT	DEL	DCP	M2	M1	M0	R - W	21
27	80	CR5	1	TS0E	APD	NMF	HCRD	DPIS	CENTER	FROZ	R - W	23
28	80	CR6	1	POLSa	OSCD	SaT	Sa51	Sa50	Sa41	Sa40	R - W	23
29	80	CR7	1	AMI	Sa81	Sa80	Sa71	Sa70	Sa61	Sa60	R - W	24
30	FF	CR8	1	FILT	SP	Sa4P	Sa5P	Sa6P	Sa7P	Sa8P	R - W	24
31	X	RES	RESERVED: Avoid Addressing									
32	80	TCR1	1	SGV	GTS5	GTS4	GTS3	GTS2	GTS1	GTS0	R - W	25
33	80	TCR2	1	SAV	ATS5	ATS4	ATS3	ATS2	ATS1	ATS0	R - W	25
34	80	TCR3	1	CRCC	EBC	PELC	PULS	FASC	ODTS	TWI	R - W	26
35 to 63				Reserved for the die test: Avoid Addressing								

Nu = Not used.

9.1 Reset Register

7	0
1	Dummy Register

The software reset of the circuit is performed when this register is addressed whatever the value of its bits may be. Reading or writing is irrelevant. All the programmable registers are configurated by the default value indicated in each register description and the mechanism of multiframe is launched in accordance with the procedure described in the introduction.

9.2 ALR: Alarm Register

7							0
1	EXT1	AR	SC	LOF	915	AIS	LOS

After Reset = 88H

LOS Loss of Signal.
This bit is set to 1 when ten consecutive zeros have been detected before the HDB3/BIN decoder.

AIS Alarm Indication Signal:
this bit is set to 1 in accordance with G.775 when the incoming signal is recived with only two, or less, zero for two consecutive double frame period (i.e. 512 x 2 bit).

915 This bit is set to 1 when 915 errored CRC message blocks have been received within 1 second.

LOF Loss of Frame Alignment Word.
When at 1, the synchronization is lost.

SC One second Clock.
This bit is set to one every second when there is synchronization. The number of faults which have been counted during the previous second is in fault counters FCR, ECR and PCR.

AR A bit Received.
This bit is set to 1 when the bit 3 of the odd time slot zero has been received consecutively two times at 1.

EXT1 Extension bit 1.
This bit is set to 1 when one bit out of CAR1 Register bits is put to 1.

9.3 AMR Alarm Mask Register

7							0
1	MEXT1	MAR	MSC	MLOF	M915	MAIS	MLOS

After Reset = FFH

This register can be written or read.

When a bit of this register is set to 1, the corresponding bit of the ALR register, which has the same number, is masked and an interrupt cannot be generated by this bit.

9.4 CAR1: Complementary Alarm Register 1

7							0
1	EXT2	0	Sa6R	TS0R	ER	CRCF	WER

After Reset = 80H

WER Frame Word Error Rate.
This bit is at "1"when the threshold of fault condition has been reached; this bit is at "0" when the threshold of deactivating has been reached. These two thresholds are indicated by the error Rate Threshold Register (ERTR). The Error Rate function is validated when the synchronization is achieved.

CRCF CRC Frame.
After remultiframe time, this bit is at "1" when an eight frame block has been received with an error.

ER E Bit received.
ER bit is at "1" during the frame 13 received when the E1 bit value of the same frame 13 is zero.
ER bit is at "1" during the frame 15 received when the E2 bit value of the previous frame 15 is zero (E1 and E2 = first bit of time slot zero in frames 13 and 15 respective).

TS0R Time slot Zero Register.
This bit is at "1" when the TS0RR Register has been loaded in accordance withCR8 register and bit POLSa(CR6 register).

Sa6R Sa6R Register.
This bit is put to one when Sa6RR Register has been loaded in accordance with SaT bit (CR6 Register).

EXT2 EXTENSION Bit 2
This bit is at "1" when one bit out of CAR2 Register bits has been set to "1".

9.5 CAMR1 Complementary Alarm Mask Register 1

7							0
1	MEXT2	Nu	MSaRm	MTSOR	MER	MCRCF	MWER

At Reset = FFH

This register can be read or written.

When a bit of this register is at "1", the CAR1 Register bit which has the same number is masked. The CAR1 bit which is masked do not generate an interrupt.

9.6 CAR2: Complementary Alarm Register 2

7							0
1	PRSL	PRSR	MFNR	MFR	0	SLC	SKIP

After Reset = 80H

SKIP SKIP.
After frame recovery, this bit is at "1" when an entire frame (32 words) has been ignored or has been repeated two times onto DOUT.

SLC Slow Local Clock.
This bit does not generate interrupt.
When the value of this bit is 0, local clock is faster than the remote clock.
When the value is "1", local clock is slower than the remote clock (an entire frame has been ignored).

MFR Multiframe recovered within 400 ms.
After reframe time, if the multiframe is recovered within 400 ms, MFR is set to "1".

MFNR Multiframe Not recovered within 500 ms.
After reframe time, the circuit researches the multiframe during 500 milliseconds. After this time, if the multiframe has not been recovered, MFNR is set at "1". Then the circuit is activated with the frame recovery only, and the AX bit (bit 3 of the odd Time Slot Zero transmitted) is set at "0".

PRSR Pseudo Random Sequence Recovered.
When the PRS analyzer is validated (SAV = 1), PRSR bit is set at "1" if the synchronization is performed.

PRSL Pseudo Random Sequence Lost.
PRSL, this bit is set to "1" when PCR1/2 (PRS Counter Register) has reached 2^{14} detected faults.

9.7 CAMR2: Complementary Alarm Mask Register 2

7							0
1	MPRSL	MPRSR	MMFNR	MMFR	Nu	1	MSKIP

After Reset = FFH

This register can be read or written.
Bits: MMFNR, MMFR and MSKIP mask respectively bit MFNR, MFR and SKIP when they are at "1".

9.8 FCR1: Fault Counter Register 1

7							0
1	F6	F5	F4	F3	F2	F1	F0

After Reset = 80H

F0/6 7 less significant bits of the FCR counter.

9.9 FCR2: Fault Counter Register 2

7							0
1	F13	F12	F11	F10	F9	F8	F7

After Reset = 80H

F7/13 7 most significant bits of the FCR counter.

If POL bit of CR2 register is at "0", the value of 14 bits fault counter is loaded into these registers each second. If POL = 1, the registers are resetted after each access. (POL indicates the difference between polling mode and interrupt mode, see also CR2 register).

When the multiframe has not been recovered within 400ms (MFNR = 1), these two registers indicate the number of errored bits of Frame Alignment Signal received over one second period.

When the multiframe is recovered, these two registers indicate the number of errored CRC blocks received over one second period.

9.10 ECR1: E Bit Counter Register 1

7							0
1	E6	E5	E4	E3	E2	E1	E0

After Reset = 80H

E 0/6 7 less significant bits of ECR counter

9.11 ECR2: E Bit Counter Register 2

7							0
1	E13	E12	E11	E10	E9	E8	E7

After Reset = 80H

E 7/13 7 most significant bits of the ECR counter

.

ECR1 and ECR2 are two registers associated to ECR counter. Each second, the value of the counter is loaded into these register (POL = 0).

When the multiframe is recovered, these two registers indicate the number of errored E bits received over 1 second period.

9.12 PCR1: PRS Counter Register 1

7							0
1	P6	P5	P4	P3	P2	P1	P0

After Reset = 80H

P0/6 7 less significant bits of the Pseudo Random Counter Register.

9.13 PCR2: PRS Counter Register 2

7							0
1	P13	P12	P11	P10	P9	P8	P7

After Reset = 80H

P7/13 7 most significant bits of the Pseudo Random Counter Register.

PCR1 and PCR2 are two registers associated to Pseudo Random Sequence Counter.
When the Pseudo Random Sequence Analyser is validated, the counter indicates the number of erroneus bits received after the synchronisation of the Pseudo Random Sequence.

9.14 ERTR: Error Rate Threshold Register

7							0
1	IT2	IT1	IT0	VT3	VT2	VT1	VT0

After Reset = B8H

VT 0/3 Error Rate Validation Threshold of WER.
VT0/3 bits give the threshold of activating the indication of Alarm for erroneous Frame Alignment words.
WER is set to "1" only if the fault condition is confirmed within the following 2 seconds.

VT3	VT2	VT1	VT0	Number of erroneous Frame Alignement words received during 2 seconds
0	0	0	0	16
0	0	0	1	18
0	0	1	0	20
0	0	1	1	22
0	1	0	0	24
0	1	0	1	26
0	1	1	0	28
0	1	1	1	30
1	**0**	**0**	**0**	**32**
1	0	0	1	36
1	0	1	0	40
1	0	1	1	44
1	1	0	0	48
1	1	0	1	52
1	1	1	0	56
1	1	1	1	60

IT 0/2 Error Rate Inhibition Threshold of WER
IT 0/2 bits give the threshold of deactivating the indication of Alarm. Per default, WER is set at "0" when 12 or less erroneous Frame Alignment Words are detected.
The Alarm deactivation requires the confirmation of the condition for the following 2 sec.

IT2	IT1	IT0	Number of erroneous Frame Alignment words received during 2 seconds
0	0	0	8
0	0	1	9
0	1	0	10
0	**1**	**1**	**12**
1	0	0	14
1	0	1	16
1	1	0	20
1	1	1	24

NB: If the threshold value of deactivating the indication of Alarm is superior to threshold value of activating the indication of Alarm, then the value of deactivating is irrelevant.

9.15 TS0RR: Time Slot Zero Received Register

7							0
1	0	0	Sa4R	Sa5R	Sa6R	Sa7R	Sa8R

After Reset 80H

Sa4R to Sa8R Bits 4 to 8 of the odd Time Slot Zero (Sa4 to Sa8) received from the line. During reframe time, these bit are at "1". Sa4R to Sa8R fix the content of TS0RR in accordance with CR8 Register and bit POLSa (CR6 register)

9.16 Sa6RR: Sa6 Bits Receive Register

7							0
1	0	AR	Sa5R	Sa61R	Sa62R	Sa63R	Sa64R

After Reset = 9FH

Sa61R to Sa64R

These four bits are received from Sa6 subchannel.
When a new word constituted by these four bits is detected in accordance with SaT (CR6 Registers), a Sa6R interrupt is generated (a new word can occur each millisecond).

Sa5R. This bit is the same as Sa5R in TS0RR register.

AR A bit received. It's the same bit than the AR bit of ALR register (see 9.2).

9.18 TS0XR: Time Slot Zero transmit Register

7							0
1	WT	AE	Sa4X	Sa5X	Sa6X	Sa7X	Sa8X

After Reset = 9FH

Sa4X to Sa8X Bits 4 to 8 of each odd Time Slot Zero to be transmitted onto the line in accordance with CR6 and CR7

AE A bit to transmit.
AX bit to be transmitted onto the line is given by the logical "or" of LOF (Loss of Frame), WER (if the bit MERA is at 0, CR1 register) and AE (see fig 5).
AX(Odd TS0 Bit3) = AE + LOF + WER NOT MERA

WT Word to Transmit. This bit is read only.

First Case FILT = 1.
After TS0XR writing by microprocessor with WT = 1, WT is resetted at "0" after three consecutive transmissions of Sa4X to Sa8X bits onto the line.

Second Case FILT = 0.
After TSOXR writing by microprocessor with WT = 1, WT is resetted at "0" after one transmission of bits located in TS0XR register.

9.19 Sa6XR: Sa6 Bits Transmit Register

7							0
1	WT	Nu	Nu	Sa61X	Sa62X	Sa63X	Sa64X

After Reset = 8FH

Sa61X, Sa62X, Sa63X, Sa64X

These four bits are transmitted on subchannel Sa6 in accordance with CR6 and CR7 Registers.

WT Word to Transmit. This bit is read only.

First Case SaT = 1.
After Sa6XR writing by microprocessor, WT = 1. WT is resetted at "0" after three consecutive transmissions of Sa61X to Sa64X bits onto the line.

Second Case SaT = "0".
After Sa6XR writing by microprocessor, WT = 1, WT is resetted at "0" after one transmission of bits located in Sa6XR Register.

9.21 SIGR: Signalling Register

7							0
1	SHCR	SIG	STS4	STS3	STS2	STS1	STS0

After Reset = 90H

STS 0/4 Signalling Time Slot 0/4:
these five bits indicate which time Slot out of 32 to transmit and to receive on BRD0 and BXDI pins respectively, when SIG bit is at 1.

SIG Signalling Validated.

Receiver Side :

When SIG is at "1", the contents of Time Slot selected appear on the BRDO pin at 64 kb/s and its clock associated o the RCLO pin at 64kHz.

When SIG is at "0", the contentsof 32 Time slots received appear onto BRDO pin at 2 048 kb/s and clock associated onto RCLO pin at 2 048 kHz.

transmitter side :

When SIG is at "1", a bit stream at 64 kb/s on BXDI pin will be introduced into time Slot, selected by STS0 to STS4 bits, to the line. The bit stream on the input BXDI pin is clocked by clock at 64KHz delivered by BXDO pin (BXDI pin is an input and BXDO pin is an output).

When SIG is at "0", the bit stream at 2 048 kb/s on BXDI pin will be introduced into 32 Time Slots to the line.

SHCR: Synchronization of High Clock Received.
If DPIS (CR5) = 0:
SHCR = 1, DPLL receives RCLI signal from RCLI pin.
SHCR = 0, DPLL receives the remote clock recovered from the line.
If DPIS (CR5) = 1:
SHCR is not taken into account.

DPIS	SHCR	Source of the signal at the DPLL input:
0	0	line
0	1	RCLI pin
1	0	DPI pin
1	1	DPI pin

9.22 LP4R: Loop Back 4 Register

7							0
1	SLCR	LP4	LTS4	LTS3	LTS2	LTS1	LTS0

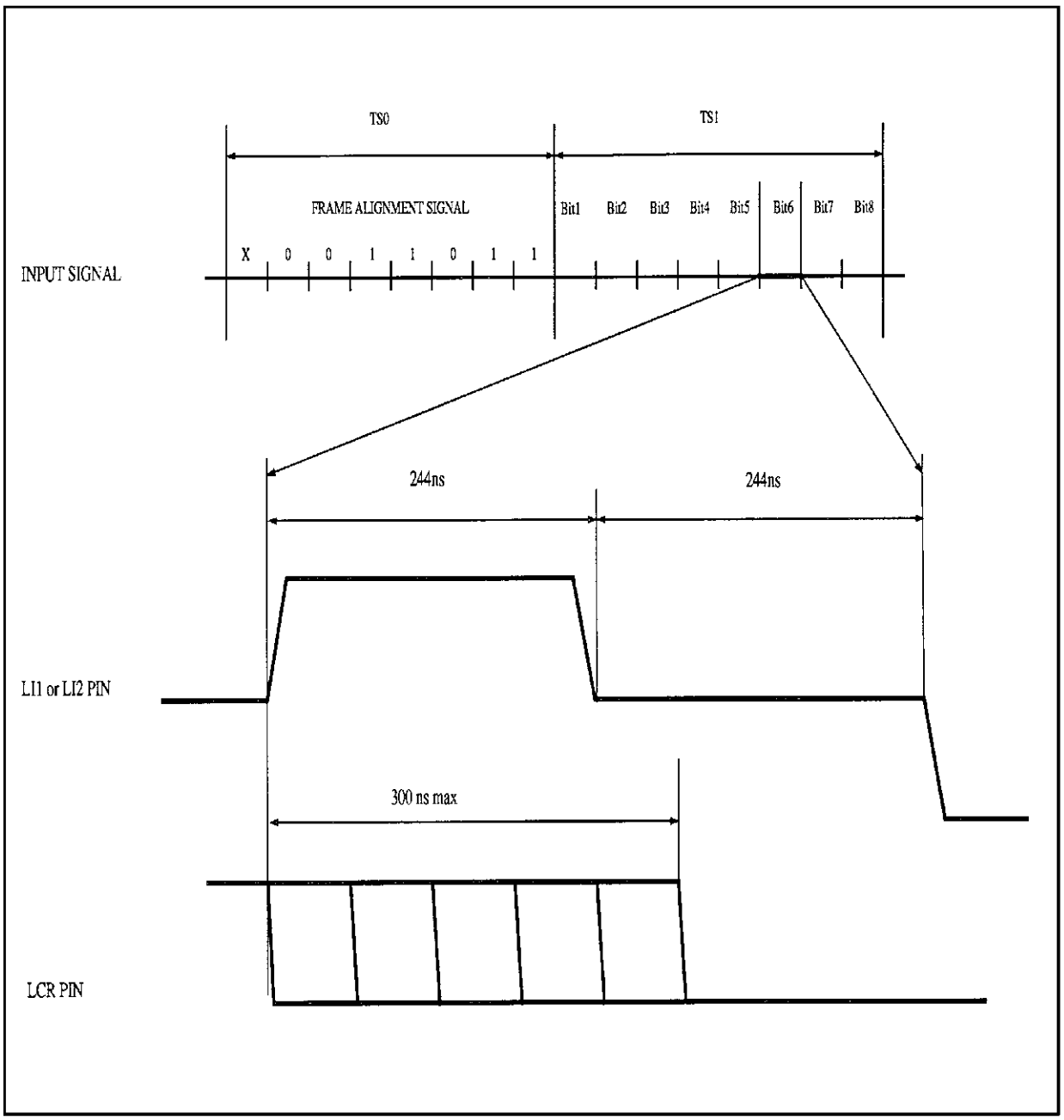
After Reset = 80 H

LTS 0/4 Loo Back time Slot 0/4:
these five bits indicate which time slot out of the 32 is selected for the loopback.

LP4 Loopback 4
When this bit is at "1", loop back 4 is validated during Time Slot selected. The loop back is located between DOUT and DIN pins. The loop back is transparent during the Time Slot selected. DOUT always delivers the contents of each Time Slot.

SLCR Synchronization of Low Clock Received
Relevant if LTM (CR1) = 0.
SLCR = 1, LCR output signal will be synchronized once when MFR bit (or MFNR bit) will go to "1". After synchronizing, the falling edge of LCR signal is in accordance with the 6th bit of time slot 1 seen at the input of the circuit. (LI1 pin or LI2 pin). The input signal is assumed without jitter.
SLCR = 0, LCR output signal is free. The LCR frequency is a submultiple of HCR frequency.

DELAY BETWEEN INPUT SIGNAL (LI1 OR LI2) AND OUTPUT SIGNAL (LCR) AT 8KHz AFTER SYNCHRONIZING (when SLCR = 1, LP4R Register Bit)



9.23 CR1: Configuration Register 1

7							0
1	MERA	LTM	8KCR	MCR1	MCR0	SELEX	SELER

After Reset = 84H

SELER Selection of an external signal side receiver.
When SELER=1, the internal binary data signal and its clock associated are replaced by the external binary data signal and its clock associated (respectively BRDI and RCLI).

SELEX Selection of an external signal side transmitter.
When SELEX = 1, the internal binary data signal is replaced by the external data signal BXDI.

MCR0/1 HCR Frequency
HCR pin delivers a square wave

MCR1	MCR0	HCR Frequency in kHz
0	0	2048
0	1	4096
1	0	8192
1	1	

8KCR 8kHz Clock Received

8KCR = 1
LCR pin delivers a square wave at 8kHz (Low clock received)

8KCR0 = 0
LCR pin delivers a square wave at 4kHz

LTM Line Termination Mode

When LTM is at "1", the jitter filter is not validated. HCR and LCR pins deliver signals at a submultiple frequency of the frequency applied to XTAL1 pin.
HCR frequency is in accordance with MCR0/1 and LCR frequency is in accordance with 8KCR.

When LTM is at "0", jitter filter is validated and MCR and LCR pins deliver cloks issued from DPLL in accordance with MCR0/1 and 8KCR.

MERA Mask Error rate

MERA = 0
WER bit (Error Rate over threshold) is taken into account to transmit A bit and to force to 1 the DOUTpin.

MERA = 1
WER bit is ignored by A bit transmission and DOUT pin.

9.24 CR2: Configuration Register 2

7							0
1	DOHZ	RDS1	RDS0	POL	NR	NX	TM

After Reset = 80H

TM Transparent Mode.

For the transmitter, when this bit is at 1, the bit stream received on DIN pin is introduced directly into the Binary HDB3 encoder.
In this case, FSX (Frame Synchronization Signal) from the pin is not used by the transmitter and Time Slot 0 is not known by the transmitter. The logical result is the same if the bit stream is introduced onto BXDI pin at 2048 kb/s.

For the receiver, when TM is at "1", every bit received from HDB3-BIN decoder is connected onto DOUT through the Elastic Memory. The synchronization is researched and indicated by the different alarm registers but DOUT pin delivers the received bit stream without taking into account the result of the synchronization.
BRDO and RCLO pins provide the bit stream received from the decoder.

NX PRBS Type to be transmitted.

When the generator of Pseudo Random Binary Sequency is validated (SGV =1):
if NX = 0, the length of sequence is 2*15-1 bits
if NX = 1, the length of sequence is 2*11-1 bits.

NR PRBS type received.

When the Analyzer of Pseudo Random Binary Sequence is validated (SAV = 1):
If NR = 0, the length of sequence received is 2*15-1 bits (O.151)
If NR = 1, the length of sequence received is 2*11-1 bits (O.152)

POL Fault Counter Register Polling.
POL = 1
FCR1 and FCR2 registers or ECR1 and ECR2 registers or PCR1 and PCR2 registers are read by the microprocessor (Polling Mode). First FCR1, or ECR1, or PRC1, is read then FCR2, or ECR2, or PRC2, mandatory. The contents of a pair of registers indicate the number of faults occured from the last reading of this pair of register.
POL = 0
The two pairs of registers indicate the number of faults occured during the second which is passed just before Interrupt SC.

RDS0/1 Receive Data Select Bit 0/1

When the PRS analyser is validated SAV = 1 (TCR2), Sequence is checked by the analyser during the Time Slot(s) selected by TCR2.

RDS1	RDS0	Source
0	0	Sequence comes from Memory input.
0	1	Sequence comes from memory Output.
1	0	Sequence comes from Data Input (DIN pin). Instead of sequence, "1" are transmitted onto the line.
1	1	Sequence comes from Data Input (DIN pin). Sequence is transmitted onto the line.

When the PRS generator is validated, SGV = 1 (TCR1 register), Sequence is transmitted by the generator during the Time Slot(s) selected by TCR1.

RDS1	RDS0	Destination
0	X	Sequence is transmitted onto the line. Loopback 1 or 3 can be validated.
1	X	Sequence is transmitted on Data Out (DOUT pin).

DOHZ DOUT High Impedance

DOHZ = 1, DOUT pin is high impedance
DOHZ = 0, DOUT pin is in accordance with TS0E bit of CR5 register.

9.25 CR3 Configuration Register 3

7							0
1	ASP	Nu	AISX	ALS	LP3	LP2	LP1

After Reset = 80H

LP1 Loop Back 1

This loop back is the nearest to the line side pins. If LP1 = 1 incoming data are replaced by outgoing data.
If AISX=0, loopback is transparent (outgoing data is transmitted)
If AISX=1, Alarm Indication Signal is transmitted.

LP2 Loop Back 2

Loopback located between the HDB3/BIN decoder output and the BIN/HDB3 encoder input. Loop back 2 is always transparent.
If LP2 = 1 Data received from the line are returned to the line.

LP3 Loop Back 3

If LP3 = 1 Frames and Multiframes generated by the emitter are connected instead of data stream coming from the decoder HDB3-BIN, just before frame memory input.

ALS Alarm Line Signal to be transmitted.

When this bit is at 1, AIS or APS are transmitted onto the line.

AISX Alarm Indication signal.

If ALS is at "1", and AISX is at "1":
Alarm Indication signal (All 1s) is transmitted onto the line.

If ALS is at "1" and AISX is at '0":
Auxiliary pattern (0-1-0-1-0-1...) is transmitted onto the line.

ASP Alternate Single Pulse

If ASP = 1 The L01 and L02 outputs deliver pulse every 3.9 microseconds. On the line, one will be positive, the next negative and so on.

9.26 CR4 Configuration Register 4

7							0
1	EQV	AVT	DEL	DCP	M2	M1	M0

After Reset = 80H

The first three bits of this register, M 0/2, must not be changed by the microprocessor if the serial µP is selected, they can be programmed only in parallel interface mode. If Serial interface or Stand Alone mode is chosen, then Multiplexes are at 2 048kb/s and local clock frequency may be either 2 048 kHz or 4 096 kHz.

NB : If parallel micro interface is selected, DOUT will be valid after writing CR4 Register.

M 0/2 Multiplex DIN and Multiplex DOUT

M2 = 1
Multiplexes are at 8 192 kb/s. Each multiplex includes 128 Time Slots. M0 and M1 indicate the Time Slots selected by the device.

M2 = 0 and M1 = 1
Multiplexes are at 4 096 kb/s. Each multiplex includes 64 Time Slots. M0 indicates the Time Slots selected by the device.

M2 = M1 = 0
Multiplexes are at 2 048 kb/s. Each multiplex includes 32 Time Slots.

DCP Double Clock Pulse

When this bit is at "1", local clock frequency value is twice the data rate value.
Data In are shifted on the second falling edge of the local clock (LCLK).
When this bit is at "0", local clock frequency and data rate value have same value.
Data in are shifted on the falling edge of the local clock.

DEL Delayed mode.

When DEL is at ”0”, Bit 0 of TS0 is indicated by the rising edge of Frame synchronization signal.
When DEL is at ”1”, Bit 0 of TS0 is delayed; the rising edge of Frame Synchronization indicates the bit located just before Bit 0 Time Slot 0.

AVT Adaptative Voltage Threshold Validation.
When AVT is at 1, the adaptive voltage threshold is validated.
When AVT = 0, the adaptive function is not validated; receiving is performed if the attenuation of the signal is less than 6 dB.

EQV Equalizer Validation.
When EQV is at ”1” internal equalizer is validated (external capacitors are required at the LI1 and LI2 inputs).
When EQV is at 0, the equalizer is never operating (external capacitors are not required).

TABLE OF DIFFERENT LOCAL MULTIPLEX (with Parallel microprocessor interface only)

CONFIGURATION BITS				**Local Clock**	**Multiplexes**	**DIN**	**DOUT**
M2	M1	M0	DCP	LCLK in kHz	Data Rate in Kb/s	Number of Time Slots (TS)	Time Slot in accordance with the TSn of the device $0 \leq n \leq 31$
0 0	0 0	0 0	0 1	2048 4096	2048	1 X 32	TSn
0 0	1 1	0 0	0 1	4096 8192	4096	2 X 32	TS 2n
0 0	1 1	1 1	0 1	4096 8192			TS 2n + 1
1 1	0 0	0 0	0 1	8192 16384	8192	4 X32	TS 4n
1 1	0 0	1 1	0 1	8192 16384			TS 4n + 1
1 1	1 1	0 0	0 1	8192 16384			TS 4n + 2
1 1	1 1	1 1	0 1	8192 16384			TS 4n + 3

Ex : M2 = 1, M1 = 1, M0 = 0, each Multiplex includes 128 Time Slots, the data processed by the device during the internal time Slot 3 are the data connected to multiplexes during the external time slot 14 = 4 X 3 + 2.

9.27 CR5 Configuration Register 5

7							0
1	TS0E	APD	NMF	HCRD	DPIS	CENTER	FROZ

After Reset = 80H

FROZ Frozen DPLL.

FROZ = 1, the DPLL is immediately frozen. Id est: DPLL retains its phase and its frequency while FROZ is at "1".

CENTER Crystal Oscillator Rference.

CENTER = 1, DPLL is synchronised by the Crystal Oscillator.
CENTER = 0, DPLL is synchronised by the clock recovered from the line or by the signal applied to DPLL INPUT PIN (DPI) in accordance with DPIS.

DPIS DPLL Input Selection.

DPIS = 1, internal DPLL input receives the signal applied to DPLL INPUT PIN (DPI)
DPIS = 0, internal DPLL input receives the signal recovered from the line.

HCRD HCR Disabled.

HCRD = 1, HCR pin is high impedance
HCRD = 0, HCR pin is low impedance.

NMF No Multiframe.

NMF = 1 the multiframe is not transmitted, only the Frame Alignement Signal (FAS) is transmitted on the line during the time slot 0. The receiver is not concerned by this bit.
NMF = 0 the multiframe (MFAS) is transmitted with the CRC4, the Frame Alignement Signal (FAS) is transmitted in accordance with G.704.

APD Alarm Pattern on DOUT.

When this bit is "1", DOUT Pin delivers Auxiliary Pattern: (0-1-0-1-0-1...).

TS0E DOUT enabled during Time Slot Zero.

In serial microprocessor mode, this bit is not significant: in this case Time Slot Zero is used to exchange data between the device and the remote serial interface microprocessor.
In parallel microprocessor mode,TS0E bit is taken into account:
TS0E =1.

Sa4R to Sa8R bits of the TS0RR Register are transmitted onto DOUT during the time Slot Zero. The bits 1 to 3 of this same time Slot Zero are ODD, SKIP, SLC.

- When ODD = 1, the contents of Time Slot 1 to 31 are relative to the contents of odd frame received from the line.
- When ODD = 0, the contents of Time Slot 1 to 31 are relative to the contents of even frame received from the line.

If the sinchronisation is lost or if the error rate is over the programmed threshold, the DOUT pin is set at "1".
The bits 4 to 8 of the incoming time Slot Zero (DIN pin) are transmitted onto the line in accordance with CR6 and CR7 Registers. Bits 1 to 3 are ignored.
TS0E = 0.

DOUT is high impedance during the time Slot Zero. Incoming bits on DIN pin are ignored during Time Slot Zero.

9.28 CR6 Configuration Register 6

7							0
1	POLSa	OSCD	SaT	Sa51	Sa50	Sa41	Sa40

After Reset = 80H

Sa40/Sa41

Sa41	Sa40	For Subchannel Sa4 in Transmission, the source is:	For Subchannel Sa4 in Reception, the destination is:
0	0	Bit Sa4X of TS0XR Register	TS0RR Register receives Bit Sa4R and DOUT pin delivers Bit Sa4R.
0	1	Bit Sa4X of DIN received during TS0	
1	0	Reserved Code: Do not use	
1	1	Reserved Code: Do not use	

Sa50/Sa51

Sa51	Sa50	For Subchannel Sa5 in Transmission, the source is:	For Subchannel Sa5 in Reception, the destination is:
0	0	Bit Sa5X of TS0XR Register	TS0RR Register receives Bit Sa5R and DOUT pin delivers Bit Sa5R.
0	1	Bit Sa5X of DIN received during TS0	
1	0	Reserved Code: Do not use	
1	1	Reserved Code: Do not use	

SaT Same Bits Three times.

SaT = 1: if a new value for the Sa5R, Sa61R, Sa62R, Sa63R and Sa64R bits has been received three times identical, these bits are loaded into Sa6RR register and a Sa6R interrupt is generated.

SaT = 0: each millisecond the Sa5R, Sa61R, Sa62R, Sa63R and Sa64R bits are loaded into Sa6RR register and a Sa6R interrupt is generated.

Transmitter side:
SaT fixs the number of consencutive transmissions of Sa61 to Sa64 bits onto the line before resetting WT (Sa6XR register). See definition of WT bit in chapter 9.19

OSCD Oscillator Disabled

OSCD = 1, The clock pulse applied to XTAL1 input pin comes from an external generator. The internal oscillator is disabled to reduce power consumption.
XTAL2 pin has to be left open.

OSCD = 0, The two pins of a crystal are connected to XTAL1 pin and XTAL2 pin in accordance with the application schematic and the internal oscillator is enabled.

POLSa = 1: Each bit of TS0RR register is reset after a reading cycle from microprocessor except if the condition to set the bit at "1" is still present.

POLSa = 0: Each bit of TS0RR Register is always reset after a reading cycle from microprocessor. (see also SP bit of CR8 Register).

9.29 CR7 Configuration Register 7

7							0
1	AMI	Sa81	Sa80	Sa71	Sa70	Sa61	Sa60

After Reset = 80H

Sa60/Sa61

Sa61	Sa60	For Subchannel Sa6 in Transmission, the source is:	For Subchannel Sa6 in Reception, the destination is:
0	0	Bit Sa6X of TS0XR Register	Sa60 and Sa61 are not taken into account: TS0RR Register receives Bit Sa6R and DOUT pin delivers Bit Sa6R
0	1	Bit Sa6X of DIN received during TS0	
1	0	Contents of Sa6XR Register	Sa6RR Register
1	1	Reserved Code: Do not use	

Sa70/Sa71: same definition as Sa40/Sa41.
Sa80/Sa81: same definition as Sa40/Sa41.

AMI Alternate Mark Inversion.

AMI = 0, select HDB3 code on the line.
AMI = 1, select AMI code on the line.

9.30 CR8 Configuration Register 8

7							0
1	FILT	SP	Sa4P	Sa5P	Sa6P	Sa7P	Sa8P

After Reset = FFH

Sa8P Sa8 Bit Polarity. This bit is taken into account if SP =1.

Sa8P =1, Sa8R bit (of TS0RR Register) is set at "1", in accordance with FILT, when Sa8 bit received from the line goes from "0" to "1".

Sa8P =0, Sa8R bit (of TS0RR Register) is set at "1", in accordance with FILT, when Sa8 bit received from the line goes from "1" to "0".

Sa7P to Sa4P Same definition as Sa8P

SP Single Polarity

SP =1, Sa8P to Sa4P and POLSa (CR6 Register) bits are taken into account. Sa8 to Sa4 (changing state) received from the line are stored into TS0RR Register in accordance with FILT. When TS0RR Register is read by the microprocessor, TS0RR is put to 0 in accordance with POLSa bit (CR6 register).

SP = 0, Sa8P to Sa4P and POLSa bits are not taken into account.
Sa8 to Sa4 bits received from the line are stored into TS0RR Register in accordance with FILT. When TS0RR Register is read by the microprocessor, TS0RR keeps its contents.

FILT FILTERING
Receiver side:

FILT = 1 and SP = 1,
Sa8R to Sa4R bits of TS0RR Register are set at "1" respectively if a new state has been received three times consecutively from each channel Sa8 to Sa4 processed separately one by one. A TS0R interrupt is generated.

FILT = 0 and SP = 1,
Sa8R to Sa4R bits of TS0RR Register are set at "1" respectively if a new state has been received twice consecutively from each channel Sa8 to Sa4 processed separately one by one. A TS0R interrupt is generated.

FILT = 1 and SP = 0,
Sa8 to Sa4 bits received from the line and processed independently are stored into TS0RR Register if one new bit has been received three times identically at least. A TS0R interrupt is generated.

FILT = 0 and SP = 0,
Sa8 to Sa4 bits received from the line are stored into TS0RR Register each 250ms without processing. A TS0R interrupt is generated.

Transmitter side:
See TS0XR register definition chapter 9.18.

9.32 TCR1: Test Configuration Register 1

7 0

1	SGV	GTS5	GTS4	GTS3	GTS2	GTS1	GTS0

After Reset = 80H

GTS0 to GTS5 Time Slot associated to generator. These 6 bits indicate Time Slot(s) selected to transmit the Pseudo Random Binary Sequence (PRBS) provided by the internal generator (see Table).

SGV Sequence Generator Validated. When SGV is at "1", the generator provides Pseudo Random Binary Sequence in accordance with NX bit. When SGV is at 0, the generator is not validated.

GTS5	GTS4	GTS3	GTS2	GTS1	GTS0	Time Slot(s) selected to transmit PRBS
0	0	0	0	0	0	All the Time Slots except TS0
0	X	X	X	X	1	All the Time Slots including TS0
1	0	0	0	0	0	Not use
1	0	0	0	0	1	TS1
1	0	0	0	1	0	TS2
↓	↓	↓	↓	↓	↓	↓
1	1	1	1	1	0	TS30
1	1	1	1	1	1	TS31

9.33 TCR2: Test Configuration Register 2

7 0

1	SAV	ATS5	ATS4	ATS3	ATS2	ATS1	ATS0

After Reset = 80H

ATS0 to ATS5 Time Slot associated to Analyzer. These 6 bits indicate Time Slot(s) selected to receive the Pseudo Random Binary Sequence (PRBS). The internal analyzer checks the sequence.

SAV Sequence Analyzer Validated. When SAV is at "1", the analyzer is validated and the counter ECR1-ECR2 (14 bits) is associated to analyzer. The length of PRBS is in accordance with NR bit. After the sequence is recovered by the analyzer. PRSR is set at "1" (Complementry Alarm Register); the associated counter indicates the number of faults received.

ATS5	ATS4	ATS3	ATS2	GTS1	GTS0	Time Slot(s) selected to receive PRBS
0	0	0	0	0	0	All the Time Slots except TS0
0	X	X	X	X	1	All the Time Slots including TS0
1	0	0	0	0	0	Not use
1	0	0	0	0	1	TS1
1	0	0	0	1	0	TS2
↓	↓	↓	↓	↓	↓	↓
1	1	1	1	1	0	TS30
1	1	1	1	1	1	TS31

9.34 TCR3 Test Configuration Register 3

7							0
1	CRCC	EBC	PELC	PULS	FASC	ODTS	TWI

After Reset = 80H

TWI TSO corrupted TWICE.
If FASC=1 and TWI=1, Time Slot 0 selected by ODTS is corrupted twice only.
If FASC=1 and TWI=0, Time Slot 0 selected by ODTS is corrupted three times only.

ODTS Odd Time Slot 0
If FASC=1 and ODTS=1, Odd Time Slot zero is transmitted with Bit 2 at "0".
If FASC=1 and ODTS=0, Even Time Slot Zero is transmitted with Bit 2 at "1".

FASC Frame Alignment Signal Corrupted.
In accordance with ODTS and TWI.
If FASC=1, Time Slot 0 transmitted is corrupted. After transmitting twice or three times consecutively, FASC changes from "1" to "0".

PULS PULSE
First case : SGV = 0 (TCR2 Register)
If PELC=1 and PULS=1, 512 consecutive pulses are transmitted on the line during frame 0 and frame 1. If PELC=1 and PULS=0, no pulses are transmitted during 16 time-bit (7,8 microseconds).
Second case : SGV = 1 (TCR2 Register) PULSE is ignored; if PELC changes "0" to "1", one pseudo random sequence bit transmitted is corrupted. After transmitting corrupted bit, PELC changes "1" to "0".

PELC Pulses transmitted on the line are corupted in accordance with PULS and SGV (TCR2 Register). After transmitting once time, PELC changes from "1" to "0".

EBC E Bit Corrupted.
If EBC=1, E bit of the next frame 13 and E bit of the next frame 15 will be transmitted at "0". After transmitting once time, EBC changes from "1" to "0".

CRCC CRC4 corrupted
When CRCC is at "1", CRC4 transmitted into multiframe is continuously corrupted.

Figure 3: Connections with and without Internal Equalizer.

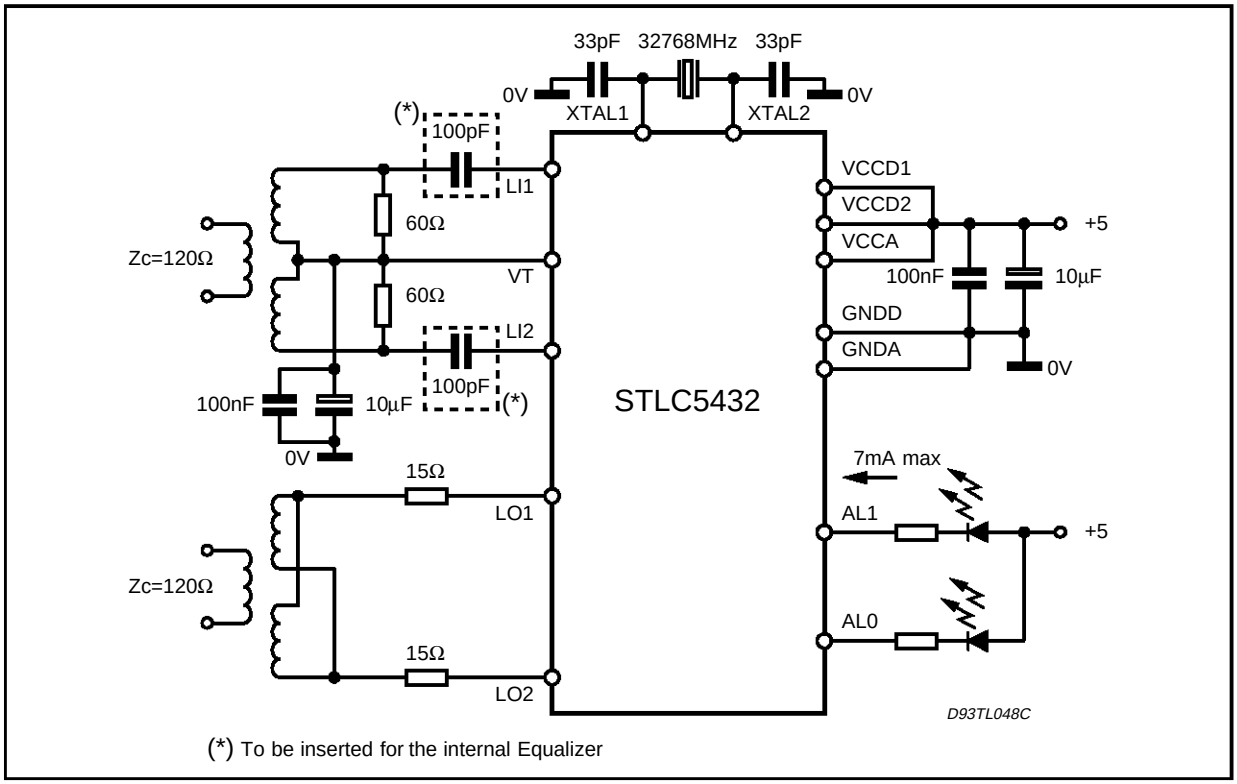


Figure 4: STLC5432 Line Interface Configurations (CEPT 120Ω or 75Ω)

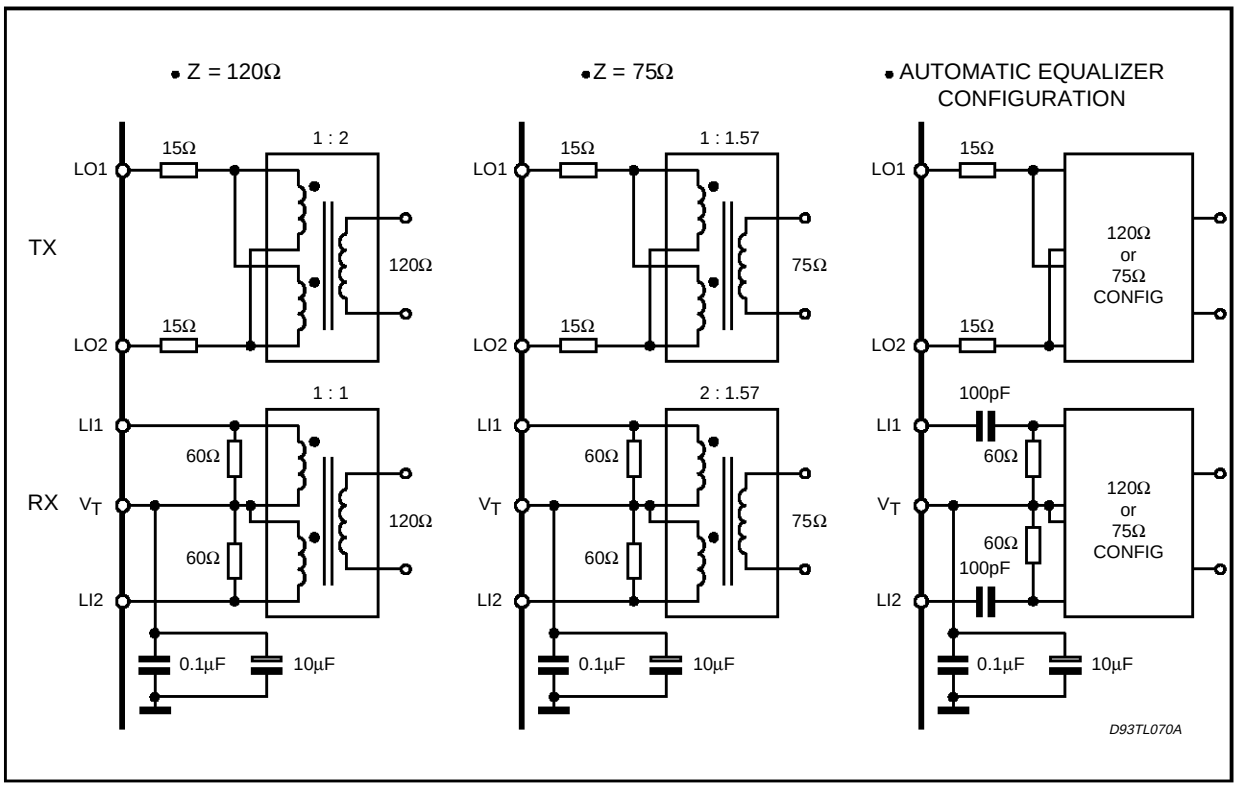


Figure 5: Main Alarm Processing

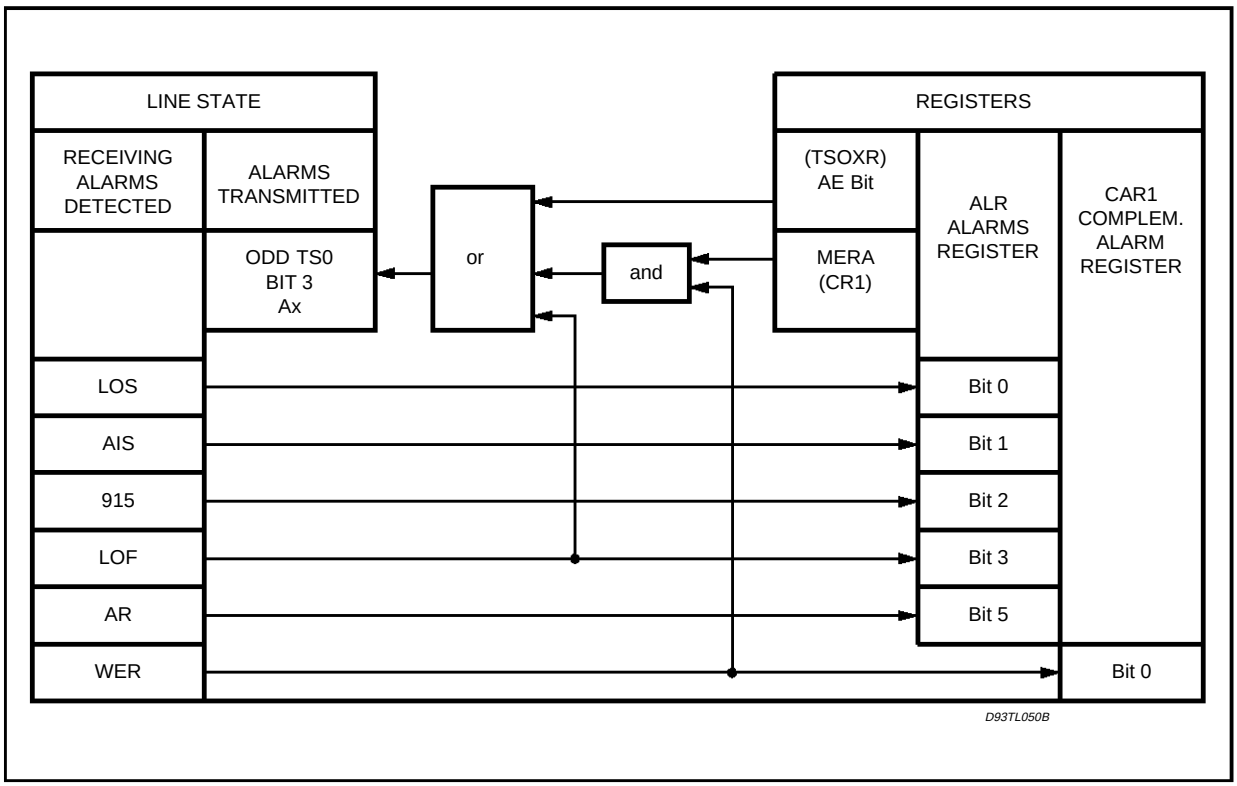


Figure 6: DIN and DOUT During Time slot 0.

SA pin: 0V		SA pin: 5V
Serial Interface P0 + P1 = 0	Parallel Interface: P0 + P1 # 0	Stand Alone
During Time Slot 0:	IF TSOE = 0 (CR5) During Time Slot 0: Dout pin is High Z.	
Dout pin delivers messages and Din pin receives messages	IF TSOE = 1 During Time Slot 0: Dout pin delivers consecutively: ODD | SKIP | SLC | Sa4R | Sa5R | Sa6R | Sa7R | Sa8R ODD = 1 The contents of 31 Time Slots is related to odd frame received from the line. ODD = 0 The contents of 31 Time Slots is related to even frame received from the line. (See Figure 6a).	During Time Slot 0: Dout pin delivers eight alarms SLC | SKIP | AR | MFNR | LOF | B | AIS | LOS
	Din pin receives eight bits: X | X | X | Sa4E | Sa5E | Sa6E | Sa7E | Sa8E	Din pin is ignored during Time Slot 0

D93TL051E

Figure 6a: DOUT during Timeslot 0 (Bits 1 to 3) when TS0E = 1 (CR5)

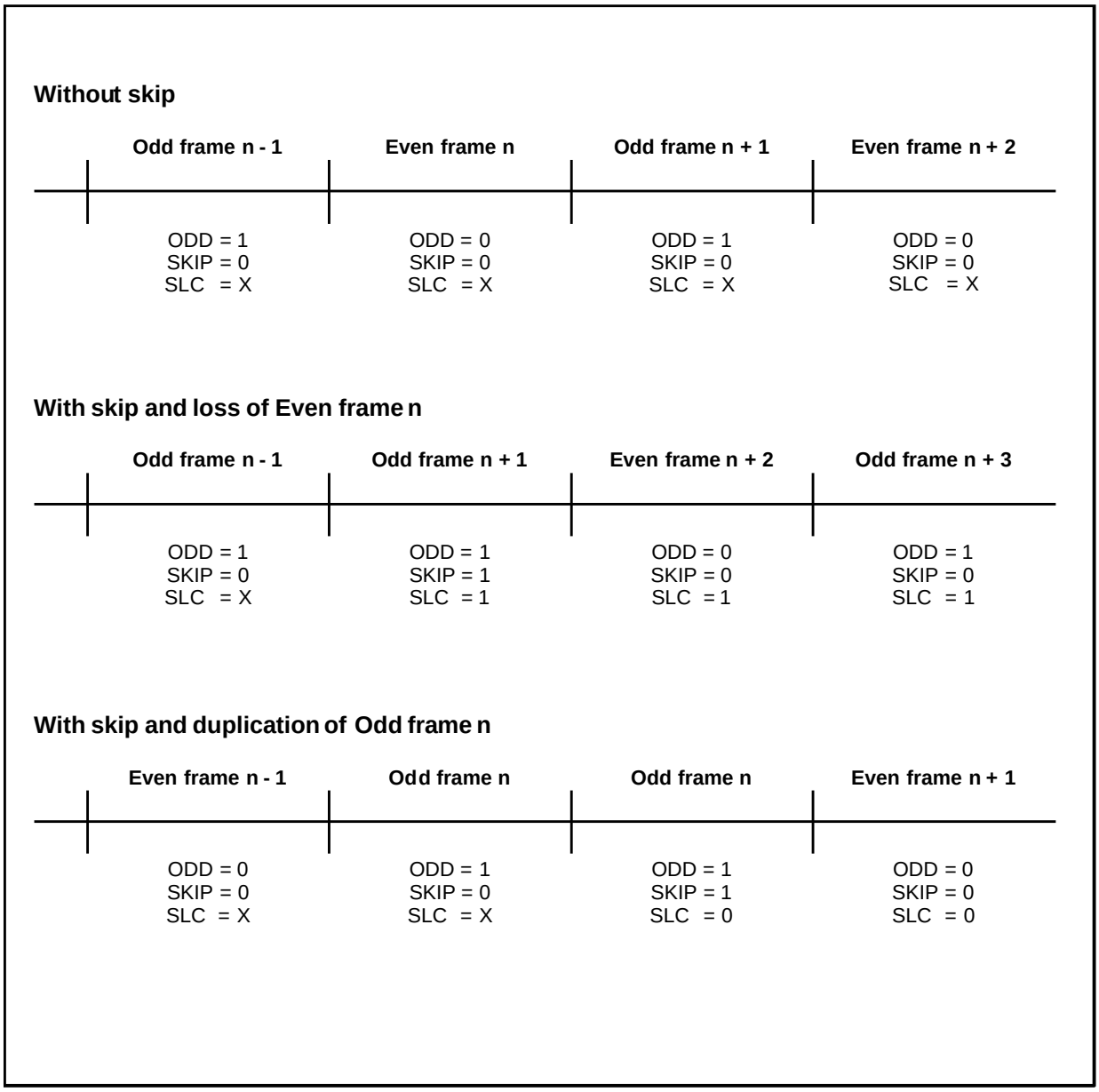


Figure 7: DIN/DOUT multiplex during Time Slot 0 - Serial Microprocessor Interface Mode.

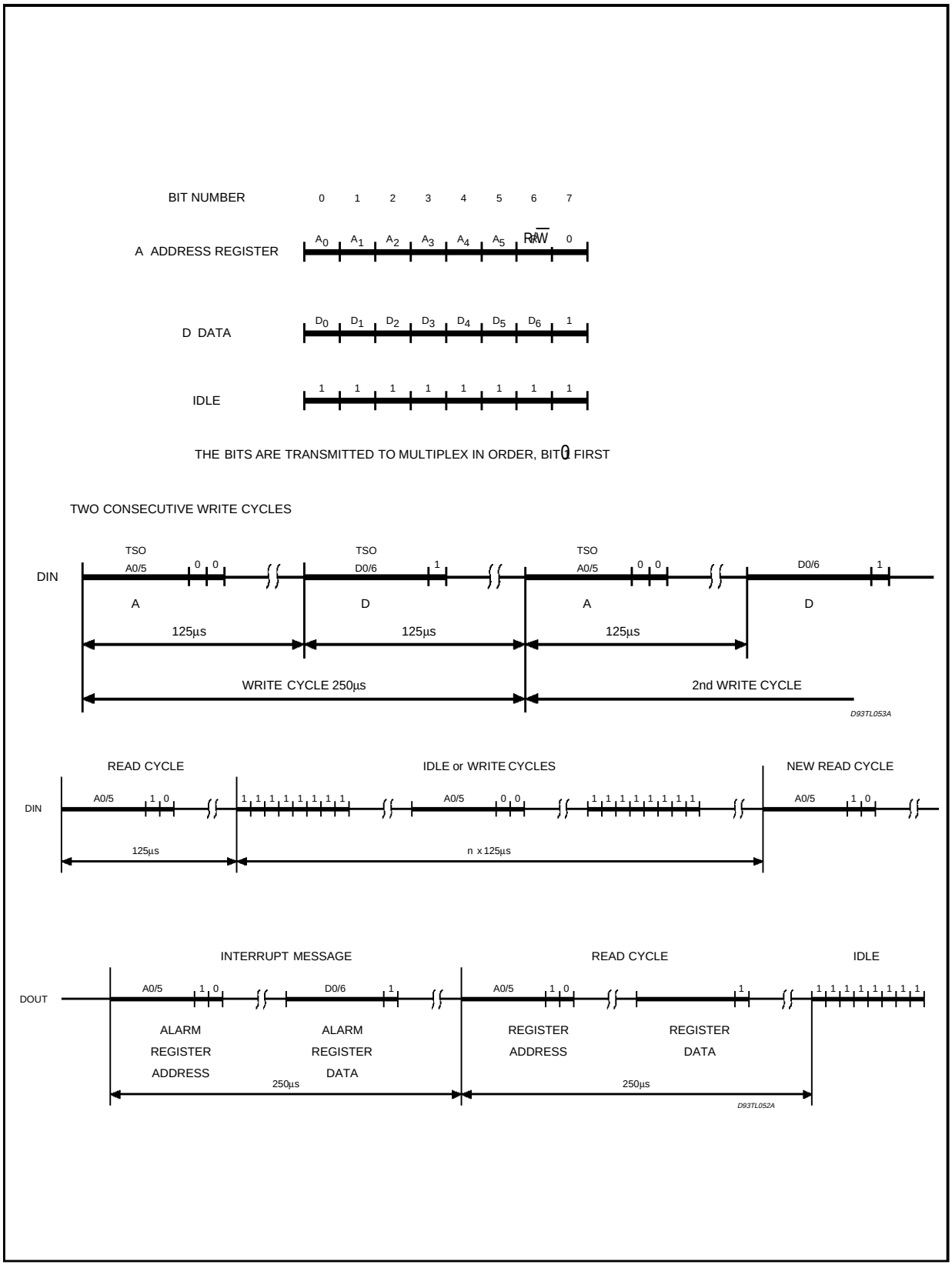
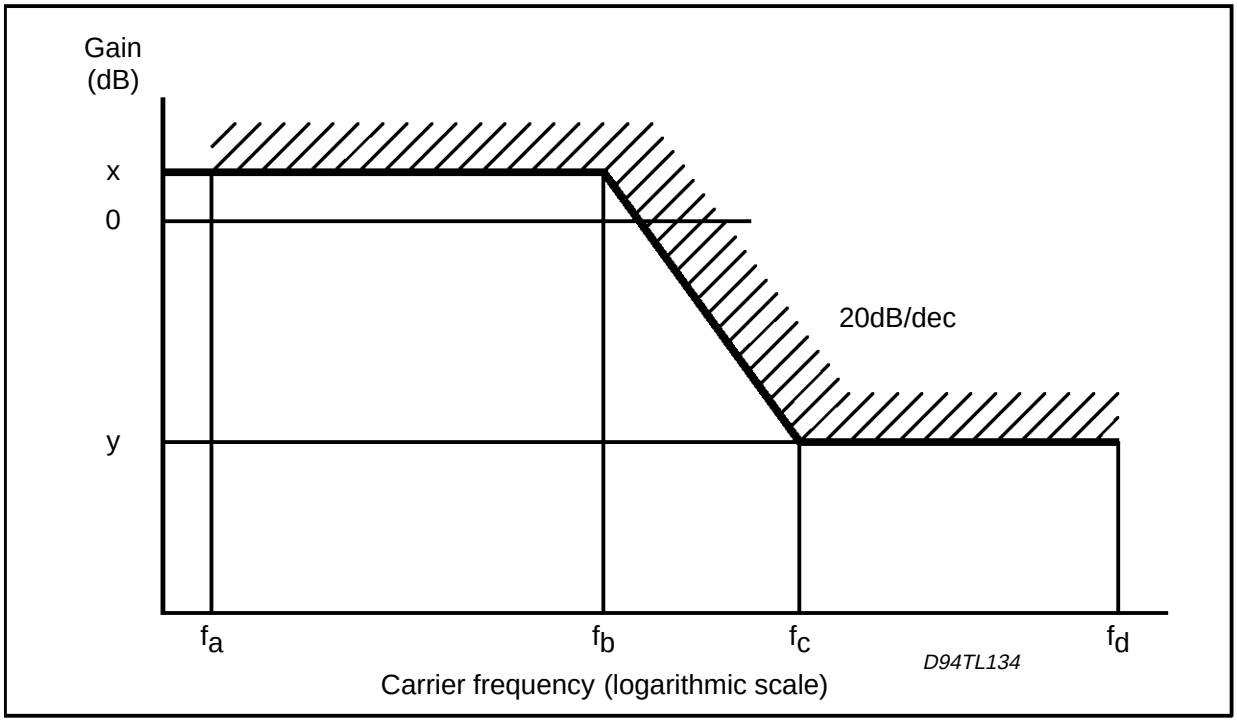


Figure 8: Jitter Transfer Characteristic (CCITT I431)



Y	X	f_a	f_b	f_c	f_d
–19.5dB	0.5dB	10Hz	40Hz	400Hz	100kHz

Figure 9: Level 1 - Level 2 Process with Parallel Interface µP.

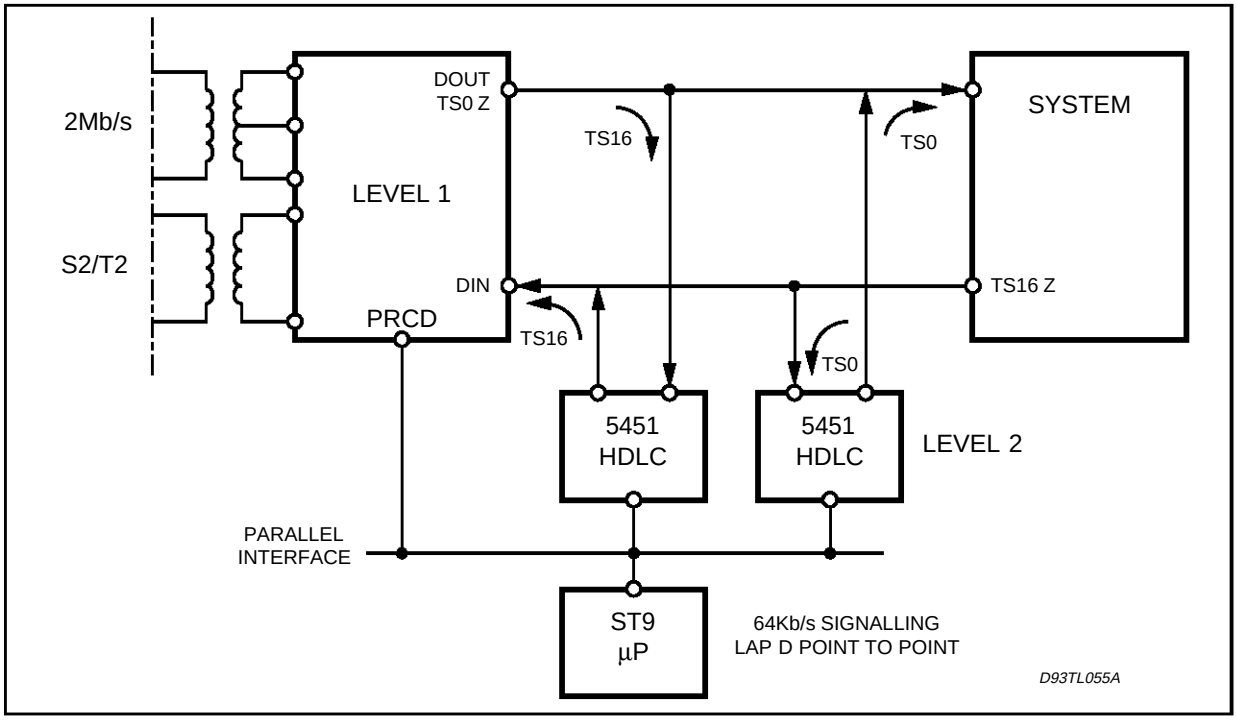


Figure 10: Primary Rate Controller Device PRCD - TE mode with serial Microprocessor

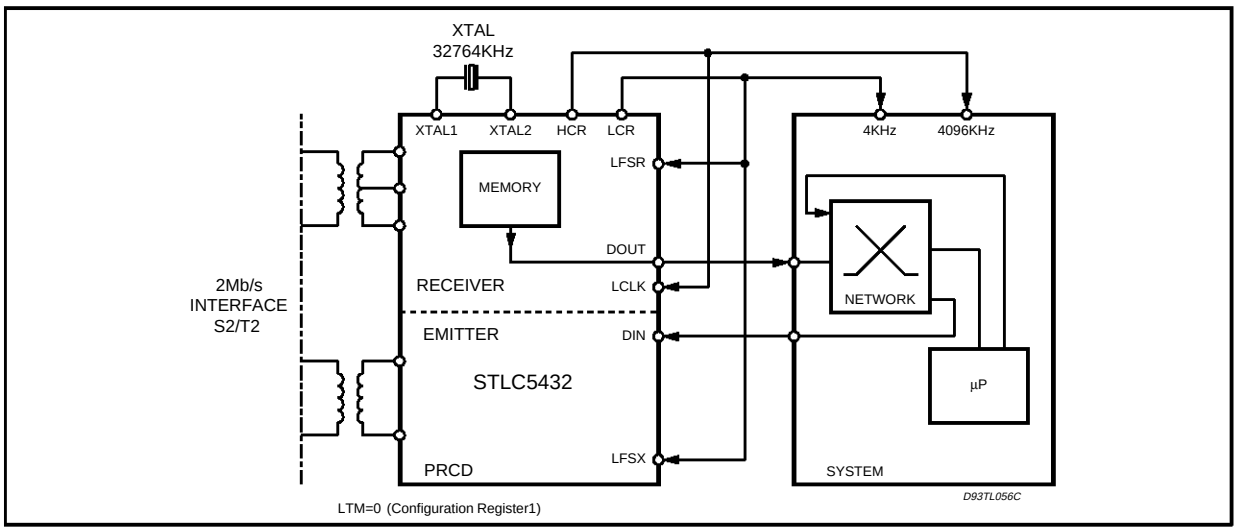


Figure 11: Four STLC5432 in LT Mode

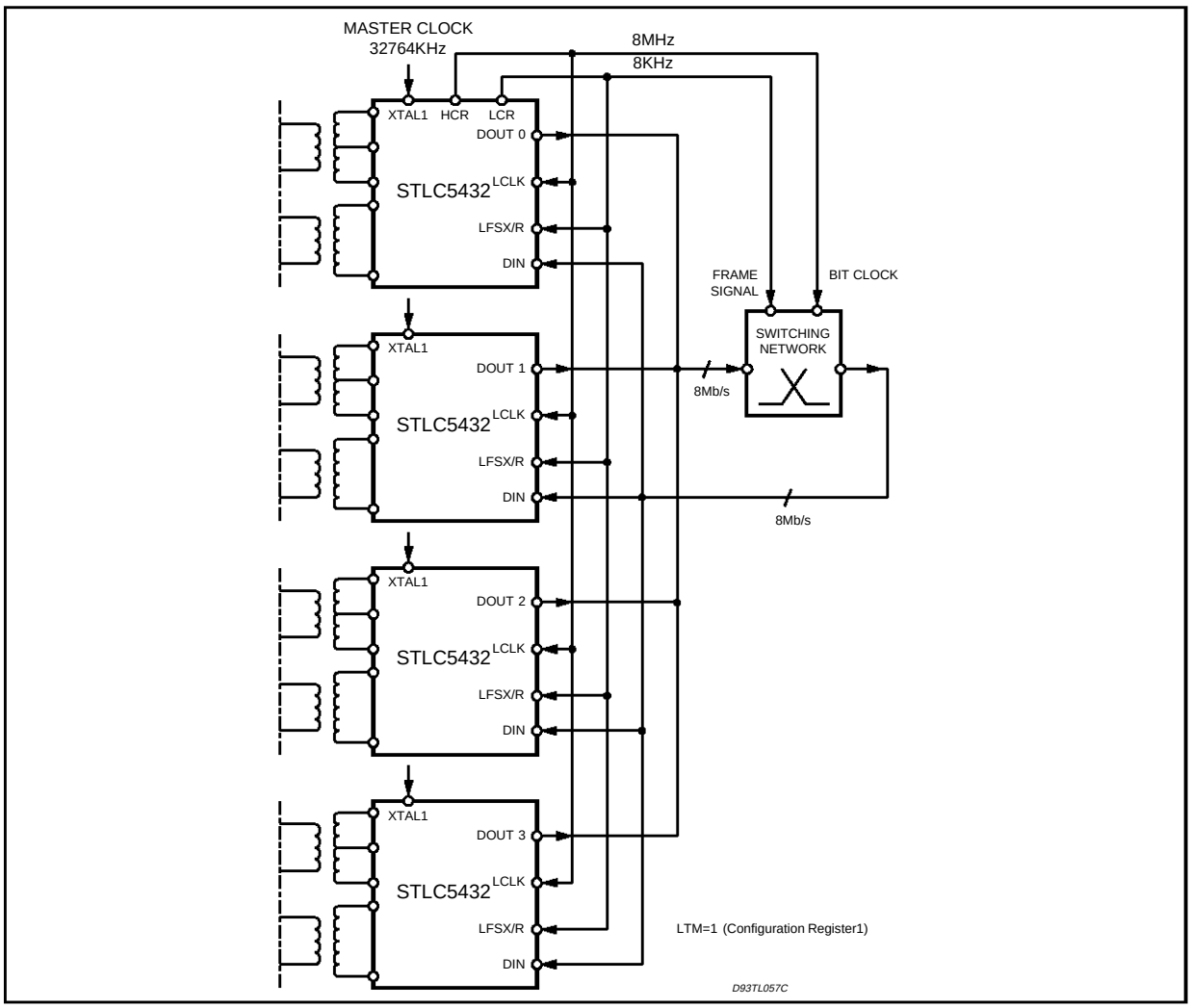


Figure 12: ETSI NT1 Option 2

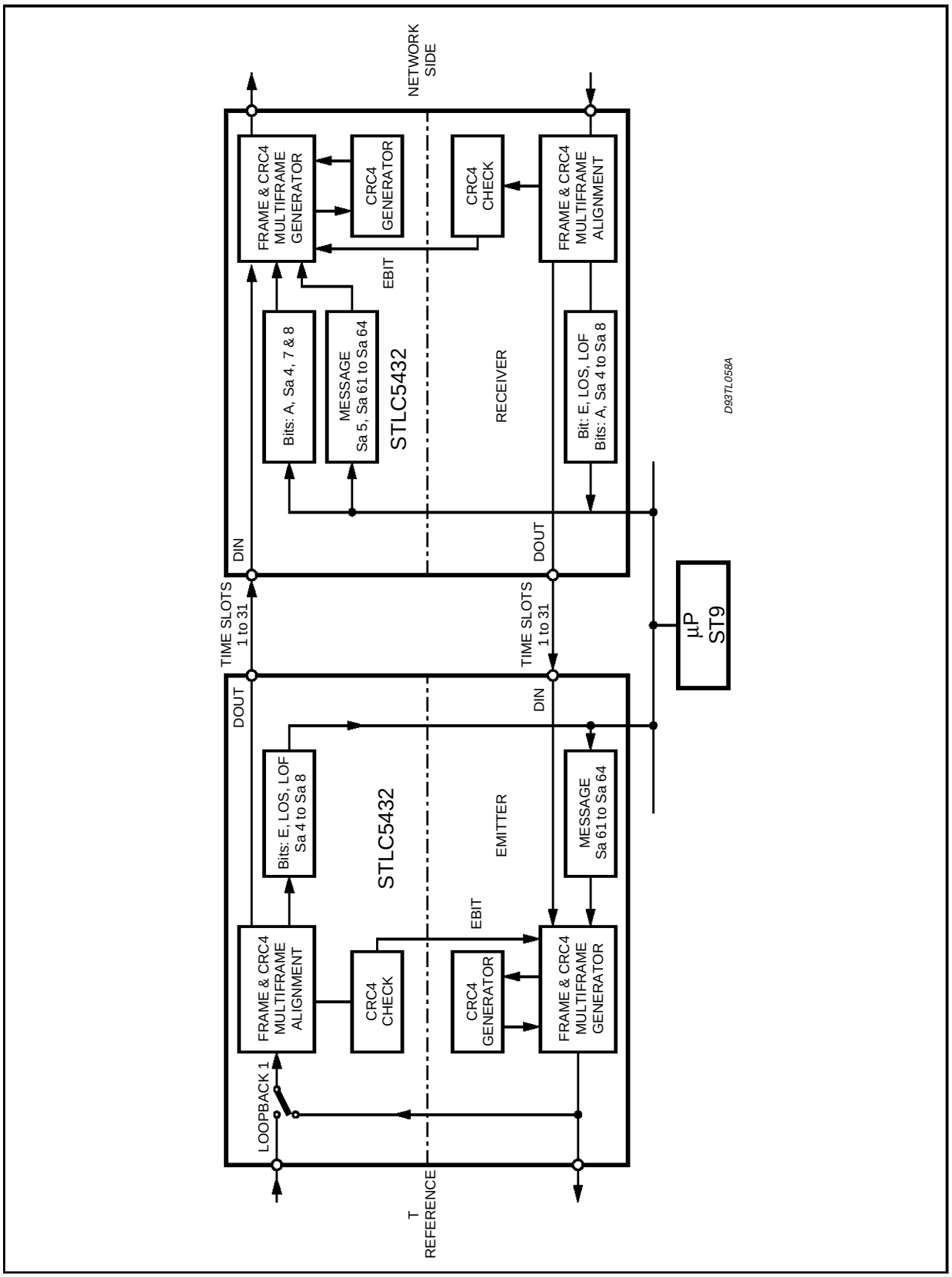


Figure 13: Synchronization Algorithm

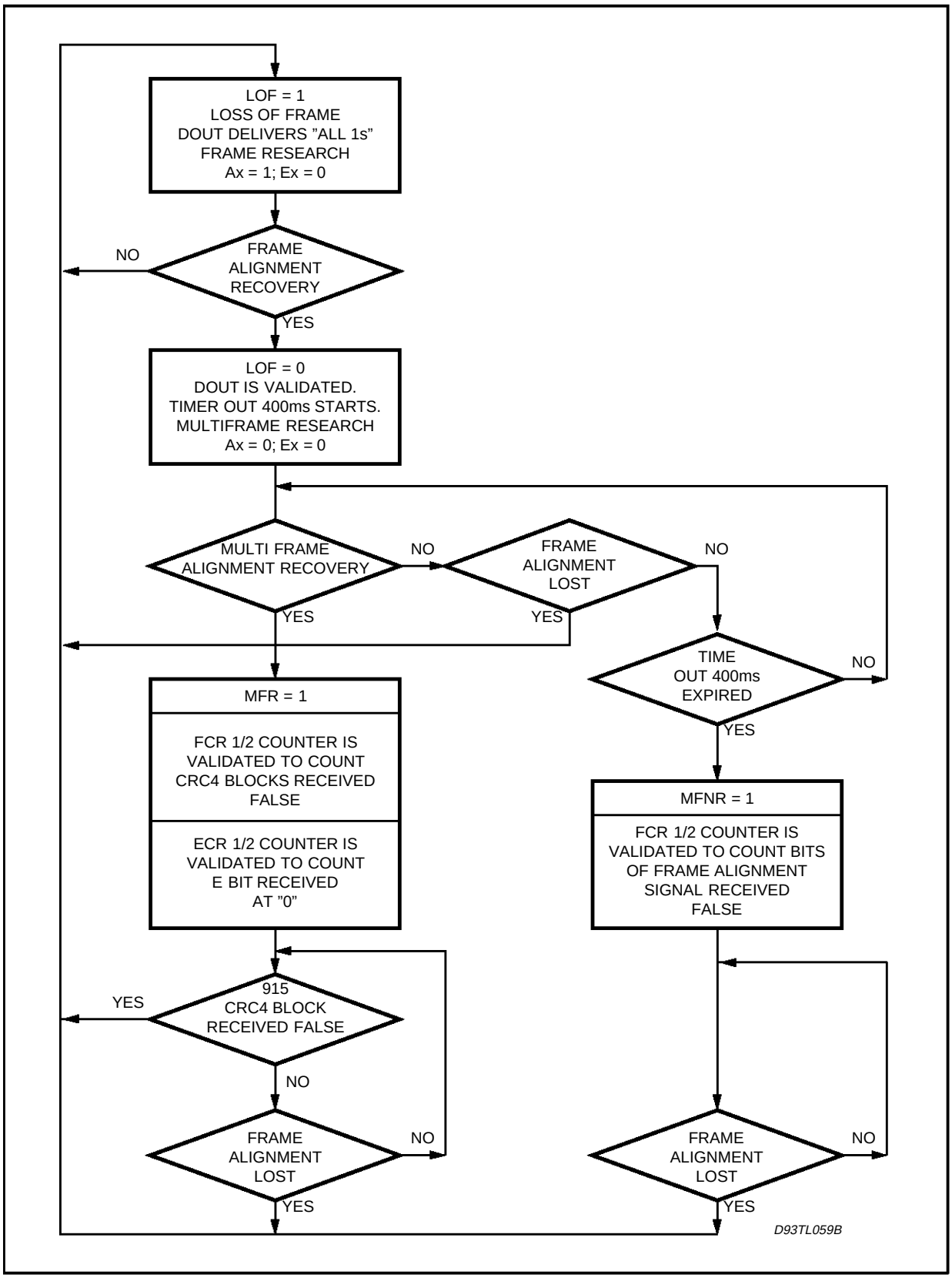


Figure 14: Three Cases of Synchronization.

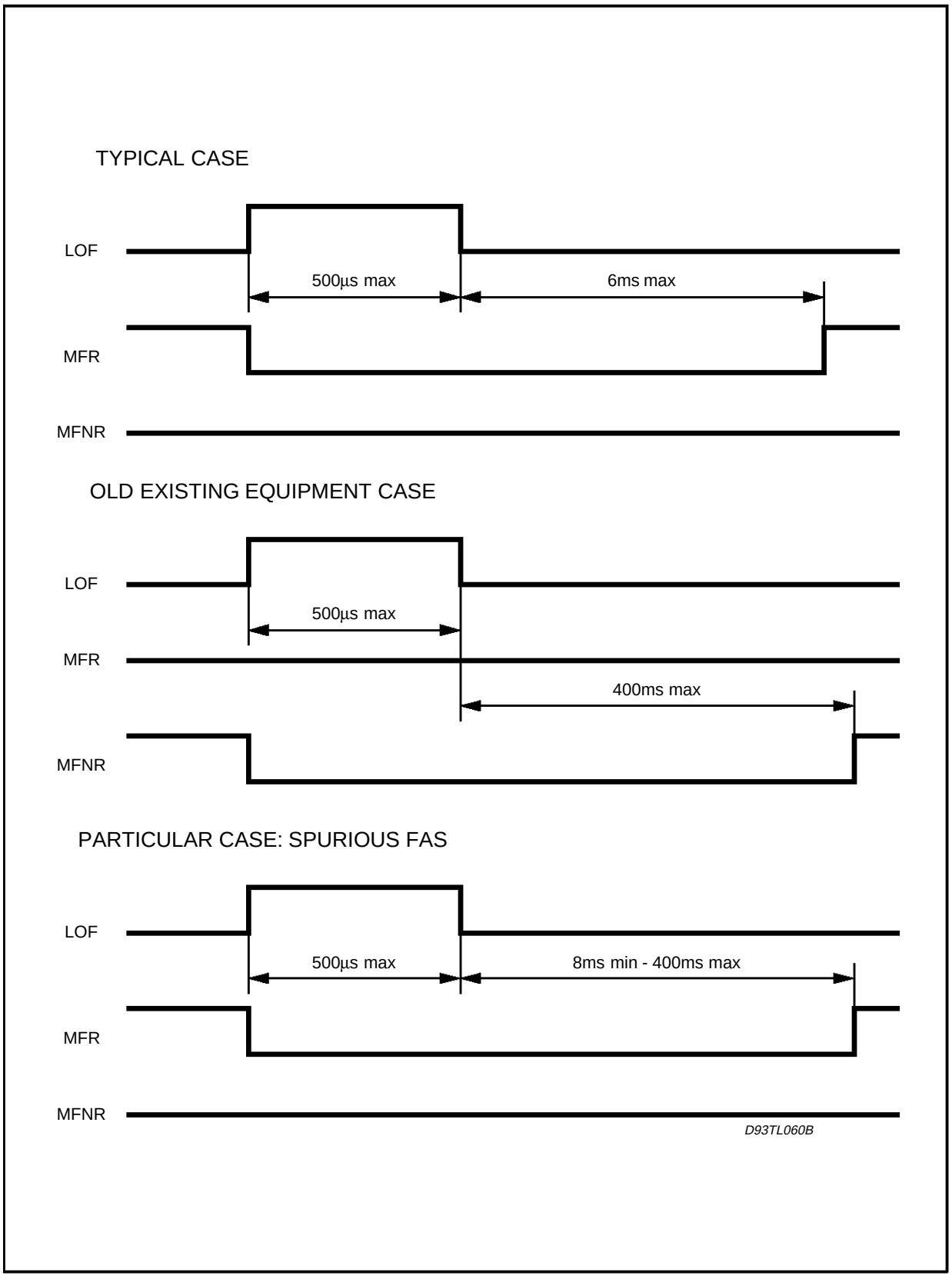


Figure 15: Pseudo Random Sequence Analyzer Algorithm.

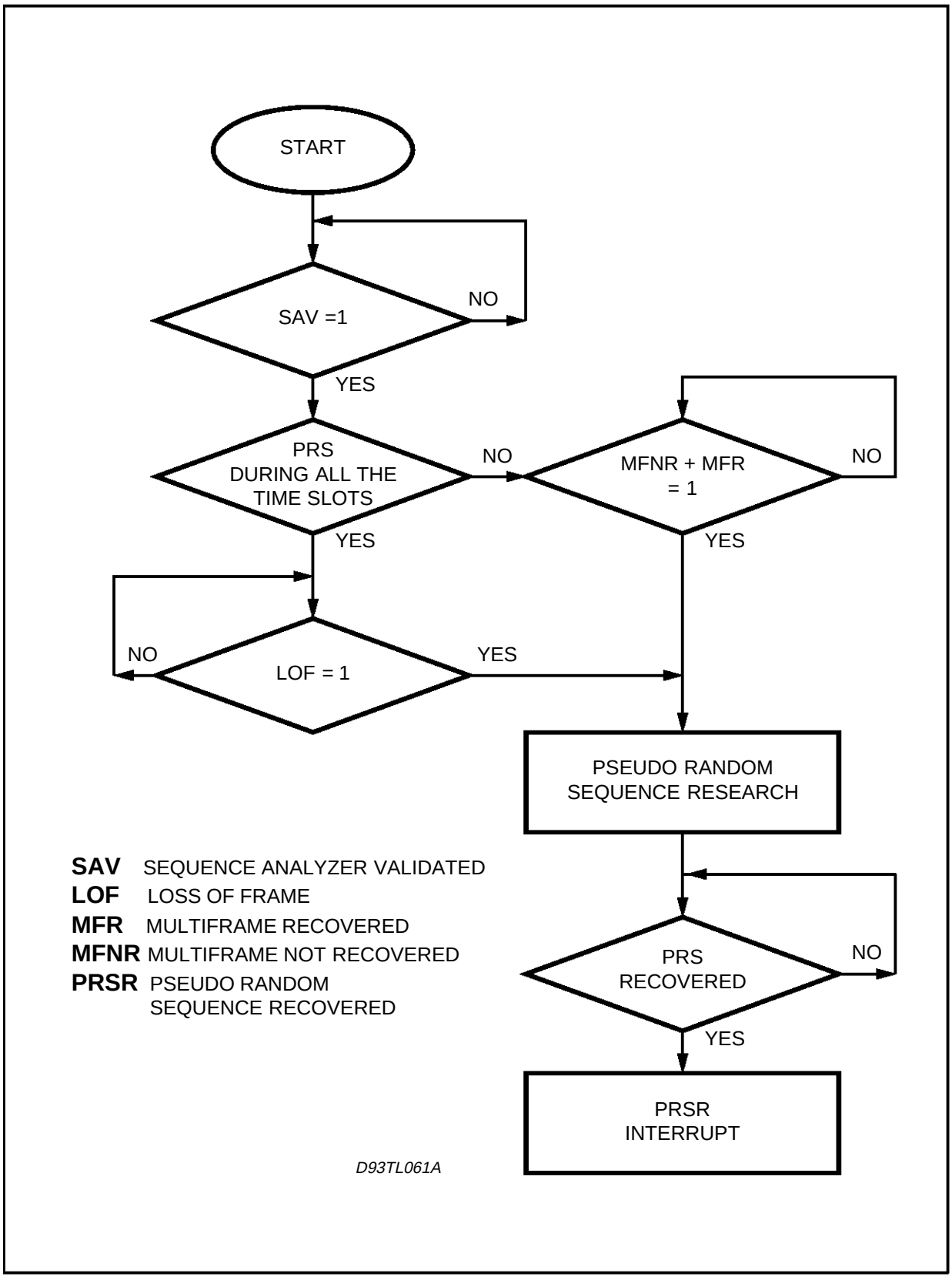


Figure 16: Transmitter Side Timing

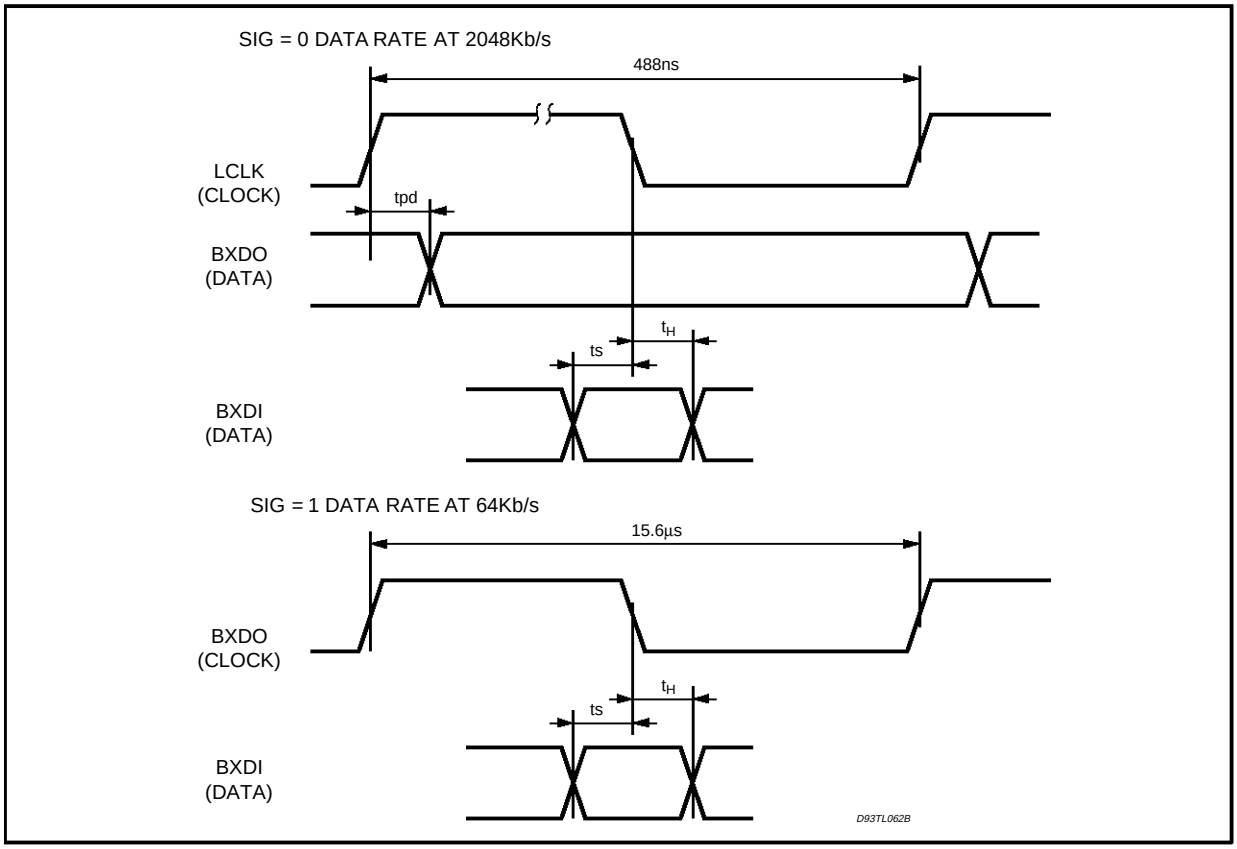


Figure 16a: Transmitter Side: Delay on BXD0 pin

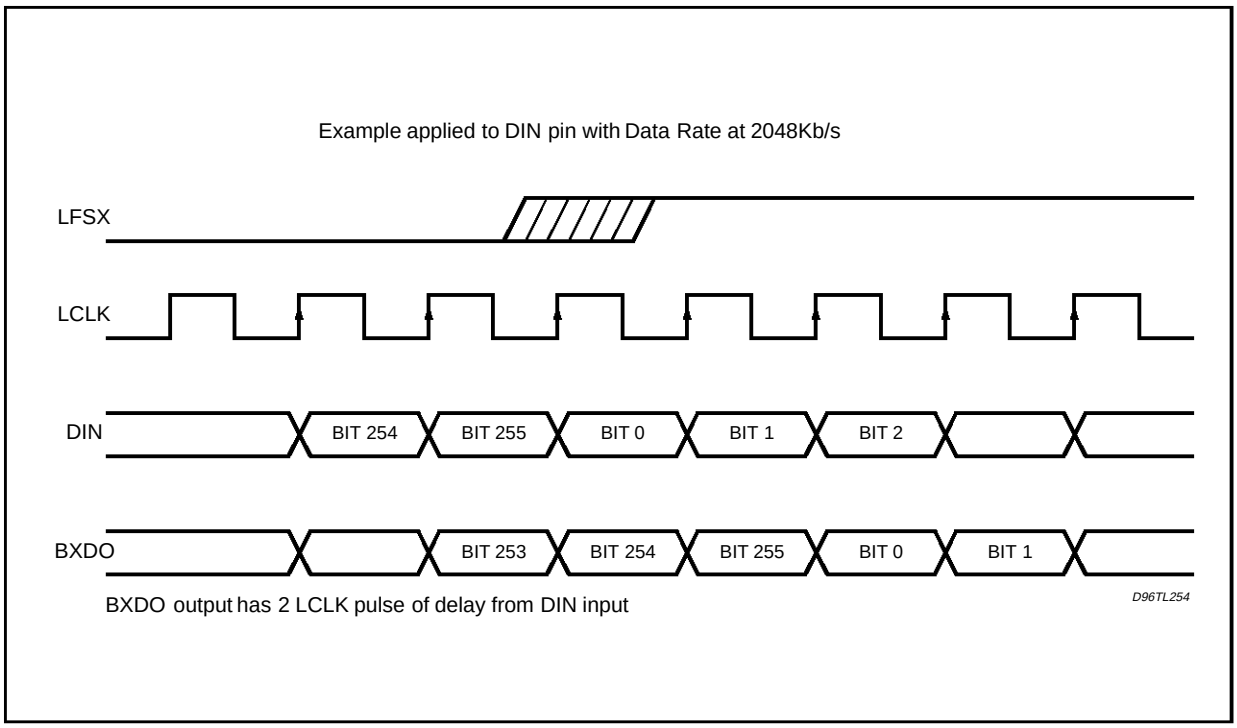


Figure 17: Receiver Side Timing

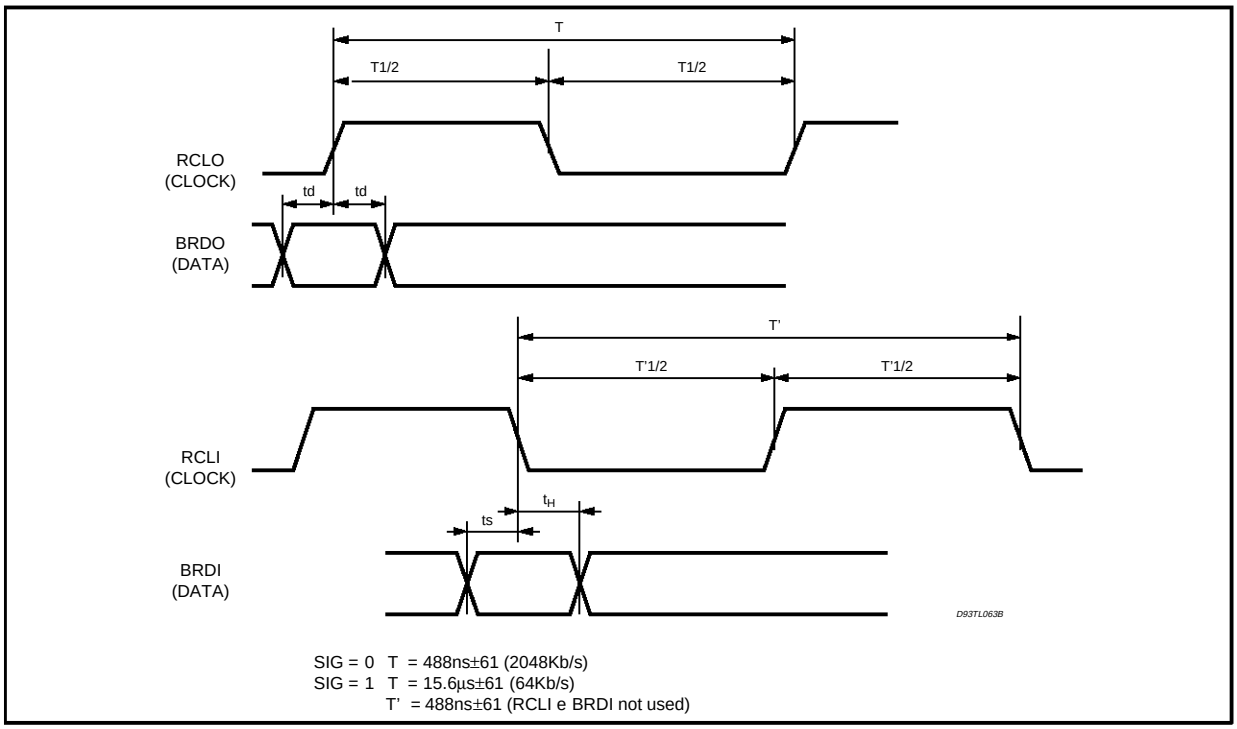


Figure 18: HCR and LCR versus configuration bits.

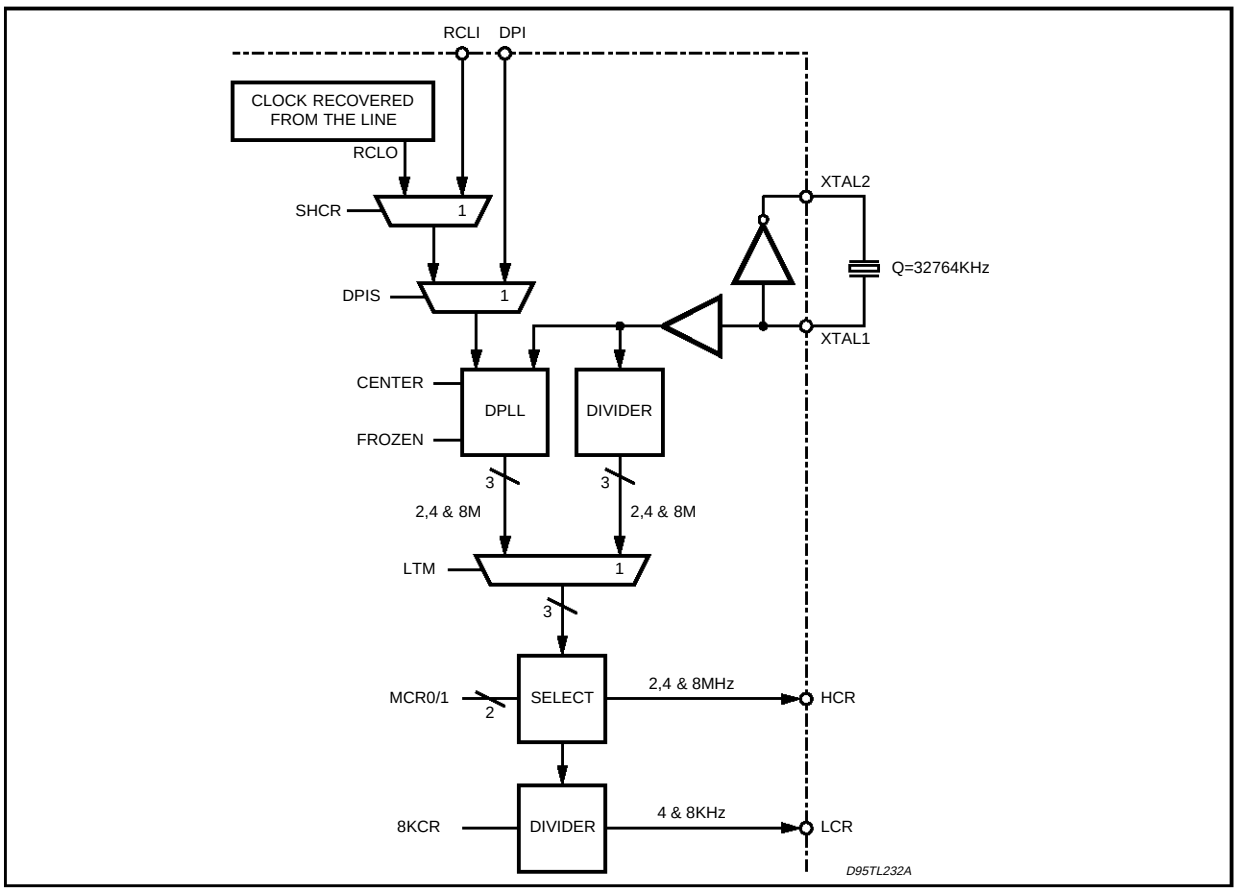
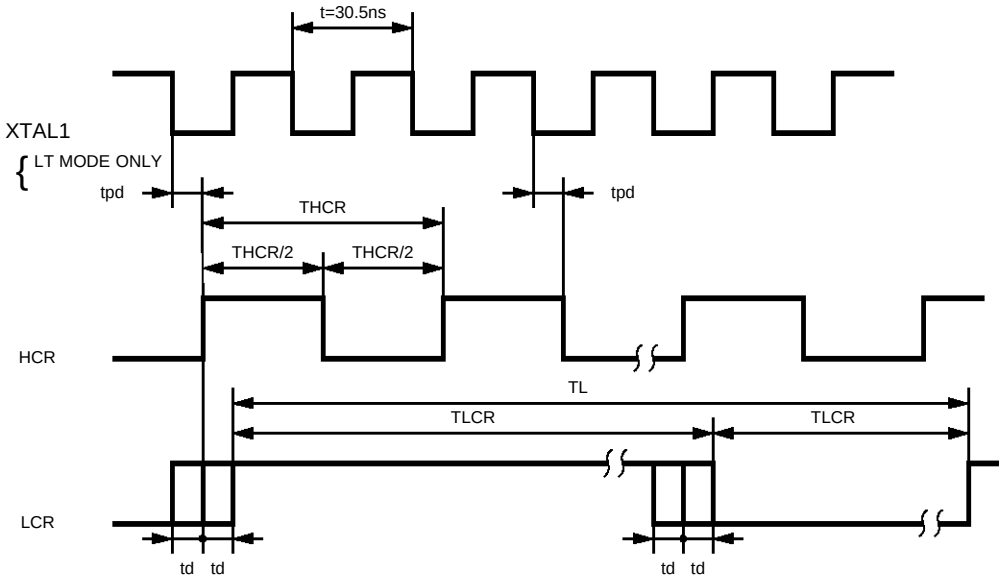


Figure 18a: High Clock and Low Clock in LT and TE Mode



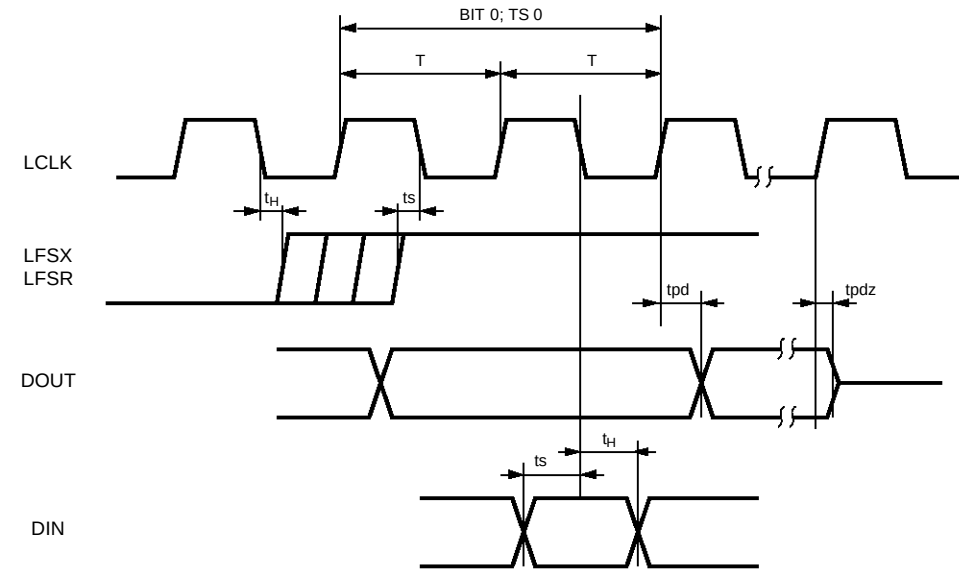
8MCR	THCR
1 (8MHz)	122ns
0 (4MHz)	244ns

8KCR	TLCR
1 (8MHz)	125µs
0 (4KHz)	250µs

LTM = 1 LT MODE HCR AND LCR ARE GENERATED BY CLOCK APPLIED TO XTAL1 PIN. JITTER FILTER IS NOT VALIDATED

LTM = 0 LE MODE HCR AND LCR CLOCK ARE RECOVERED FROM THE LINE VIA JITTER FILTER

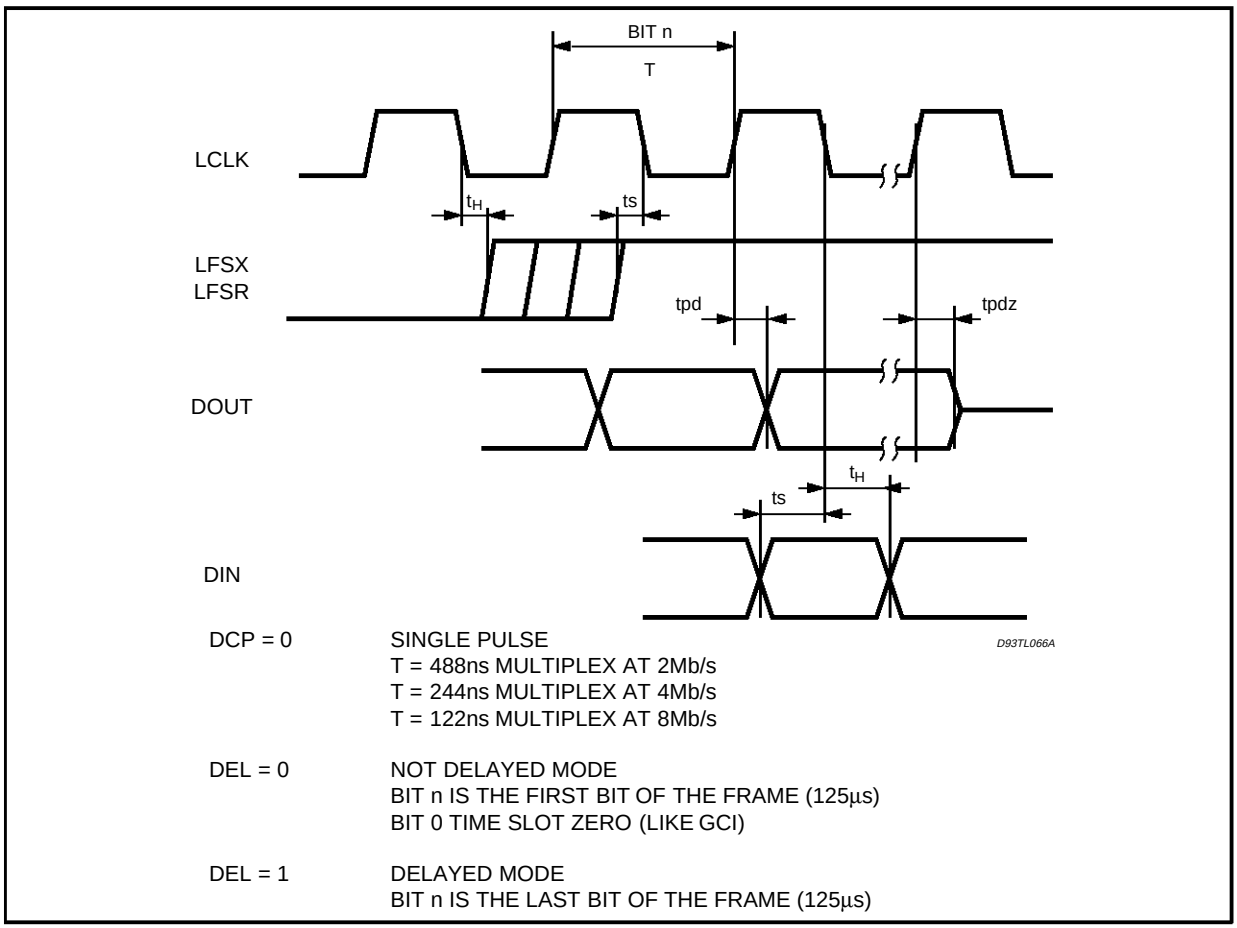
Figure 19: Double Clock Pulse Timing.



DCP = 1 DOUBLE CLOCK PULSE

T = 244ns MULTIPLEX AT 2Mb/s
T = 122ns MULTIPLEX AT 4Mb/s
T = 61ns MULTIPLEX AT 8Mb/s

Figure 20: Single Clock Delayed Mode.

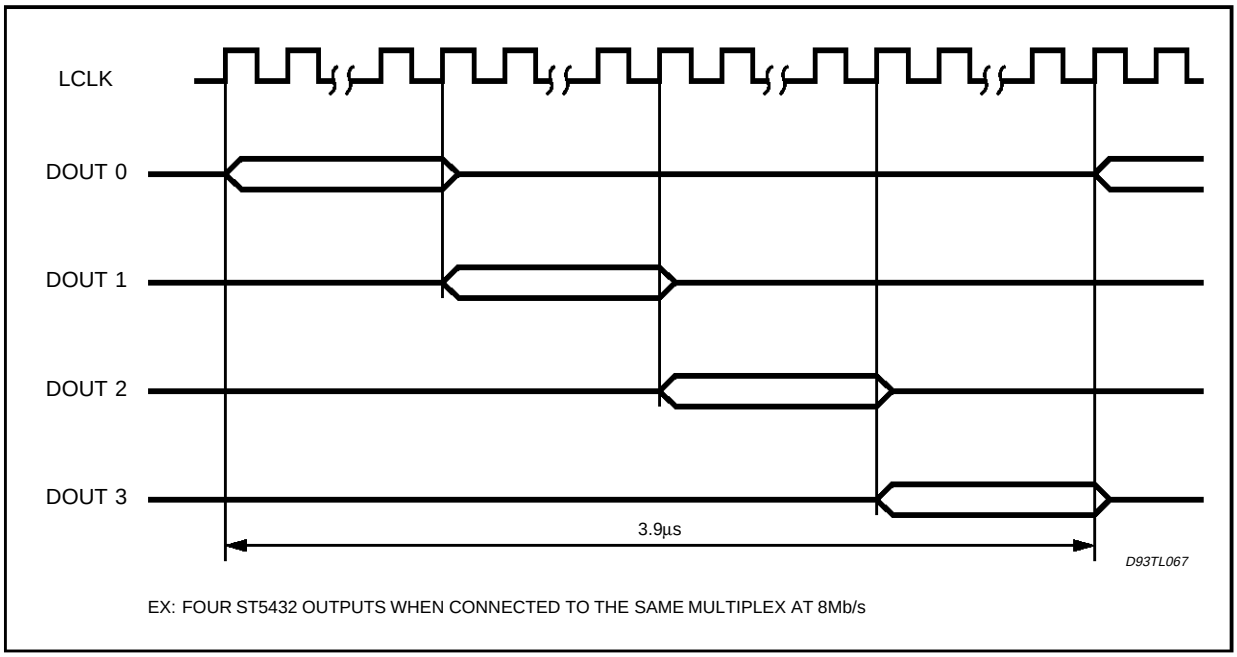


DCP = 0 SINGLE PULSE
T = 488ns MULTIPLEX AT 2Mb/s
T = 244ns MULTIPLEX AT 4Mb/s
T = 122ns MULTIPLEX AT 8Mb/s

DEL = 0 NOT DELAYED MODE
BIT n IS THE FIRST BIT OF THE FRAME (125µs)
BIT 0 TIME SLOT ZERO (LIKE GCI)

DEL = 1 DELAYED MODE
BIT n IS THE LAST BIT OF THE FRAME (125µs)

Figure 21: Multiplex Diagram



EX: FOUR ST5432 OUTPUTS WHEN CONNECTED TO THE SAME MULTIPLEX AT 8Mb/s

Figure 22: CCITT G703 HDB3 Pulse Template

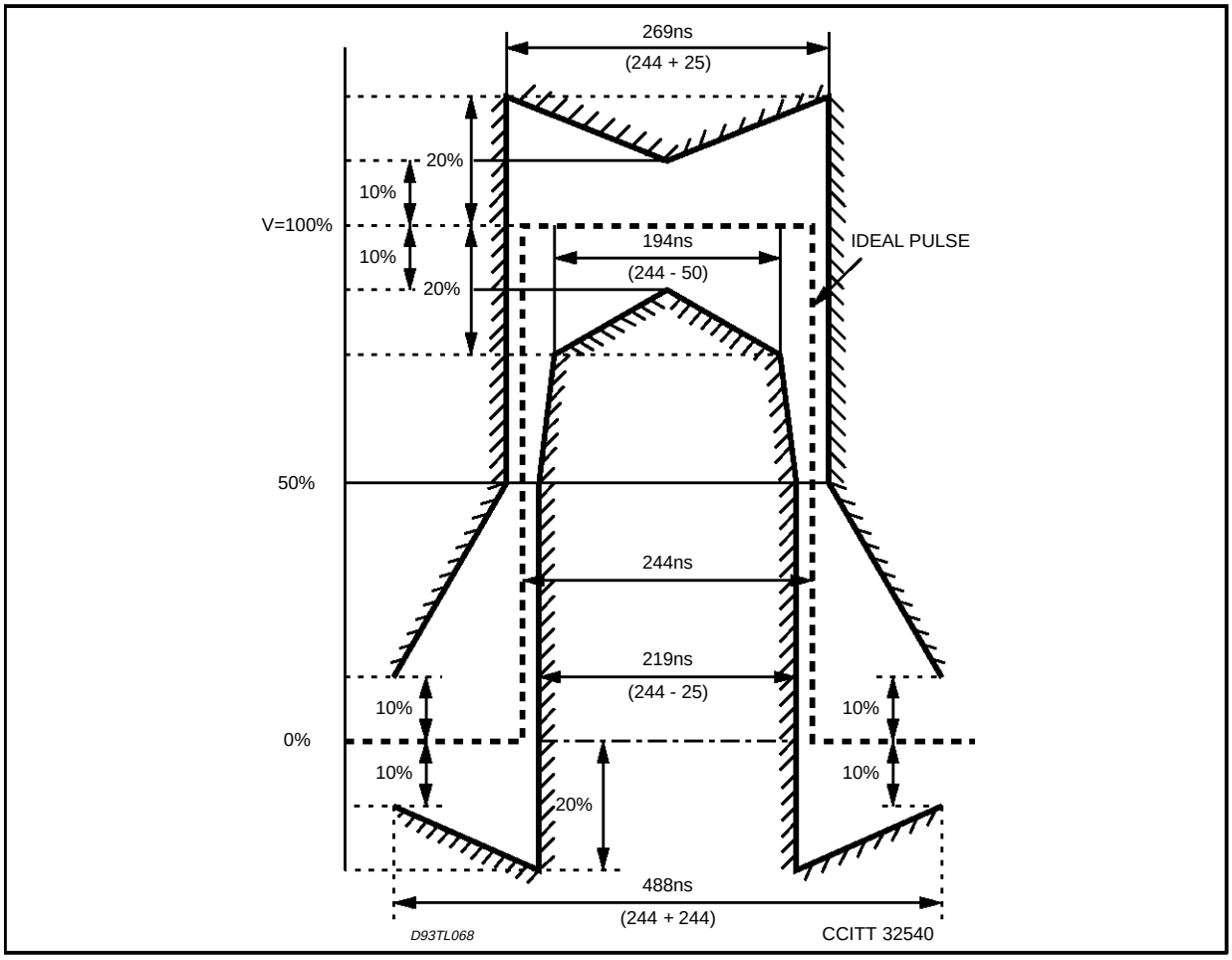
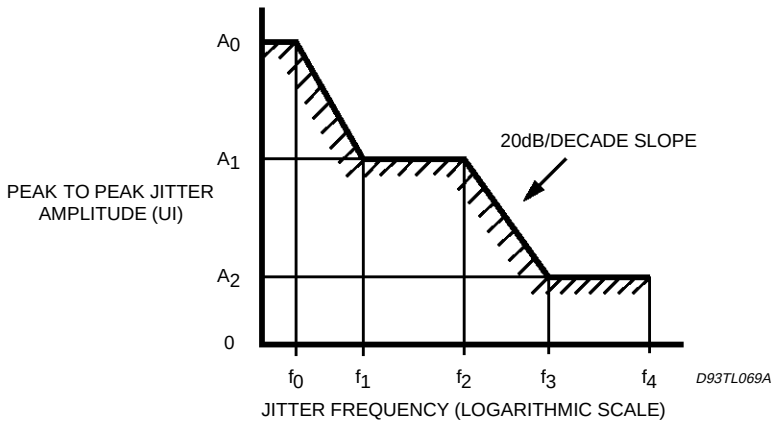
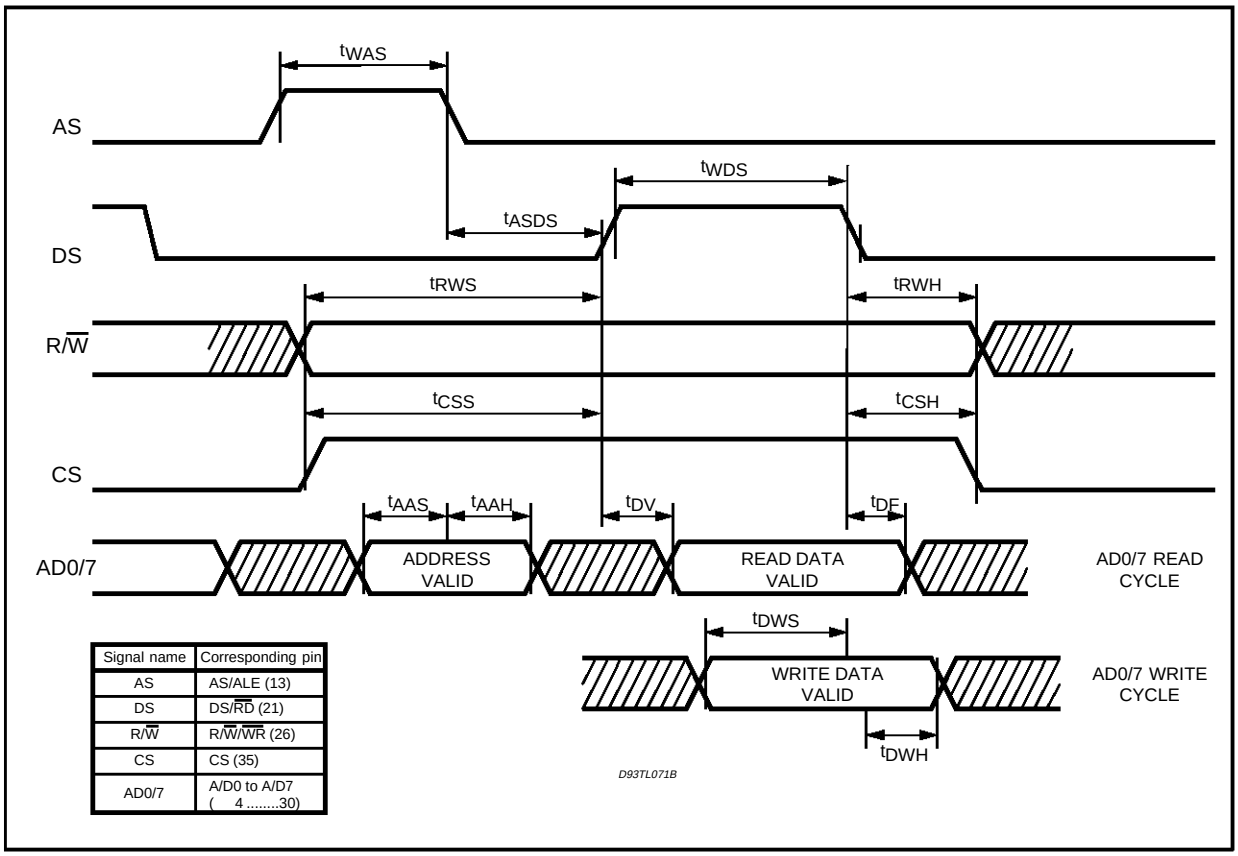


Figure 23: Allowed Jitter at the TE and LT Inputs (CCITT I431)



A_0	A_1	A_2	f_0	f_1	f_2	f_3	f_4
20.5 IU	1.0	0.2 IU	12 x 10^{-6} Hz	20Hz	3.6kHz	18kHz	100kHz

Multiplexed Motorola-like µP bus timing. (P0 = 0V; P1 = 5V)



Symbol	Parameter	Min.	Max.	Unit
t_{WAS}	AS Pulse Width	30		ns
t_{WDS}	DS Pulse Width	110		ns
t_{ASDS}	AS low to DS high	10		ns
t_{RWS}	R/$\overline{W}$ to DS setup	20		ns
t_{RWH}	R/$\overline{W}$ hold after DS	10		ns
t_{CSS}	CS to DS setup	20		ns
t_{CSH}	CS hold after DS	10		ns
t_{AAS}	Address to AS setup	20		ns
t_{AAH}	Address hold after AS	10		ns

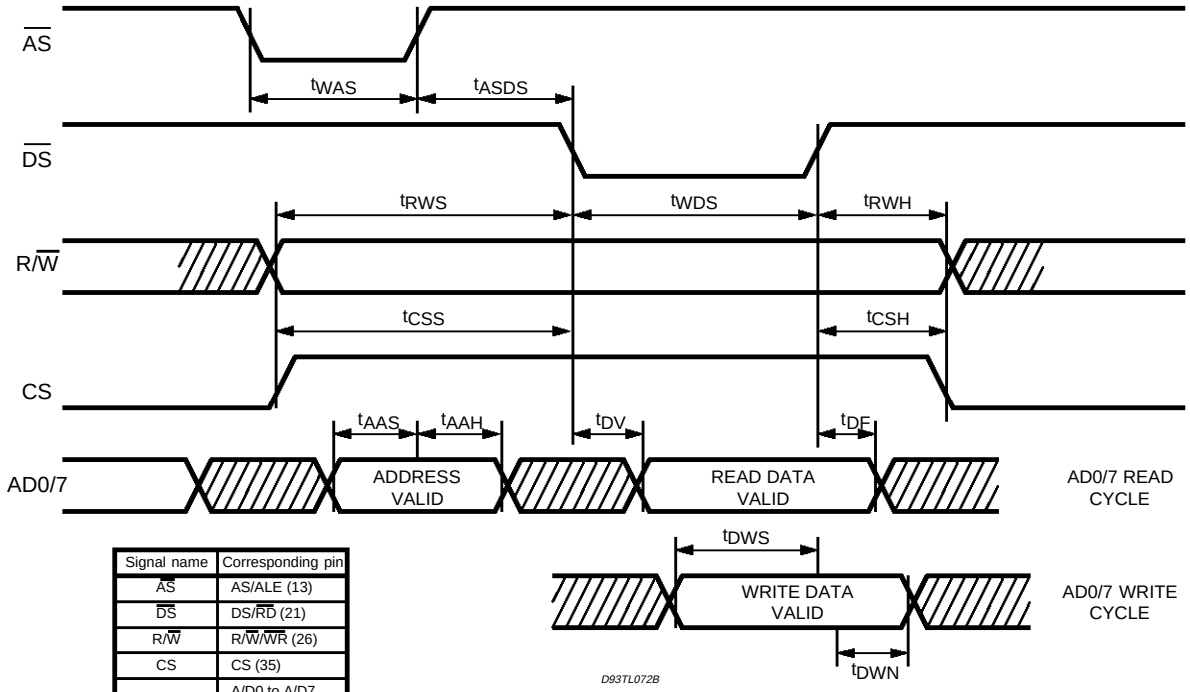
READ CYCLE

Symbol	Parameter	Min.	Max.	Unit
t_{DV}	Data Valid after DS		80	ns
t_{DF}	Output Flat Delay		25	ns

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit
t_{DWS}	Data to DS setup	35		ns
t_{DWH}	Data Hold after DS	10		ns

Multiplexed ST9-like μP bus timing. (P0 = 5V; P1 = 0V)



Signal name	Corresponding pin
AS	AS/ALE (13)
DS	DS/RD (21)
R/W	R/W/WR (26)
CS	CS (35)
AD0/7	A/D0 to A/D7 (4 .....30)

Symbol	Parameter	Min.	Max.	Unit
t_{WAS}	AS Pulse Width	30		ns
t_{WDS}	DS Pulse Width	110		ns
t_{ASDS}	AS high to DS low	10		ns
t_{RWS}	R/W to DS setup	20		ns
t_{RWH}	R/W hold after DS	10		ns
t_{CSS}	CS to DS setup	20		ns
t_{CSH}	CS hold after DS	10		ns
t_{AAS}	Address to AS setup	20		ns
t_{AAH}	Address hold after AS	10		ns

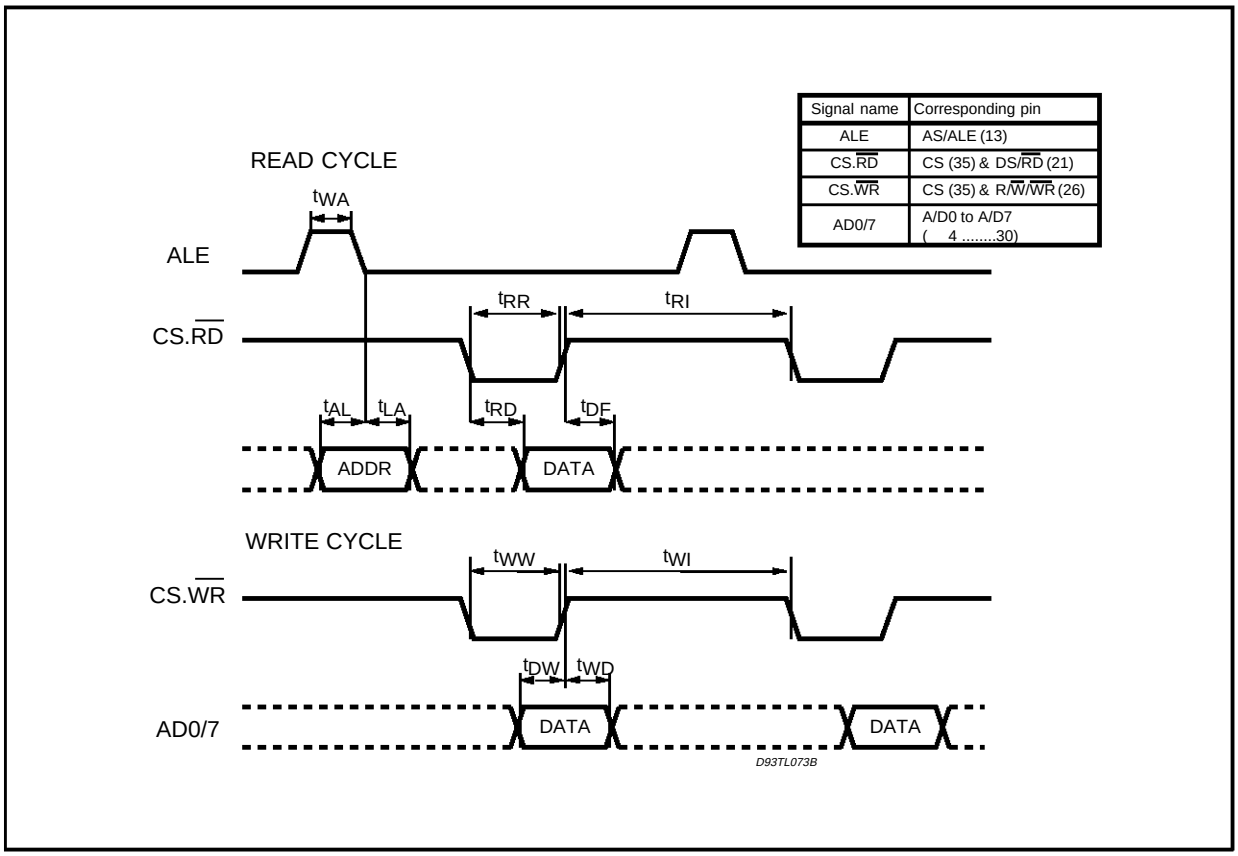
READ CYCLE

Symbol	Parameter	Min.	Max.	Unit
t_{DV}	Data Valid after DS		80	ns
t_{DF}	Output Flat Delay		25	ns

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit
t_{DWS}	Data to DS setup	35		ns
t_{DWH}	Data Hold after DS	10		ns

Multiplexed Intel-like µP bus timing. (P0 = 5V; P1 = 5V)



READ CYCLE (Multiplexed Intel Mode)

Symbol	Parameter	Min.	Max.	Unit
t_{LA}	Address Hold After ALE	10		ns
t_{AL}	Address to ALE Setup	20		ns
t_{RD}	Data Delay from $\overline{RD}$		80	ns
t_{RR}	$\overline{RD}$ Pulse Width	110		ns
t_{DF}	Output Float Delay		25	ns
t_{RI}	$\overline{RD}$ Control Interval	70		ns
t_{WA}	ALE Pulse Width	30		ns
t_{CSS}	CS to $\overline{RD}$ or $\overline{WR}$ set-up t_{CSS}	20		ns
t_{AAH}	CS hold after $\overline{RD}$ or $\overline{WR}$ t_{CSH}	10		ns

WRITE CYCLE (Multiplexed Intel Mode)

Symbol	Parameter	Min.	Max.	Unit
t_{WW}	$\overline{WR}$ Pulse Width	60		ns
t_{DW}	Data Setup to $\overline{WR}$	35		ns
t_{WD}	Data Hold after $\overline{WR}$	10		ns
t_{WI}	$\overline{WR}$ Control Interval	70		ns

TQFP44 (10 x 10) PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.014	0.018
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030