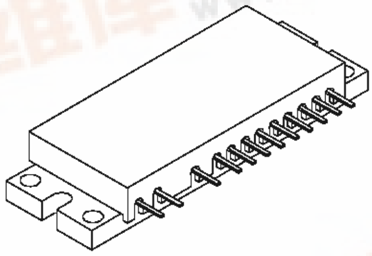
SGS-THOMSON MICROELECTRONICS

STM901-30

RF POWER MODULE
LINEAR BASE STATION APPLICATIONS

- LINEAR POWER AMPLIFIER
- 860 - 900 MHz
- 26 VOLTS
- INPUT/OUTPUT 50 OHMS
- P_{OUT} = +44.7 dBm PEP
- GAIN = 35 dB MIN.

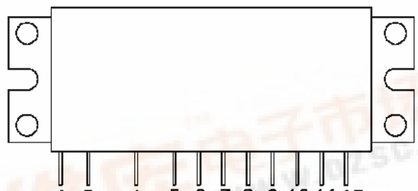


CASE STYLE H141

ORDER CODE STM901-30

BRANDING STM901-30

PIN CONNECTION



1. RF Input 2. V_{G1} 3. deleted 4. V_{G2}
5. V_D 6. V_{B1} 7. Cap_1 8. V_{C1}
9. V_{B2} 10. Cap_2 11. V_{C2} 12. RF Output

DESCRIPTION

The STM901-30 module is designed for digital cellular radio base station applications in the 860-900 MHz frequency range operating at 26V.

The STM901-30 is designed to meet the low distortion, high linearity requirements of modern digital cellular base station equipment.

ABSOLUTE MAXIMUM RATINGS (Tcase = 25°C)

Symbol	Parameter	Value	Unit
V, V_D, V_{C1}, V_{C2}	DC Supply Voltage	28	Vdc
I_{Q1}	Bias Current @ V = 26V, 1st Stage	0.40	Adc
I_{Q2}	Bias Current @ V = 26V, 2nd Stage	0.40	Adc
I_{Q3}	Bias Current @ V = 26V, 3rd Stage	0.54	Adc
I_{Q4}	Bias Current @ V = 26V, 4th Stage	1.62	Adc
P_{IN}	RF Input Power (P_{OUT} < 44.7 dBm PEP)	14	dBm PEP
P_{OUT}	RF Output Power (V = 26V)	48	dBm PEP
T_{STG}	Storage Temperature	– 30 to +100	°C
T_{OPER}	Operating Temperature	– 30 to +100	°C

ELECTRICAL SPECIFICATIONS (T_{case} = 25°C, V_D, V_{C1}, V_{C2} = 26V) (I_{DQ1} = 100mA, I_{DQ2} = 180mA, I_{CQ1} = 50mA, I_{CQ2} =150mA)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
BW	Frequency Range		860	—	900	MHz
G_P	Power Gain	P_{OUT} = +44.7 dBm PEP	35	38	—	dB
η_{dt}*	Double-Tone Efficiency	P_{OUT} = +44.7 dBm PEP	27	30	—	%
—	Input VSWR	P_{OUT} = +44.7 dBm PEP	—	1.5:1	3:1	—
IMD*	Intermodulation Distortion	P_{OUT} = +44.7 dBm PEP	—	–33	–26	dBT**
—	Load Mismatch	VSWR = 5:1 V = 26Vdc P_{OUT} = +44.7 dBm PEP	No Degradation in Output Power			

Note: * Two-Tone test; 20 KHz separation ** dBT - in dB, referenced to tone level (See Figure 1 below)

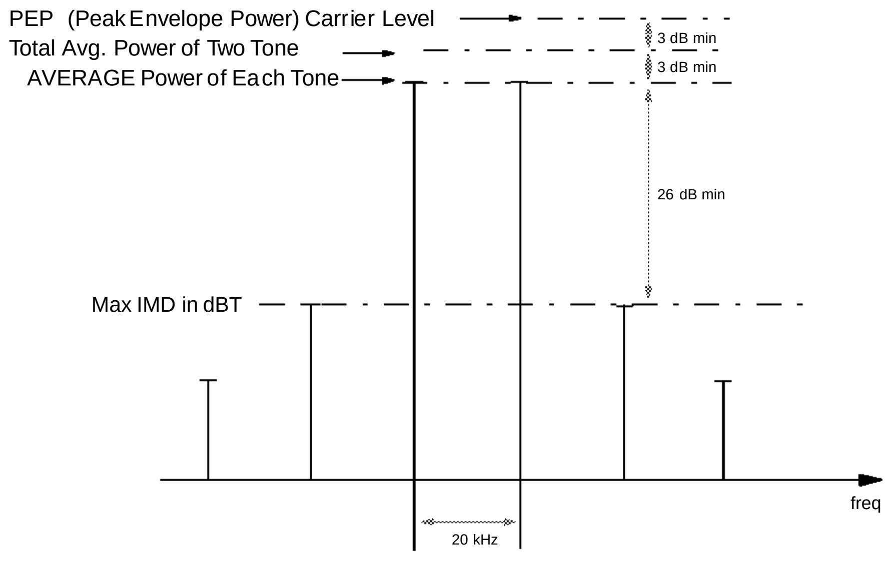
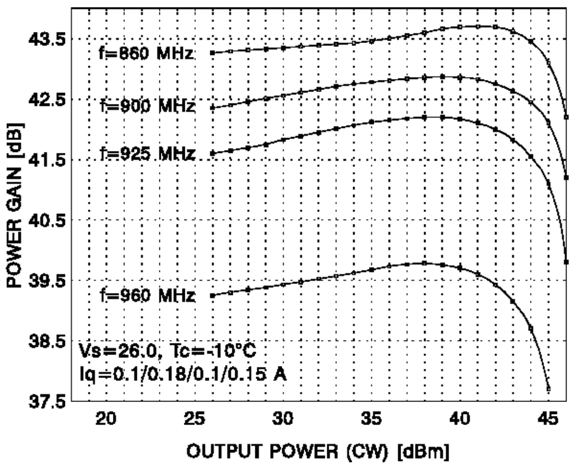


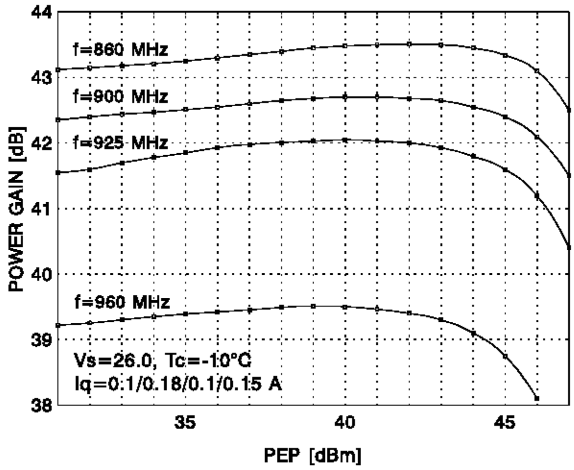
Figure 1

TYPICAL PERFORMANCE

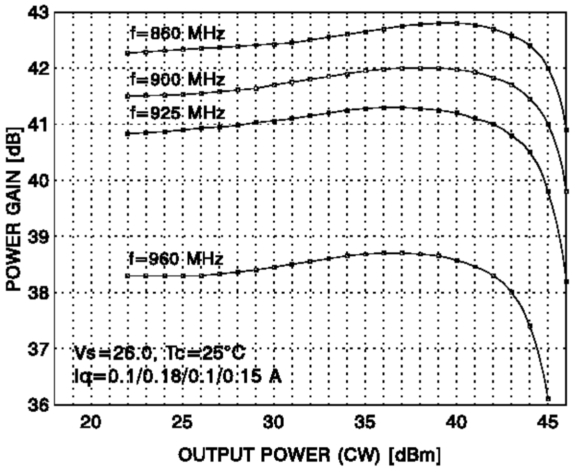
POWER GAIN vs OUTPUT POWER & FREQUENCY



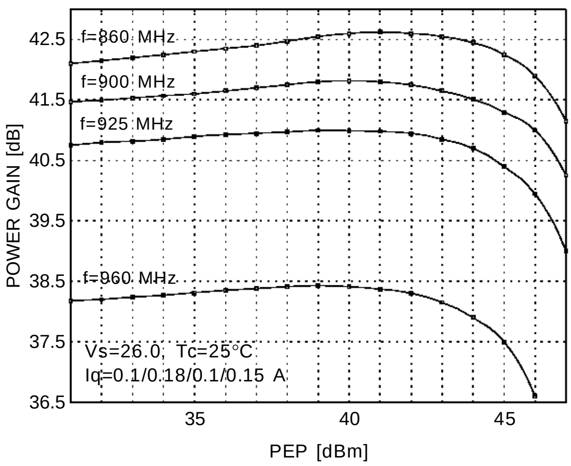
POWER GAIN vs PEP & FREQUENCY



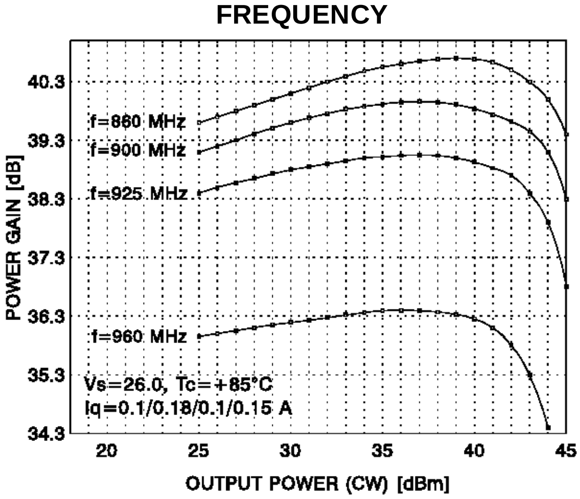
POWER GAIN vs OUTPUT POWER & FREQUENCY



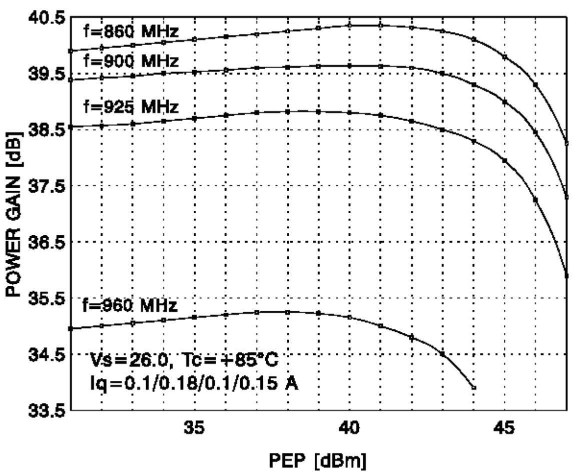
POWER GAIN vs PEP & FREQUENCY



POWER GAIN vs OUTPUT POWER & FREQUENCY

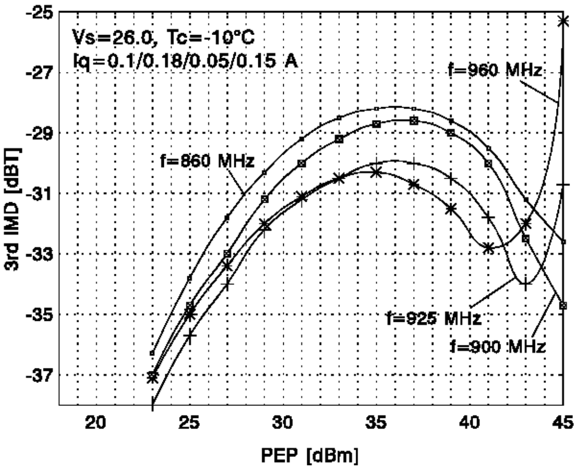


POWER GAIN vs PEP & FREQUENCY

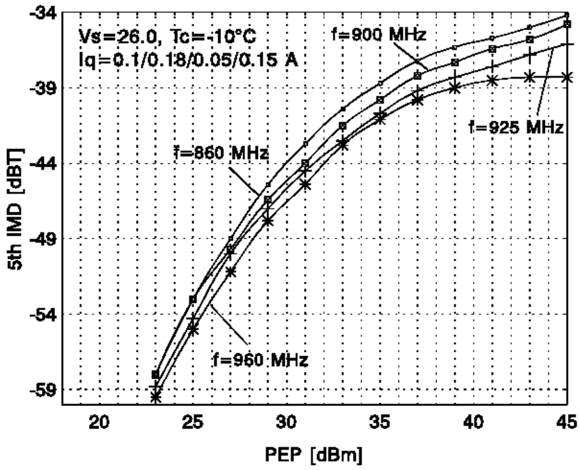


TYPICAL PERFORMANCE

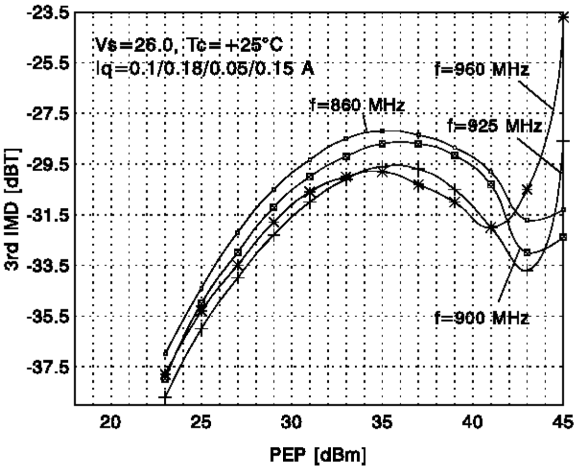
3rd ORDER IMD vs PEP



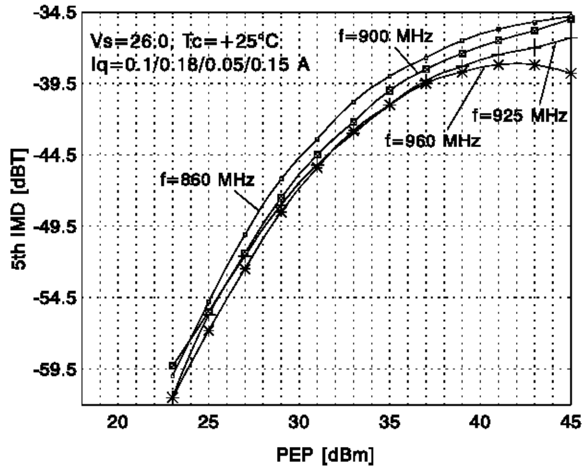
5th ORDER IMD vs PEP



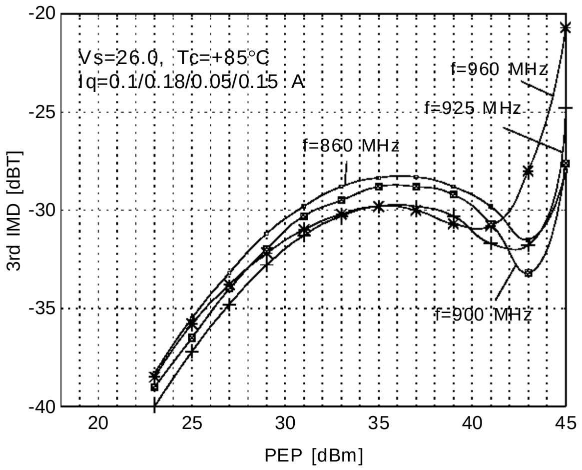
3rd ORDER IMD vs PEP



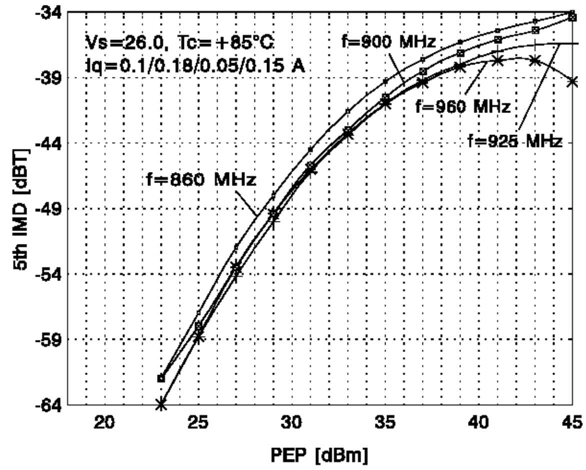
5th ORDER IMD vs PEP



3rd ORDER IMD vs PEP

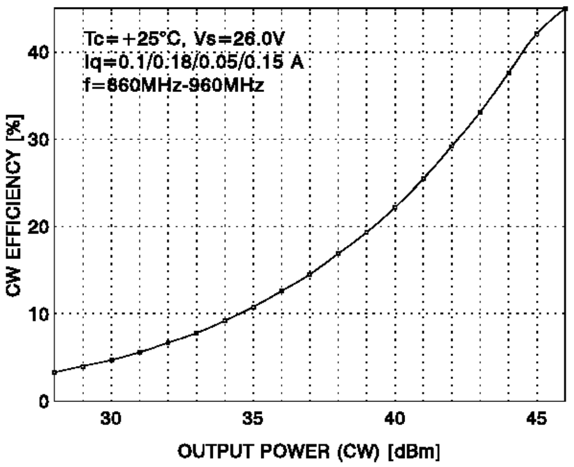


5th ORDER IMD vs PEP

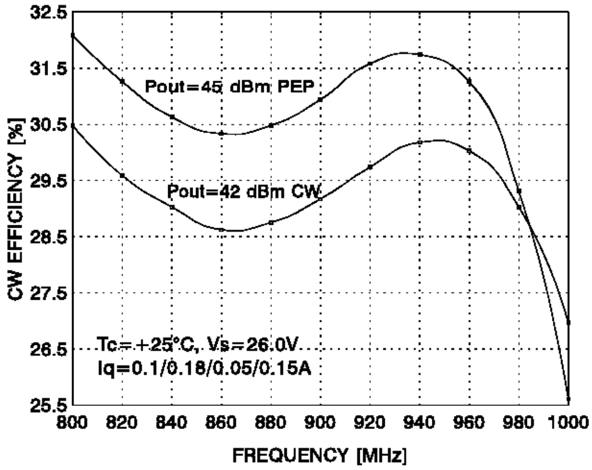


TYPICAL PERFORMANCE

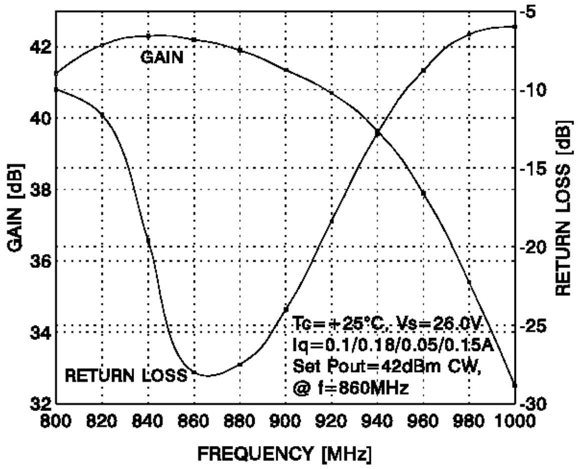
CW EFFICIENCY vs OUTPUT POWER & FREQUENCY



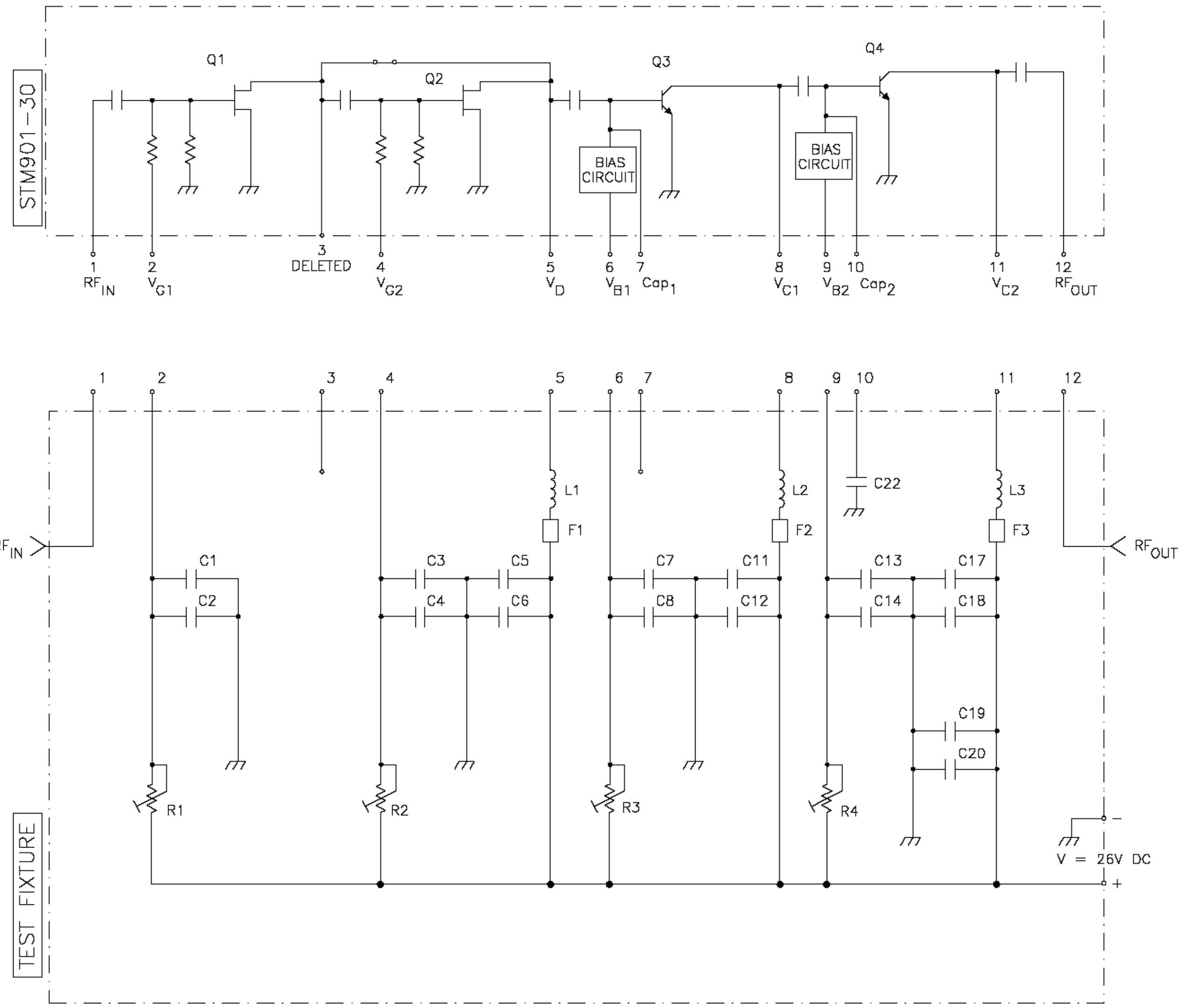
EFFICIENCY vs FREQUENCY



GAIN & RETURN LOSS vs FREQUENCY



MODULE DC AND TEST FIXTURE CONFIGURATION



C1, C3, C5, C7, C11, C13, C17 : 100 pF
C2, C4, C6, C8, C12, C14, C18 : .001 µF
C19 : .1 µF
C20, C22 : 100 µF
F1, F2, F3 : FAIR-RITE #2664000101
L1, L2, L3 : 5 Turns of 24 AWG Wire, Inner Diameter 1.27mm
R1, R2, R3, R4 : 20 KOHM

Setting Bias: (Ex.: I_{Q1} = .1A, I_{Q2} = .18A, I_{Q3} = .050A, I_{Q4} = .150A)

1. Set all variable resistors clockwise. (No bias current flows through transistors when all variable resistors are set clockwise.)
2. Record stationary current I_O.
3. Adjust R1 for (I_O + 100)mA.
4. Adjust R2 for (I_O + 100 + 180)mA.
5. Adjust R3 for (I_O + 100 + 180 + 50)mA.
6. Adjust R4 for (I_O + 100 + 180 + 50 + 150)mA.

APPLICATIONS RECOMMENDATIONS

OPERATION LIMITS

The STM901-30 power module should never be operated under any condition which exceeds the Absolute Maximum Ratings presented on this data sheet. Nor should the module be operated continuously at any of the specified maximum ratings. If the module is to be operated under any condition such that it may be subjected to one or more of the maximum rating conditions, care must be taken to monitor other parameters which may be affected.

DECOUPLING

Failure to properly decouple any of the voltage supply pins will result in oscillations at certain operating frequencies. Therefore, it is recommended that these pins be bypassed as indicated in the Module DC and Test Fixture Configuration drawing of this data sheet.

MODULE MOUNTING

To insure adequate thermal transfer from the module to the heatsink, it is recommended that a satisfactory thermal compound such as Dow Corning 340, Wakefield 120-2 or equivalent be applied between the module flange and the heatsink.

The heatsink mounting surface under the module should be flat to within +/- 0.05 mm (+/- 0.002 inch). The module should be mounted to the heatsink using 3 mm (or 4-40) or equivalent screws torqued to 5-6 kg-cm (4-6 in-lb).

The module leads are attached to the equipment PC board using 180°C solder applied to the leads with a properly grounded soldering iron tip, not to exceed 195°C, applied a minimum of 2 mm (0.080 inch) from the body of the module for a duration not to exceed 15 seconds per lead. It is imperative that no other portion of the module, other than the leads, be subjected to temperatures in excess of 100°C (maximum storage temperature), for any period of time, as the plastic moulded cover, internal components and sealing adhesives may be adversely affected by such conditions.

Due to the construction techniques and the materials used within the module, reflow soldering of the flange heatsink or the leads, is not recommended.

THERMAL CONSIDERATIONS

It will be necessary to provide a suitable heatsink in order to maintain the module flange temperature at or below the maximum case operating temperature. In a case where the module output power will be limited to +44.7 dBm (30W PEP) and designing for the worst case double-tone efficiency of 25%, the power dissipated by the module will be 48 watts. The heatsink must be designed such that the thermal rise will be less than the difference between the maximum ambient temperature at which the module will operate and the maximum operating case temperature of the module while dissipating 48 watts.

At T_{case} = +85°C, V = 26v, I_{Q1} = 0.1A, I_{Q2} = 0.18A, I_{Q3} = 0.05A, I_{Q4} = 0.2A, Z_L = 50 ohms and P_{OUT} = +44.7dBm PEP, maximum junction temperatures for the individual transistors should be below the following values:

Q1 = 115°C

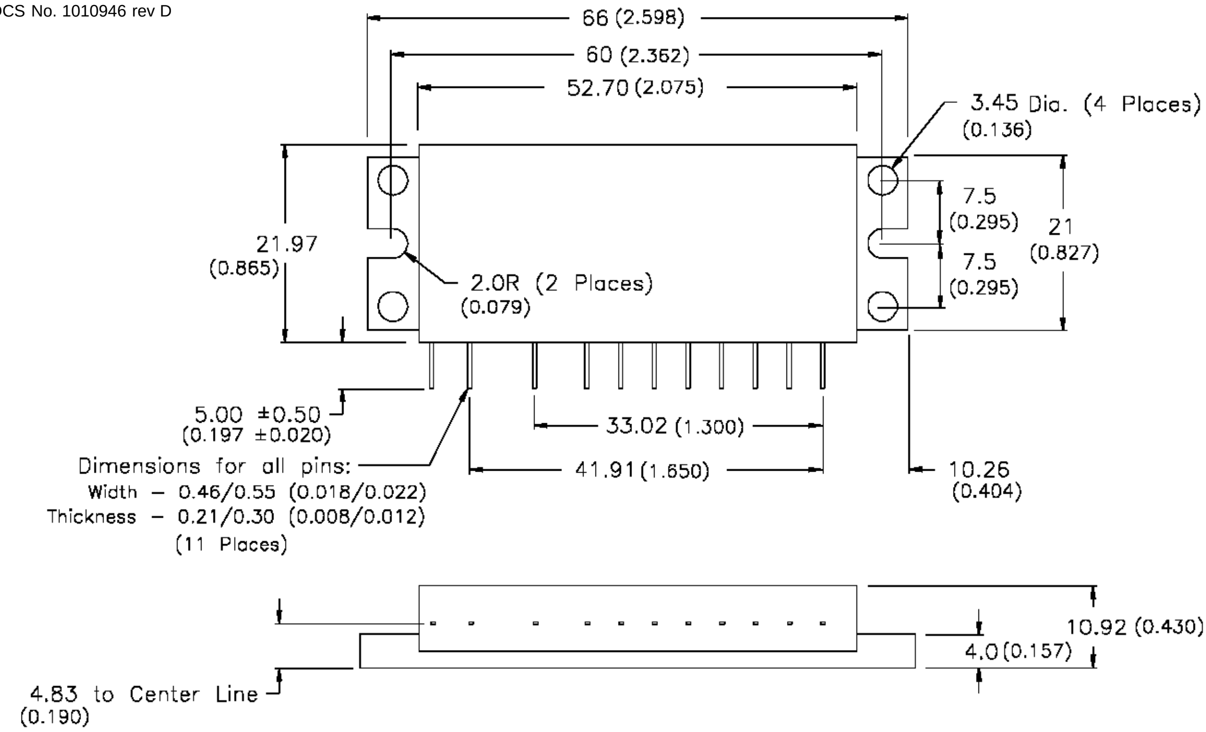
Q2 = 130°C

Q3 = 125°C

Q4 = 145°C

PACKAGE MECHANICAL DATA

UDCS No. 1010946 rev D



NOTES:
- Pin spacings 3.81mm (0.15in) unless otherwise specified
- All tolerances ±0.25mm (±0.010in) unless otherwise specified.
- Numbers in ( ) are inches.

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