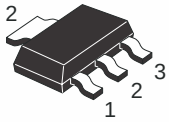
STN7NF10

N-CHANNEL 100V - 0.055 Ω - 5A SOT-223
LOW GATE CHARGE STripFET™ II POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STN7NF10	100 V	< 0.065 Ω	5 A

- TYPICAL $R_{DS}(on)$ = 0.055 Ω
- APPLICATION ORIENTED CHARACTERIZATION

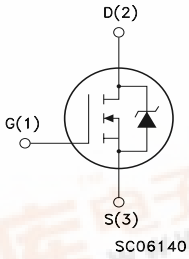


SOT-223

DESCRIPTION

This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	100	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	100	V
V_{GS}	Gate- source Voltage	±20	V
I_D	Drain Current (continuous) at T_C = 25°C	5	A
I_D	Drain Current (continuous) at T_C = 100°C	3.4	A
I_{DM} (●)	Drain Current (pulsed)	20	A
P_{TOT}	Total Dissipation at T_C = 25°C	3.3	W
	Derating Factor	0.026	W/°C
T_{stg}	Storage Temperature	–55 to 150	°C
T_j	Operating Junction Temperature		

(●) Pulse width limited by safe operating area

THERMAL DATA

Rthj-PCB	Thermal Resistance Junction-PCB Max(*)	38	°C/W
Rthj-PCB	Thermal Resistance Junction-PCB Max(**)	100	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose (1.6 mm from case,for 10s)	260	°C

Note: (*) When mounted on 1 in^2 FR-4 BOARD,2 oz Cu, t<10s.
Note: (**) When mounted on minimum footprint.

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	100			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 1.5 A		0.055	0.065	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 15 V , I_D = 1.5 A		12		S
C_{iss}	Input Capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		870		pF
C_{oss}	Output Capacitance			125		pF
C_{rss}	Reverse Transfer Capacitance			52		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 50 V, I_D = 12 A		58		ns
t_r	Rise Time	R_G = 4.7Ω V_{GS} = 10 V (see test circuit, Figure 3)		45		ns
Q_g	Total Gate Charge	V_{DD} = 80 V, I_D = 24 A,		30	41	nC
Q_{gs}	Gate-Source Charge	V_{GS} = 10 V		6		nC
Q_{gd}	Gate-Drain Charge			10		nC

SWITCHING OFF

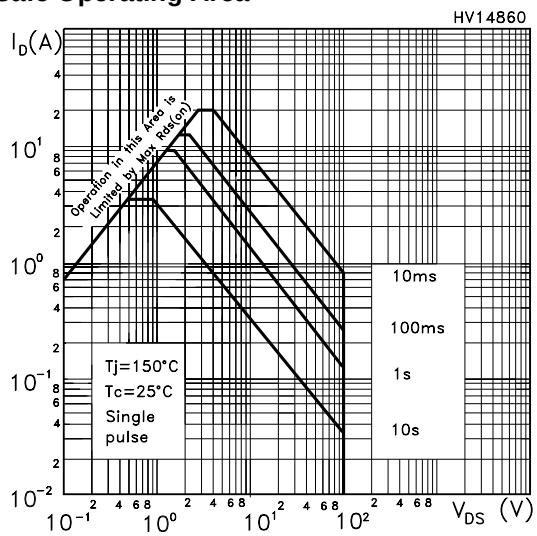
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	V_{DD} = 50 V, I_D = 12 A,		49		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 3)		17		ns

SOURCE DRAIN DIODE

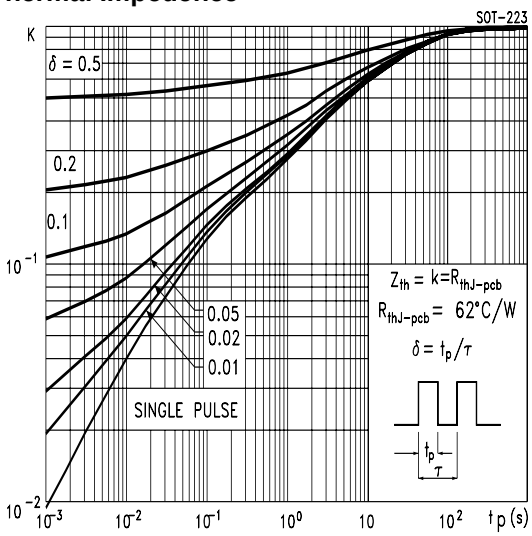
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				5	A
I_{SDM} (1)	Source-drain Current (pulsed)				20	A
V_{SD} (2)	Forward On Voltage	I_{SD} = 5 A, V_{GS} = 0			1.3	V
t_{rr}	Reverse Recovery Time	I_{SD} = 5 A, di/dt = 100A/µs,		100		ns
Q_{rr}	Reverse Recovery Charge	V_{DD} = 30 V, T_j = 150°C		375		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		7.5		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

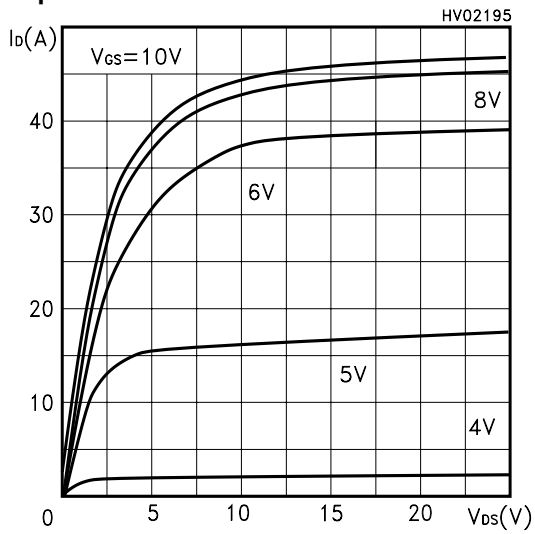
Safe Operating Area



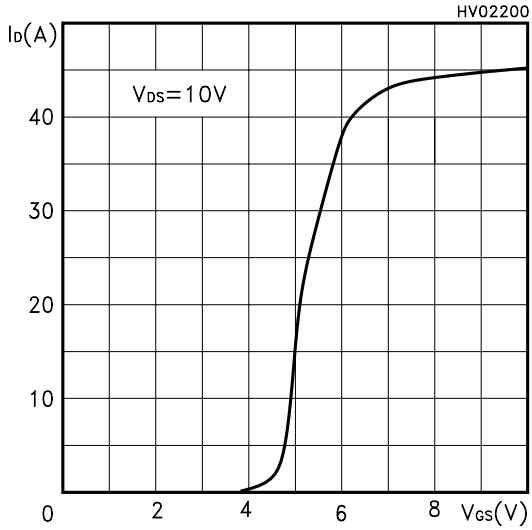
Thermal Impedence



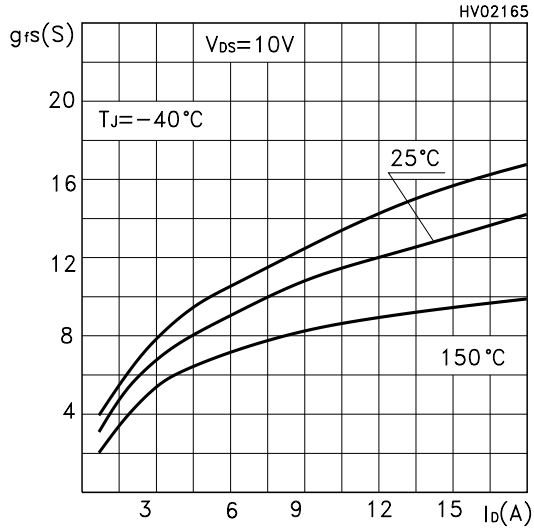
Output Characteristics



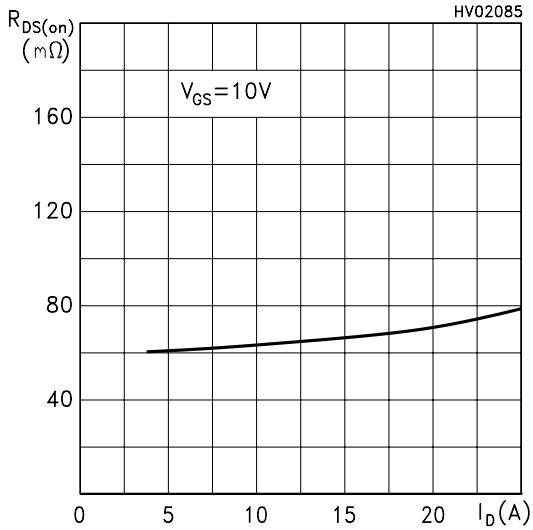
Transfer Characteristics



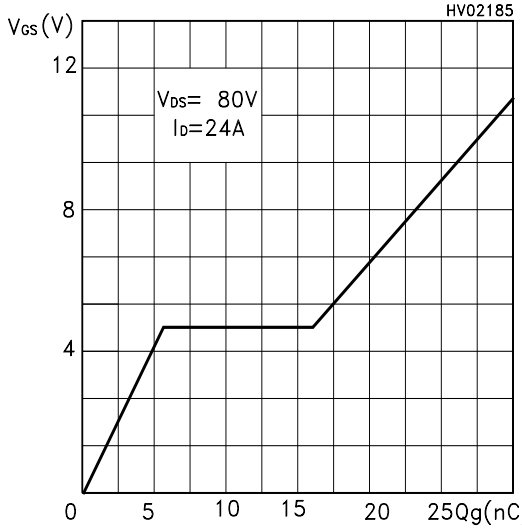
Transconductance



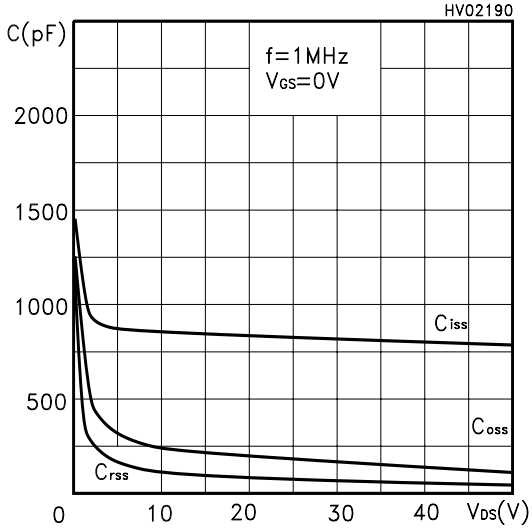
Static Drain-source On Resistance



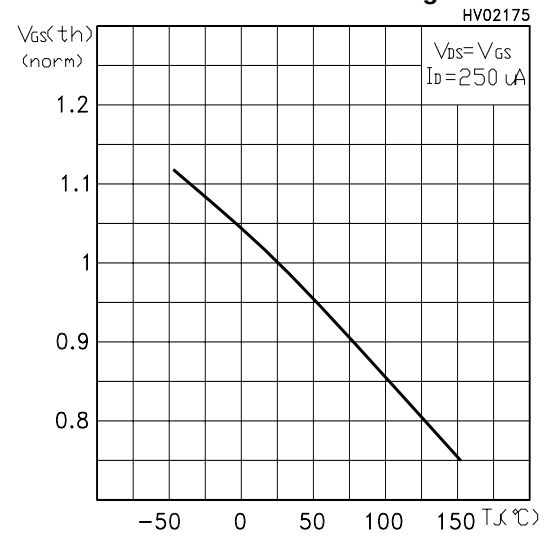
Gate Charge vs Gate-source Voltage



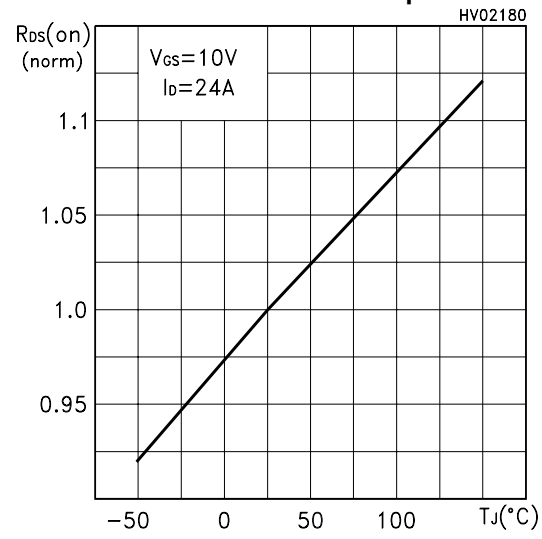
Capacitance Variations



Normalized Gate Thereshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

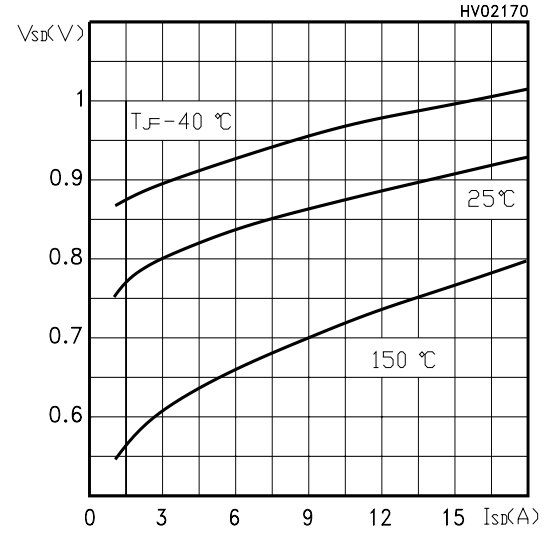


Fig. 1: Unclamped Inductive Load Test Circuit

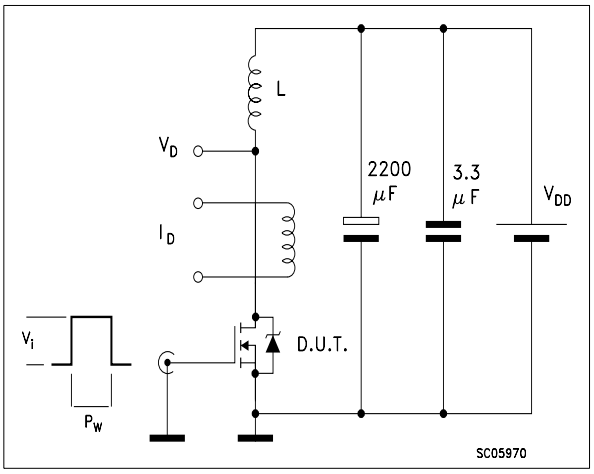


Fig. 2: Unclamped Inductive Waveform

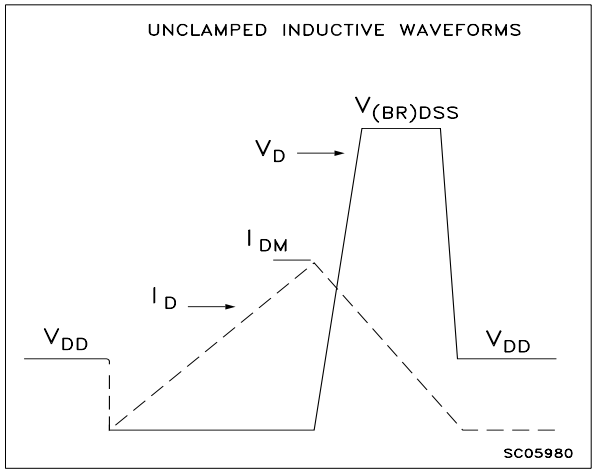


Fig. 3: Switching Times Test Circuit For Resistive Load

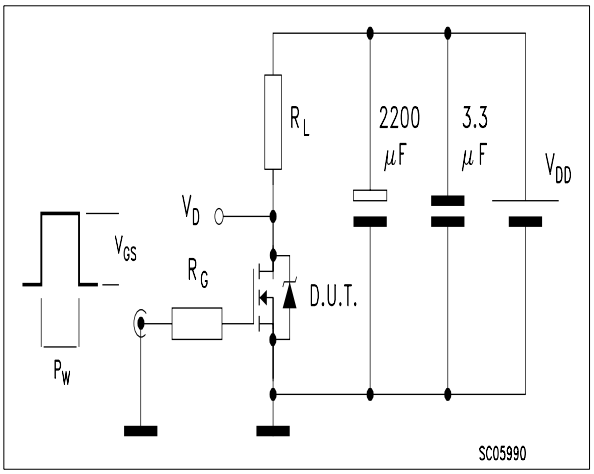


Fig. 4: Gate Charge test Circuit

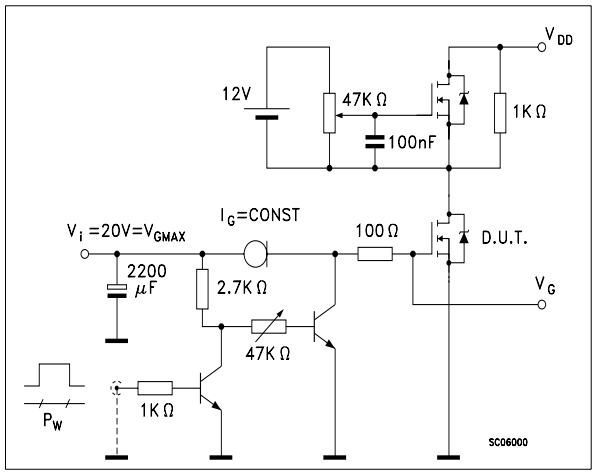
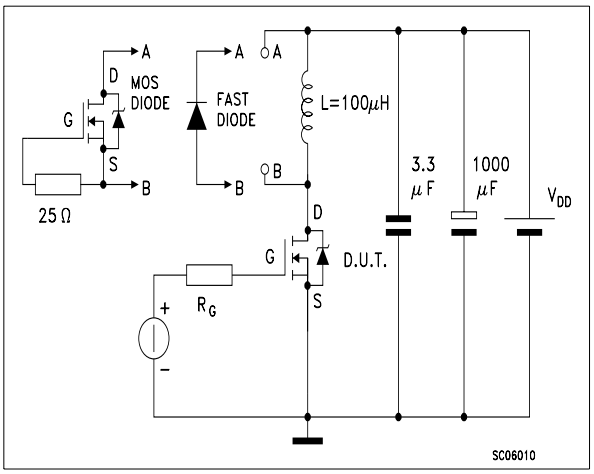
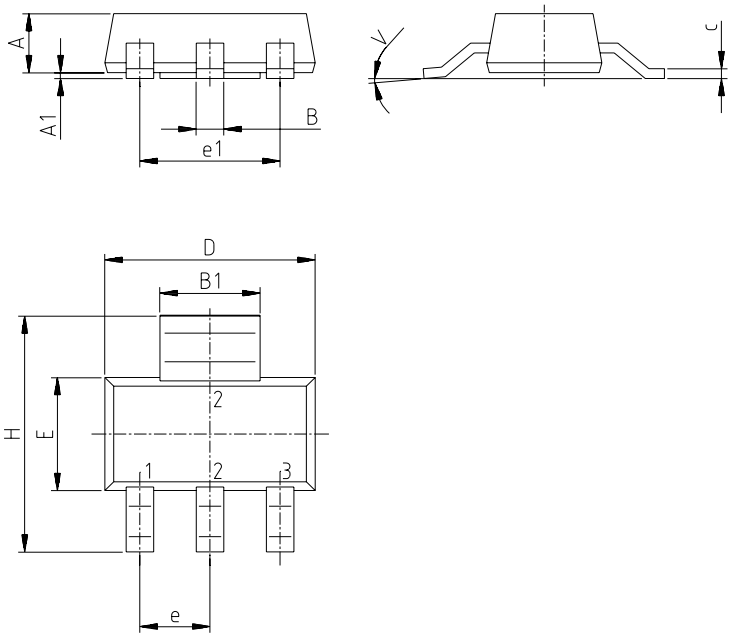


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



SOT-223 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.80			0.071
B	0.60	0.70	0.80	0.024	0.027	0.031
B1	2.90	3.00	3.10	0.114	0.118	0.122
c	0.24	0.26	0.32	0.009	0.010	0.013
D	6.30	6.50	6.70	0.248	0.256	0.264
e		2.30			0.090	
e1		4.60			0.181	
E	3.30	3.50	3.70	0.130	0.138	0.146
H	6.70	7.00	7.30	0.264	0.276	0.287
V			10^o			10^o
A1		0.02				



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