

STQ2NF06L

N-CHANNEL 60V - 0.1 Ω - 2A TO-92 STripFET™ II POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	ID
STQ2NF06L	60 V	<0.12 Ω	2 A

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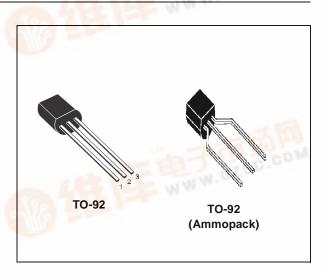
- TYPICAL R_{DS}(on) = 0.1Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- AVALANCHE RUGGED TECHNOLOGY
- LOW THRESHOLD DRIVE

DESCRIPTION

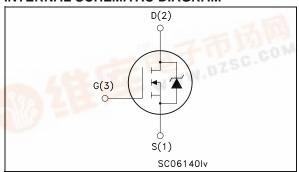
This Power MOSFET is the latest development of STMicroelectronis unique "Single Feature Size^{TMI}" strip-based process. The resulting transistor shows extremely high packing density for low onresistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC MOTOR CONTROL (DISK DRIVES, etc.)
- DC-DC & DC-AC CONVERTERS
- SYNCHRONOUS RECTIFICATION



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (VGS = 0)	60	V
VDGR	Drain-gate Voltage (R _{GS} = 20 kΩ)	60	V
Vgs	Gate- source Voltage	± 16	V
ID	Drain Current (continuous) at T _C = 25°C	2	А
ΙD	Drain Current (continuous) at T _C = 100°C	1.2	Α
IDM(●)	Drain Current (pulsed)	8	Α
P _{tot} (1)	Total Dissipation at T _C = 25°C	3	W
Y 1.	Derating Factor	8	W/°C
dv/dt (2)	Peak Diode Recovery voltage slope	6	V/ns
EAS (3)	Single Pulse Avalanche Energy	200	mJ
T _{stg}	Storage Temperature	55 to 150	°C
Tj	Max. Operating Junction Temperature	-55 to 150	°C

Pulse width limited by safe operating area.

1) Related to Rthj -I

(2) $I_{SD} \le 2A$, $di/dt \le 100A/\mu s$, $V_{DD} \le V_{(BR)DSS}$, $T_j \le T_{JMAX}$ (3) Starting $T_j = 25$ °C, $I_D = 2A$, $V_{DD} = 30V$

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THERMAL DATA

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _(BR) DSS	Drain-source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0$	60			V
IDSS	Zero Gate Voltage Drain Current (VGS = 0)	$V_{DS} = Max Rating$ $V_{DS} = Max Rating T_{C} = 125$ °C			1 10	μA μA
IGSS	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 16 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$	$I_D = 250 \mu A$	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _G S = 10 V V _G S = 5 V	I _D = 1 A I _D = 1 A		0.1 0.12	0.12 0.14	Ω Ω

DYNAMIC

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Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
gfs (*)	Forward Transconductance	V _{DS} = 15 V I _D = 1 A		3		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V f = 1 MHz V _{GS} = 0		360 55 25		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r	Turn-on Time Rise Time	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		10 20		ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 48 V I _D = 2 A V _{GS} = 5 V		5.6 1.2 2.6	7.6	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(off)}	Turn-off Delay Time Fall Time	$\begin{aligned} &V_{DD} = 30 \; V & I_{D} = 1 \; A \\ &R_{G} = 4.7\Omega, & V_{GS} = 4.5 \; V \\ &(Resistive Load, Figure 3) \end{aligned}$		17 6		ns ns

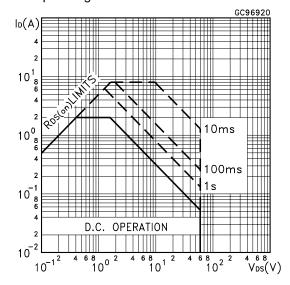
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain Current Source-drain Current (pulsed)				2 8	A A
V _{SD} (*)	Forward On Voltage	I _{SD} = 2 A V _{GS} = 0			1.3	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 2 \text{ A}$ $di/dt = 100 \text{A}/\mu \text{s}$ $V_{DD} = 20 \text{ V}$ $T_j = 150 ^{\circ}\text{C}$ (see test circuit, Figure 5)		28 31 2.2		ns nC A

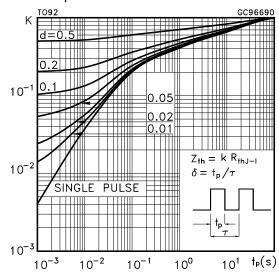
^(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

(•)Pulse width limited by safe operating area.

Safe Operating Area

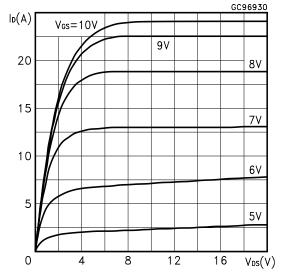


Thermal Impedance Junction-lead

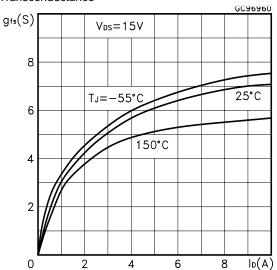


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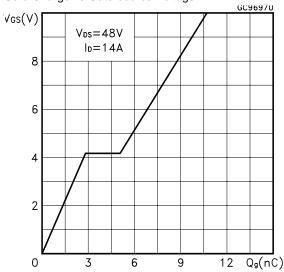
Output Characteristics



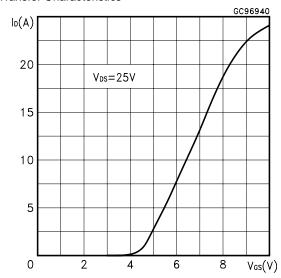
Transconductance



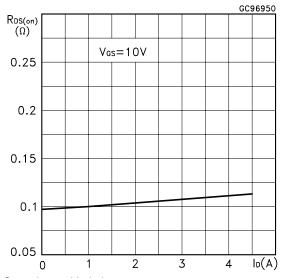
Gate Charge vs Gate-source Voltage



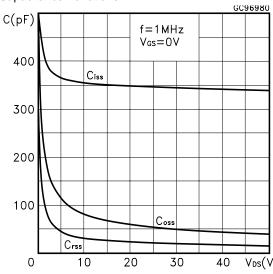
Transfer Characteristics



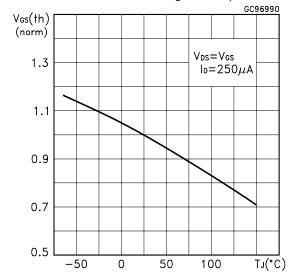
Static Drain-source On Resistance



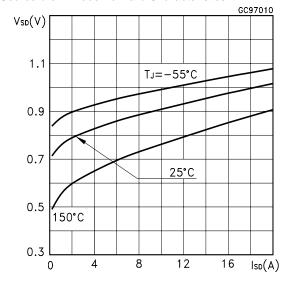
Capacitance Variations



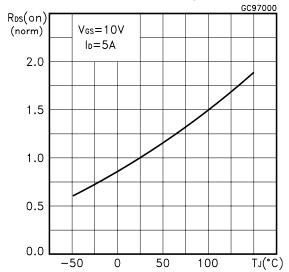
Normalized Gate Threshold Voltage vs Temperature



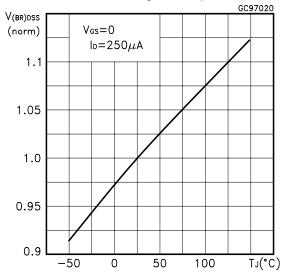
Source-drain Diode Forward Characteristics



Normalized on Resistance vs Temperature



Normalized Breakdown Voltage vs Temperature.



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Fig. 1: Unclamped Inductive Load Test Circuit

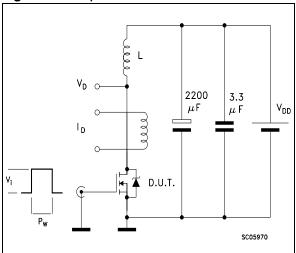


Fig. 3: Switching Times Test Circuits For Resistive Load

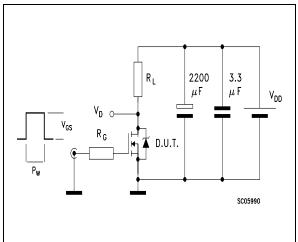


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

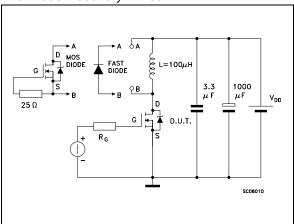


Fig. 2: Unclamped Inductive Waveform

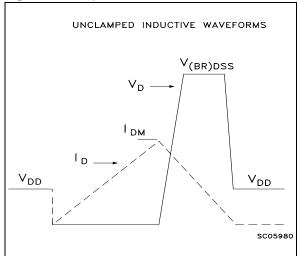
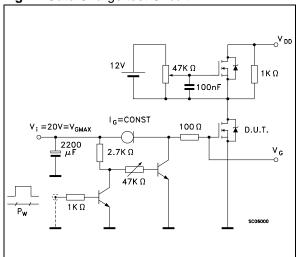


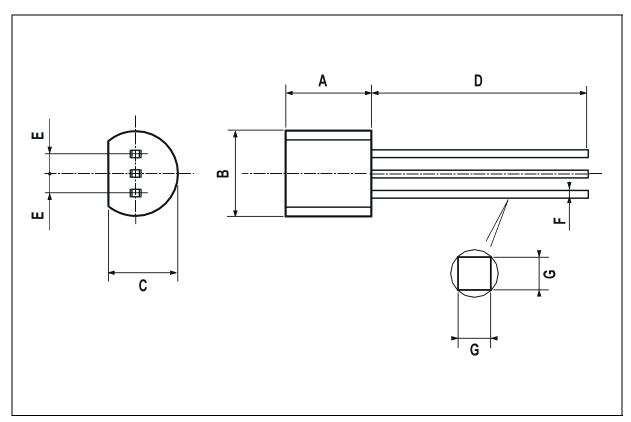
Fig. 4: Gate Charge test Circuit



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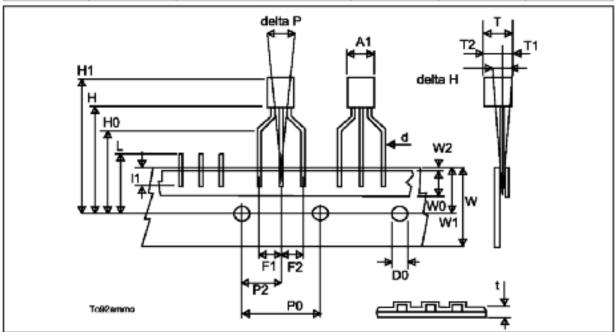
TO-92 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А	4.58		5.33	0.180		0.210
В	4.45		5.2	0.175		0.204
С	3.2		4.2	0.126		0.165
D	12.7			0.500		
E		1.27			0.050	
F	0.4		0.51	0.016		0.020
G	0.35			0.14		



TO-92 AMMOPACK

DIM.		mm.			inch			
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.		
A1			4.8			0.19		
Т			3.8			0.15		
T1			1,6			0.06		
T2			2.3			0.09		
d			0.48			0.02		
P0	12.5	12.7	12.9	0.49	0.5	0.51		
P2	5.65	6.35	7.05	0.22	0.25	0.27		
F1, F2	2.44	2.54	2.94	0.09	0.1	0.11		
delta H	-2		2	-0.08		0.08		
W	17.5	18	19	0.69	0.71	0.74		
W0	5.7	6	6.3	0.22	0.23	0.24		
W1	8.5	9	9.25	0.33	0.35	0.36		
W2			0.5			0.02		
Н	18.5		20.5	0.72		0.80		
H0	15.5	16	16.5	0.61	0.63	0.65		
H1			25			0.98		
D0	3.8	4	4.2	0.15	0.157	0.16		
t			0.9			0.035		
L			11			0.43		
l1	3			0.11				
delta P	-1		1	-0.04		0.04		



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