



# STS01DTP06

## DUAL NPN-PNP COMPLEMENTARY BIPOLAR TRANSISTOR

PRELIMINARY DATA

**Table 1: General Features**

$V_{CE(sat)}$	$h_{FE}$	$I_c$
0.35 V	> 100	1A

- n HIGH GAIN
- n LOW  $V_{CE(sat)}$
- n SIMPLIFIED CIRCUIT DESIGN
- n REDUCED COMPONENT COUNT

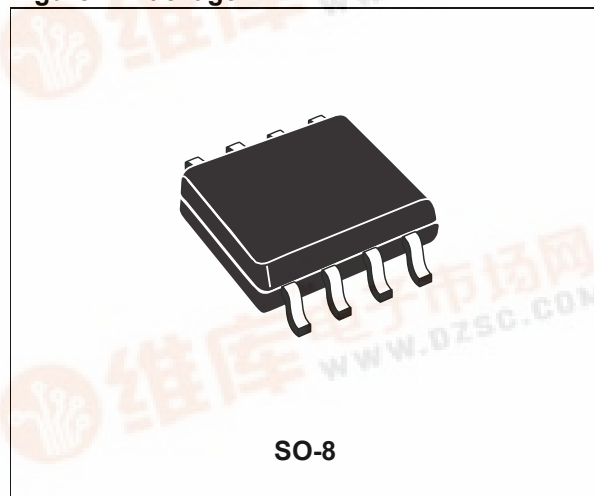
**APPLICATION**

- n PUSH-PULL OR TOTEM-POLE CONFIGURATION
- n MOSFET AND IGBT GATE DRIVING
- n MOTOR, RELAY AND SOLENOID DRIVING

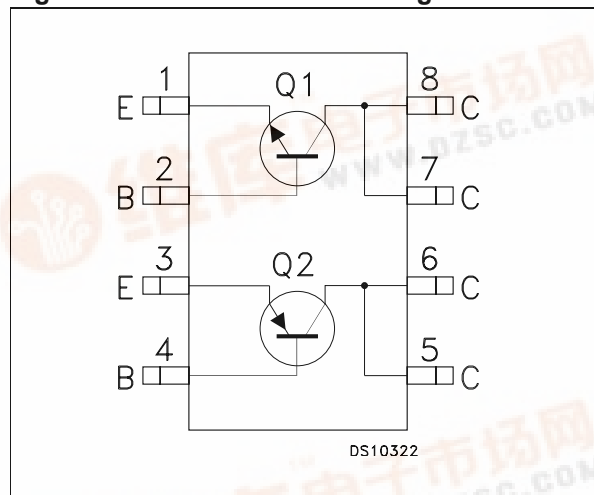
**DESCRIPTION**

The STS01DTP06 is a Hybrid dual NPN-PNP complementary power bipolar transistor manufactured by using the latest low voltage planar technology. The STS01DTP06 is housed in dual island SO-8 package with separated terminals for higher assembly flexibility, specifically recommended to be used in Push-Pull or Totem Pole configuration as post IGBTs and MOSFETs driver.

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 2: Order Codes**

Part Number	Marking	Package	Packaging
STS01DTP06T4	S01DTP06	SO-8	Tape & Reel



## STS01DTP06

**Table 3: Absolute Maximum Ratings**

Symbol	Parameter	NPN	PNP	Unit
$V_{CBO}$	Collector-Base Voltage ( $I_E = 0$ )	60	-60	V
$V_{CEO}$	Collector-Emitter Voltage ( $I_B = 0$ )	30	-30	V
$V_{EBO}$	Emitter-Base Voltage ( $I_C = 0$ )	5	-5	V
$I_C$	Collector Current	3	-3	A
$I_{CM}$	Collector Peak Current ( $t_p < 5ms$ )	6	-6	A
$I_B$	Base Current	1	-1	A
$I_{BM}$	Base Peak Current ( $t_p < 1ms$ )	2	-2	A
$P_{tot}$	Total Dissipation at $T_C = 25\text{ }^\circ\text{C}$ single	2		W
$P_{tot}$	Total Dissipation at $T_C = 25\text{ }^\circ\text{C}$ couple	1.6		W
$T_{stg}$	Storage Temperature	-65 to 150		$^\circ\text{C}$
$T_J$	Max. Operating Junction Temperature	150		$^\circ\text{C}$

For PNP type voltage and current values are negative.

**Table 4: Thermal Data**

Symbol	Parameter	Max	Unit
$R_{thj-amb}^{(1)}$	Thermal Resistance Junction-ambient (Single Operation)	62.5	$^\circ\text{C/W}$
$R_{thj-amb}^{(1)}$	Thermal Resistance Junction-ambient (Dual Operation)	78	$^\circ\text{C/W}$

(1) When mounted on 1 inch square pad of 2 oz. copper,  $t \leq 10$  sec

**Table 5: Q1-NPN Transistor Electrical Characteristics ( $T_{case} = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{CBO}$	Collector Cut-off Current ( $I_E = 0$ )	$V_{CB} = 60\text{ V}$			0.1	$\mu\text{A}$
$I_{CEO}$	Collector Cut-off Current ( $I_B = 0$ )	$V_{CE} = 30\text{ V}$			1	$\mu\text{A}$
$I_{EBO}$	Emitter Cut-off Current ( $I_C = 0$ )	$V_{EB} = 5\text{ V}$			1	$\mu\text{A}$
$V_{(BR)CEO}^*$	Collector-Emitter Breakdown Voltage ( $I_B = 0$ )	$I_C = 10\text{ mA}$	30			V
$V_{CE(sat)}^*$	Collector-Emitter Saturation Voltage	$I_C = 1\text{ A}$		0.35	1	V
		$I_C = 2\text{ A}$	$I_B = 10\text{ mA}$ $I_B = 100\text{ mA}$		0.7	V
$V_{BE(sat)}^*$	Base-Emitter Saturation Voltage	$I_C = 1\text{ A}$		0.85	1.1	V
$h_{FE}^*$	DC Current Gain	$I_C = 1\text{ A}$	$V_{CE} = 2\text{ V}$	100		
		$I_C = 3\text{ A}$	$V_{CE} = 2\text{ V}$	30		

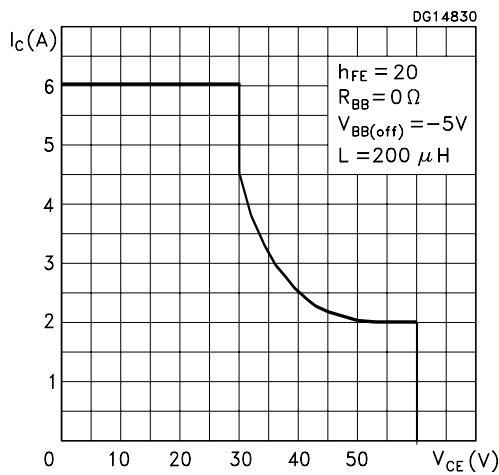
\* Pulsed: Pulsed duration = 300  $\mu\text{s}$ , duty cycle  $\leq 1.5\%$ .

**Table 6: Q2-PNP Transistor Electrical Characteristics ( $T_{case} = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$I_{CBO}$	Collector Cut-off Current ( $I_E = 0$ )	$V_{CB} = -60\text{ V}$				-0.1	$\mu\text{A}$
$I_{CEO}$	Collector Cut-off Current ( $I_B = 0$ )	$V_{CE} = -30\text{ V}$				-1	$\mu\text{A}$
$I_{EBO}$	Emitter Cut-off Current ( $I_C = 0$ )	$V_{EB} = -5\text{ V}$				-1	$\mu\text{A}$
$V_{(BR)CEO}^*$	Collector-Emitter Breakdown Voltage ( $I_B = 0$ )	$I_C = -10\text{ mA}$		-30			V
$V_{CE(sat)}^*$	Collector-Emitter Saturation Voltage	$I_C = -1\text{ A}$	$I_B = -10\text{ mA}$		-0.35	-1	V
		$I_C = -2\text{ A}$	$I_B = -100\text{ mA}$			-0.7	V
$V_{BE(sat)}^*$	Base-Emitter Saturation Voltage	$I_C = -1\text{ A}$	$I_B = -10\text{ mA}$		-0.85	-1.1	V
$h_{FE}^*$	DC Current Gain	$I_C = -1\text{ A}$	$V_{CE} = -2\text{ V}$	100			
		$I_C = -3\text{ A}$	$V_{CE} = -2\text{ V}$	30			

\* Pulsed: Pulsed duration = 300  $\mu\text{s}$ , duty cycle  $\leq 1.5\%$ .

**Figure 3: Reverse Biased Area Q1 NPN Transistor**



**Figure 4: DC Current Gain Q1 NPN Transistor**

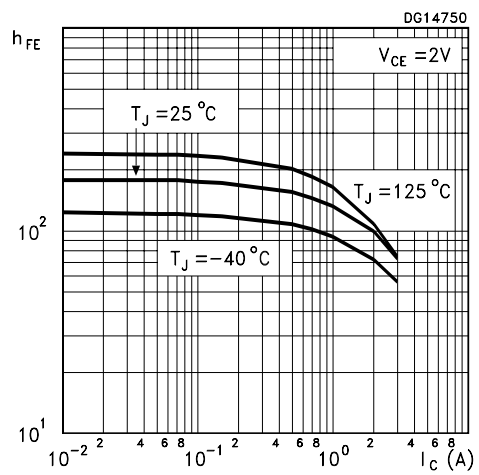


Figure 5: DC Current Gain Q1 NPN Transistor

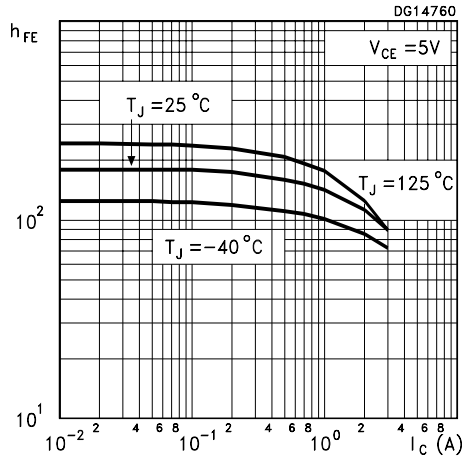


Figure 6: Base-Emitter Saturation Voltage Q1 NPN Transistor

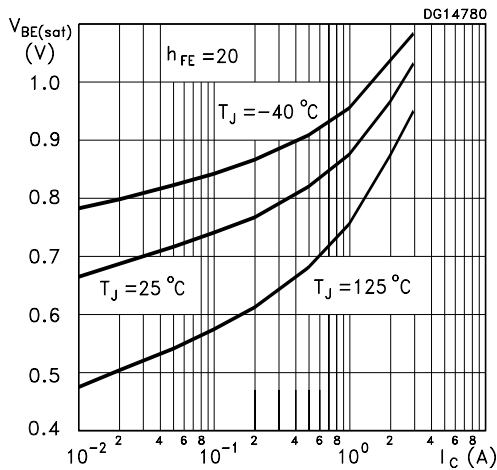


Figure 7: DC Current Gain Q2 PNP Transistor

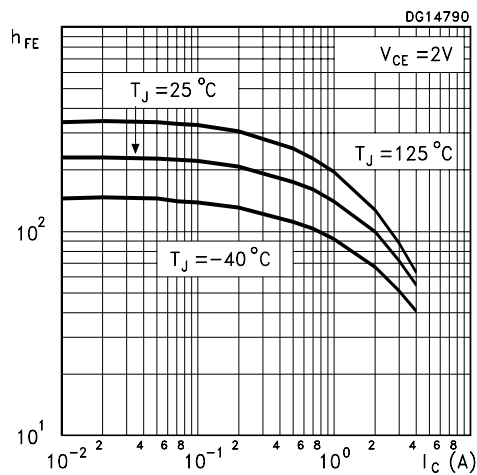


Figure 8: Collector-Emitter Saturation Voltage Q1 NPN Transistor

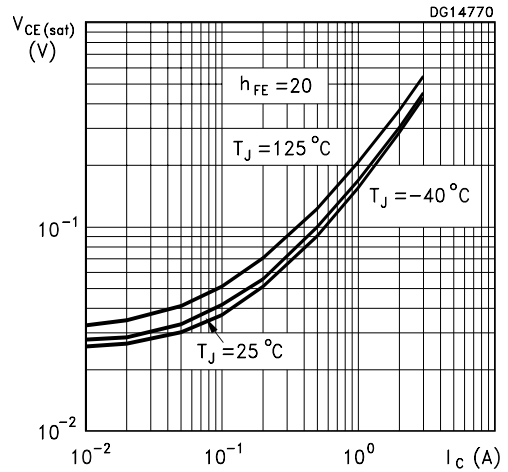


Figure 9: Reverse Biased Area Q2 PNP Transistor

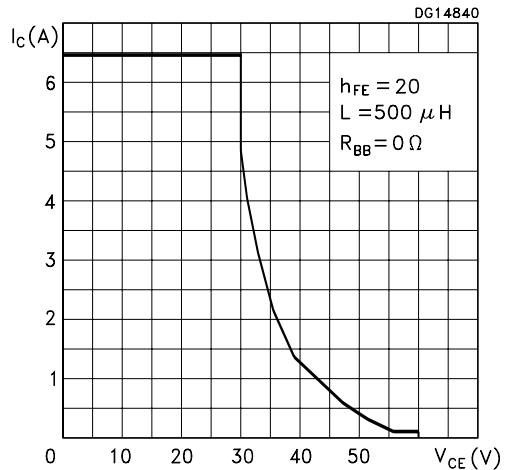
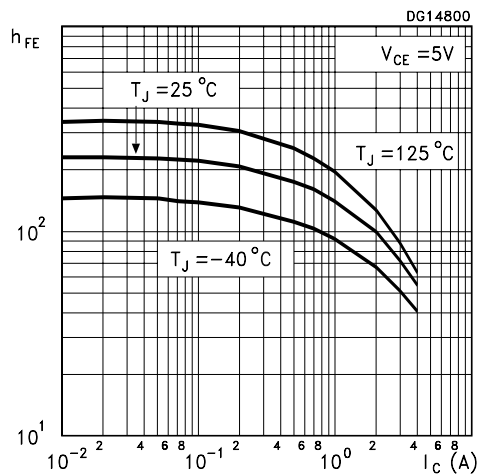
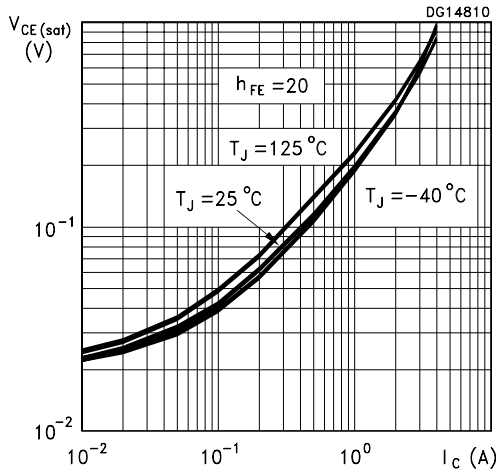


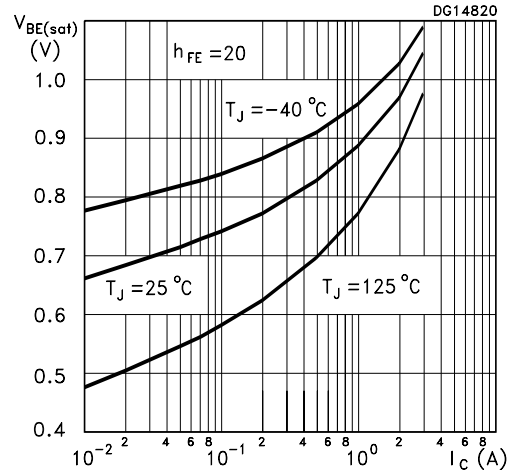
Figure 10: DC Current Gain Q2 PNP Transistor



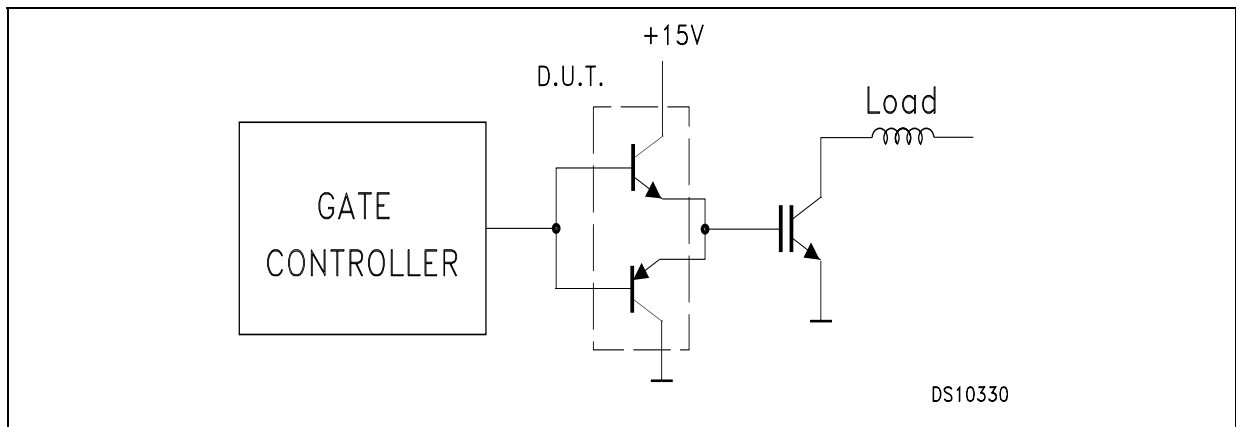
**Figure 11: Collector-Emitter Saturation Voltage Q2 PNP Transistor**



**Figure 12: Base-Emitter Saturation Voltage Q2 PNP Transistor**



**Figure 13: Typical Application**



## STS01DTP06

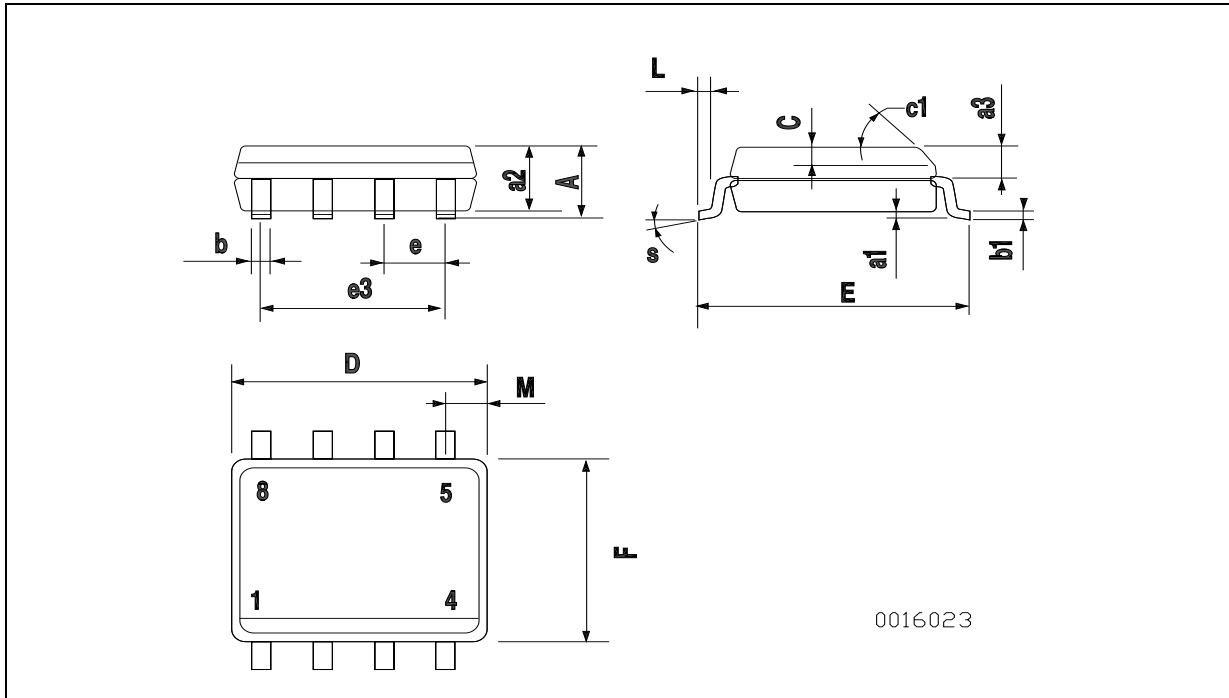
---

**Table 7: Revision History**

Version	Release Date	Change Designator
22-Apr-2005	1	First Release.

**SO-8 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics  
All other names are the property of their respective owners

© 2005 STMicroelectronics - All Rights Reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -  
Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America  
[www.st.com](http://www.st.com)