STSJ18NF3LL

N-CHANNEL 30V - 0.016 Ω - 18A PowerSO-8™ LOW GATE CHARGE STripFET™ II POWER MOSFET

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STSJ18NF3LL	30 V	<0.019 Ω	18 A

- TYPICAL $R_{DS}(on)$ = 0.016 Ω @ 10V
- TYPICAL Q_g = 12.5 nC @ 4.5 V
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- IMPROVED JUNCTION-CASE THERMAL RESISTANCE

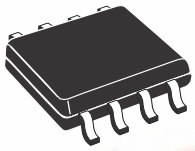
DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. This silicon, housed in thermally improved SO-8™ package, exhibits optimal on-resistance versus gate charge trade-off plus lower R_{thj-c}.

APPLICATIONS

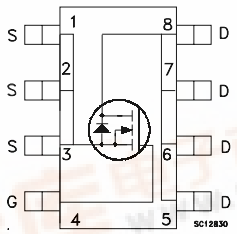
- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS FOR MOBILE PCS

Figure 1:Package



PowerSO-8™

Figure 2: Internal Schematic Diagram



DRAIN CONTACT ALSO ON THE BACKSIDE

Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STSJ18NF3LL	18F3LL)	PowerSO-8	TAPE & REEL

Table 3: ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	30	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	30	V
V_{GS}	Gate- source Voltage	± 16	V
I_D	Drain Current (continuous) at T_C = 25°C (*)	18	A
I_D	Drain Current (continuous) at T_C = 100°C(*)	18	A
I_{DM}(•)	Drain Current (pulsed)	72	A
P_{tot}	Total Dissipation at T_C = 25°C Total Dissipation at T_C = 25°C (#)	70 3	W W

(•) Pulse width limited by safe operating area. (*) Value limited by wires bonding

Table 4: THERMAL DATA

Rthj-c	Thermal Resistance Junction-case	Max	1.8	°C/W
Rthj-amb	(*)Thermal Resistance Junction-ambient	Max	41.7	°C/W
T_j	Maximum Operating Junction Temperature		150	°C
T_{stg}	Storage Temperature		-55 to 150	°C

(*) When Mounted on FR-4 board with 1 inch² pad, 2 oz of Cu and t ≤ 10 sec.

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

Table 5: OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	30			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 16 V			±100	nA

Table 6: ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 9 A V_{GS} = 4.5 V I_D = 9 A		0.016 0.019	0.019 0.022	Ω Ω

Table 7: DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS}=15 V I_D = 9 A		17		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		800 250 60		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

Table 8: SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 15 V I_D = 9 A R_G = 4.7 Ω V_{GS} = 4.5 V (Resistive Load, Figure 15)		18 32		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}=15V I_D=18A V_{GS}=4.5V (see test circuit, Figure 16)		12.5 3.2 4.5	17	nC nC nC

Table 9: SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 15 V I_D = 9 A R_G = 4.7Ω, V_{GS} = 4.5 V (Resistive Load, Figure 17)		21 11		ns ns

Table 10: SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				18 72	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 18 A V_{GS} = 0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 18 A di/dt = 100A/µs V_{DD} = 15 V T_j = 150°C (see test circuit, Figure 17)		23 17 1.5		ns nC A

(•)Pulse width limited by safe operating area.
(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

Figure 3: Safe Operating Area

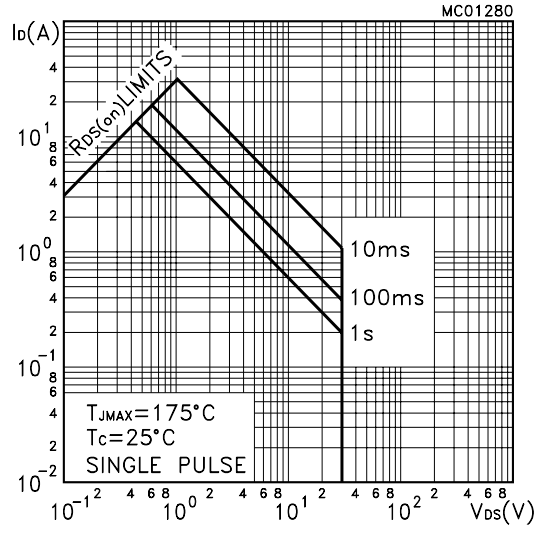


Figure 4: Thermal Impedance

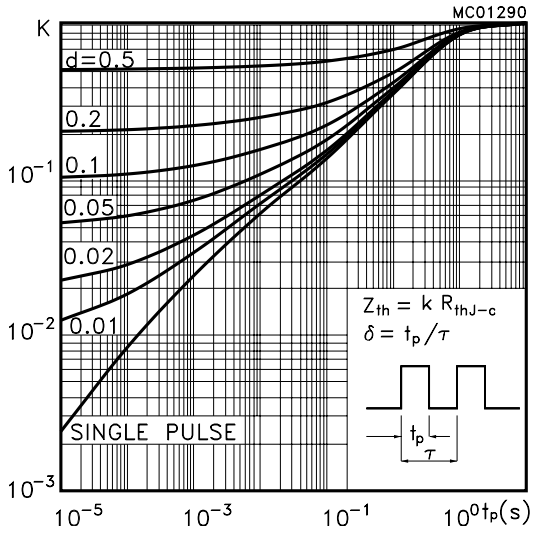


Figure 5: Output Characteristics

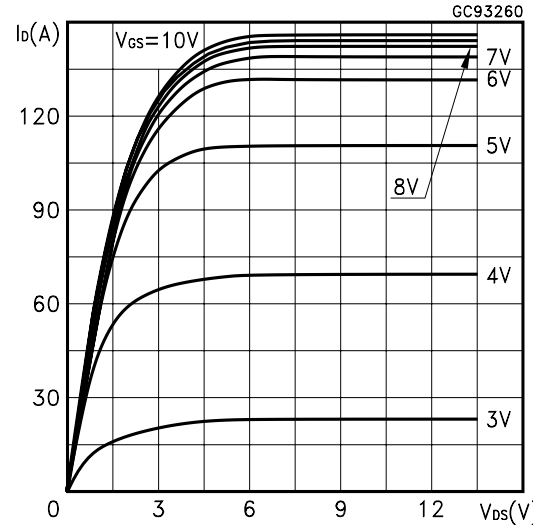


Figure 6: Transfer Characteristics

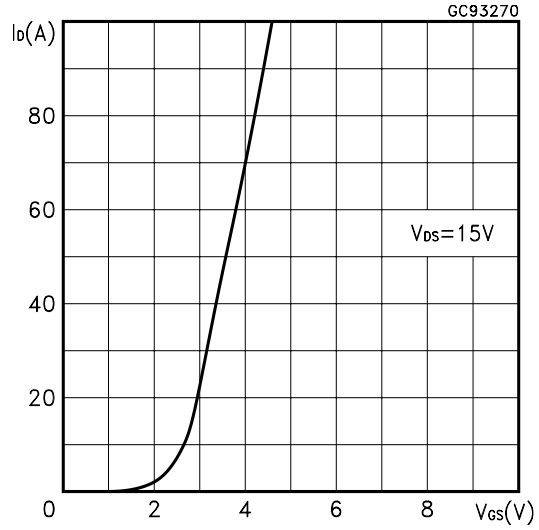


Figure 7: Transconductance

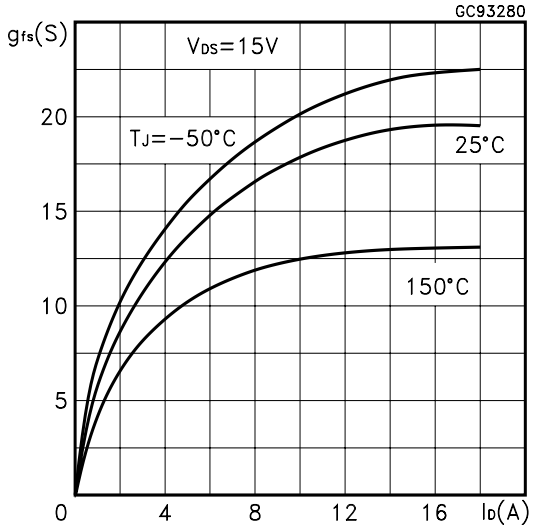


Figure 8: Static Drain-source On Resistance

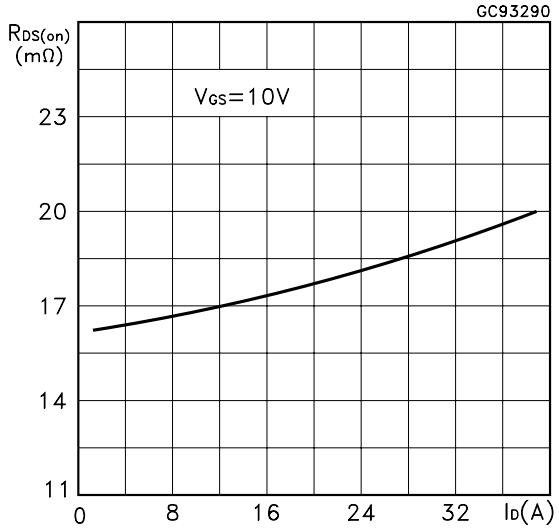


Figure 9: Gate Charge vs Gate-source Voltage

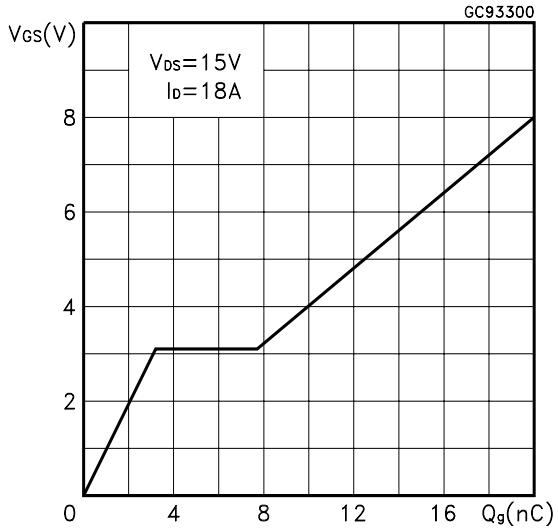


Figure 10: Capacitance Variations

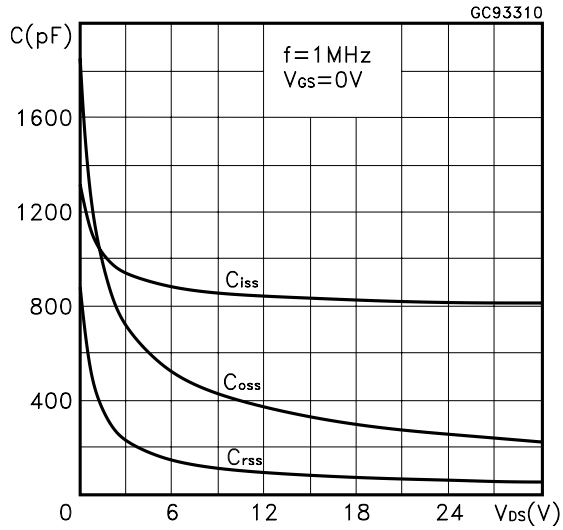


Figure 11: Normalized Gate Threshold Voltage vs Temperature

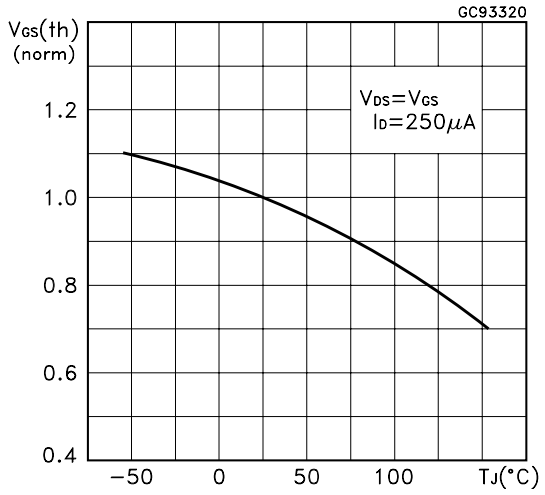


Figure 12: Normalized on Resistance vs Temperature

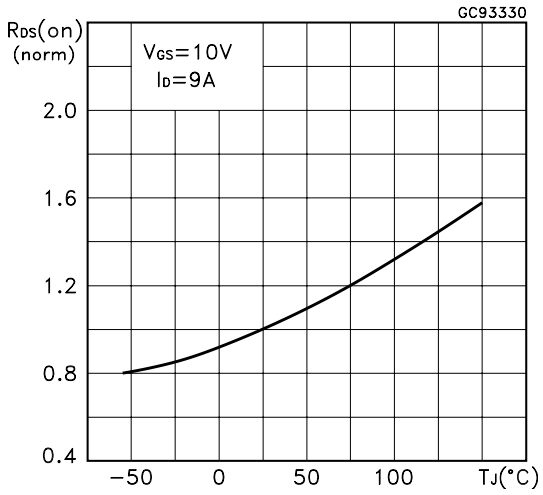


Figure 13: Source-drain Diode Forward Characteristics

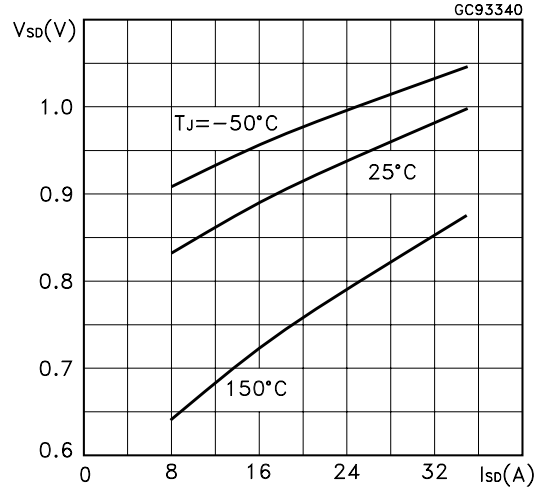


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Figure 14: Normalized Breakdown Voltage vs Temperature.

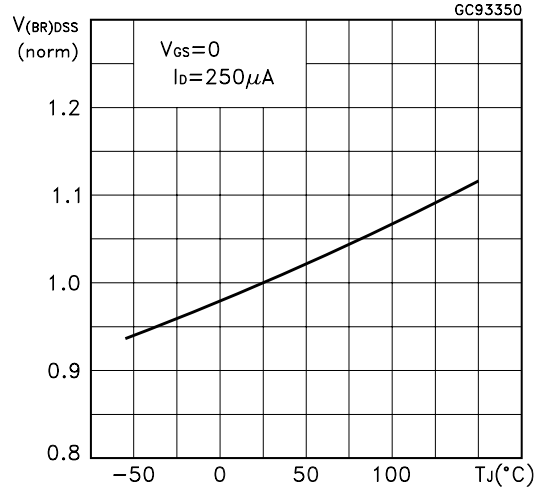

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Fig. 15 Switching Times Test Circuits For Resistive Load

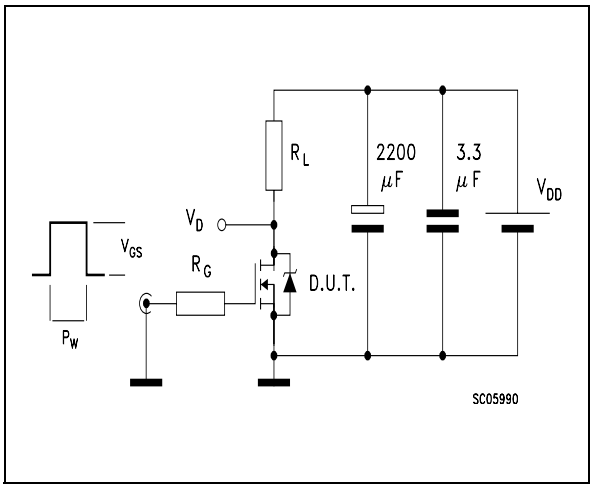


Fig.16: Gate Charge test Circuit

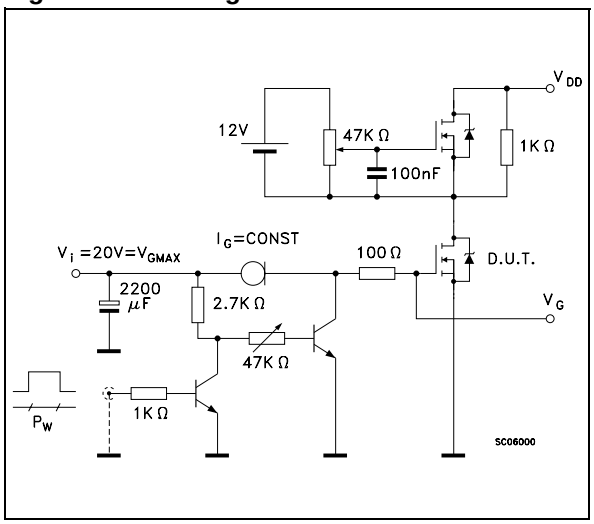
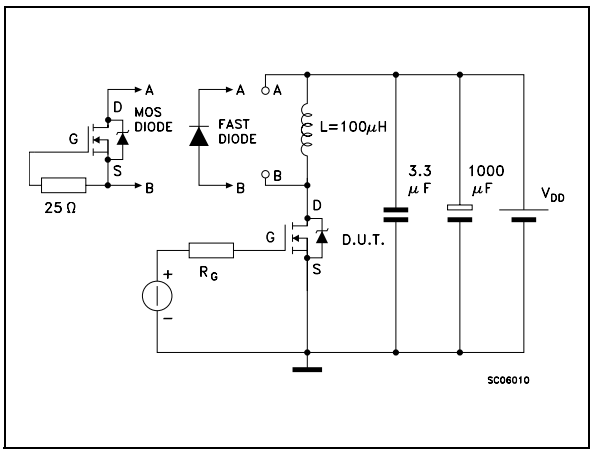


Fig. 17: Test Circuit For Diode Recovery Behaviour



PowerSO-8™ MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45° (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
e4		2.79			0.110	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8° (max.)					

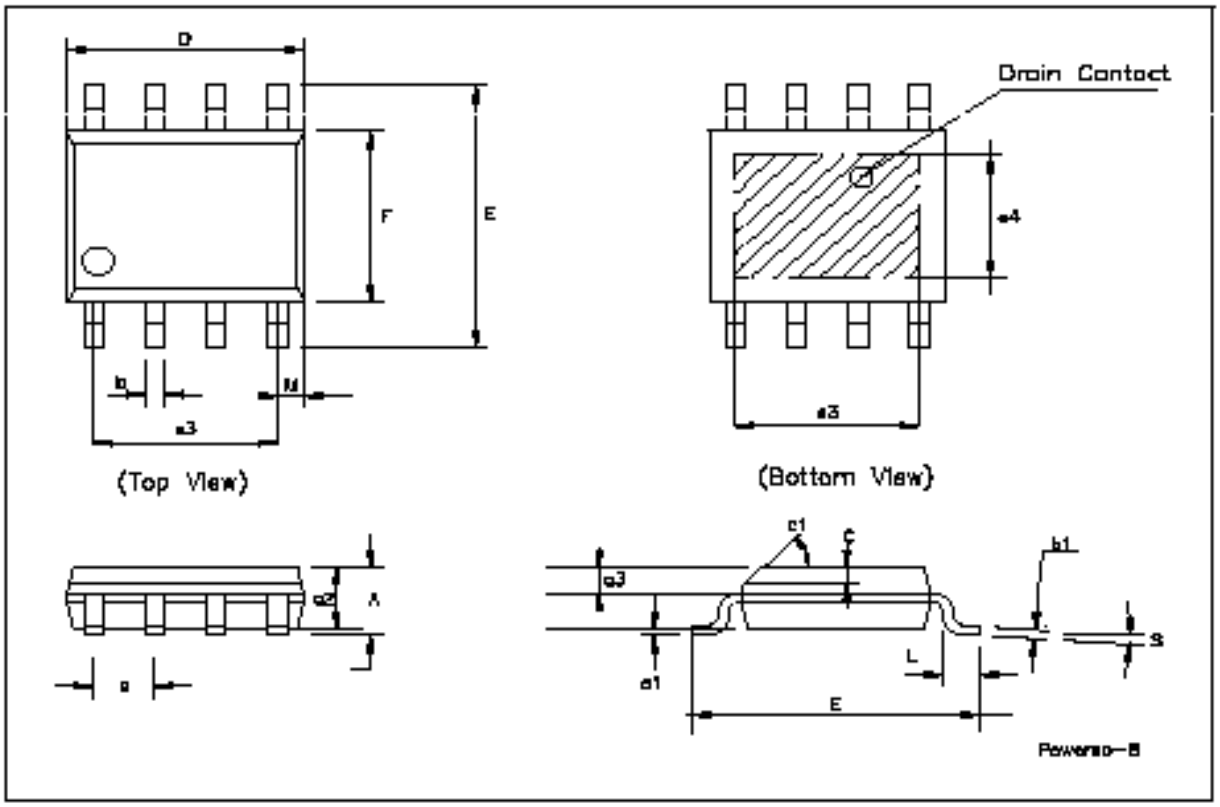


Table 11:Revision History

Date	Revision	Description of Changes
March 2005	1.0	FIRST ISSUE