



# STT4NF30L

## N - CHANNEL 30V - 0.055Ω - 4A - TSOP-6 STripFET™ MOSFET

PRELIMINARY DATA

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STT4NF30L	30 V	< 0.065 Ω	4 A

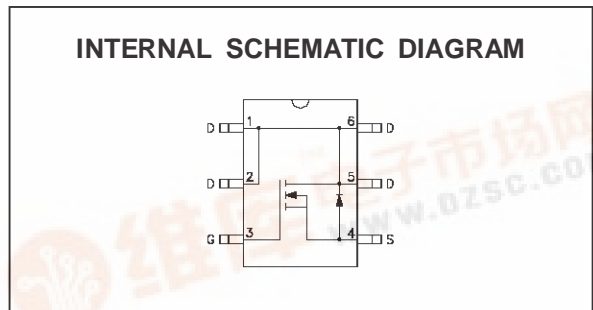
- TYPICAL R<sub>DS(on)</sub> = 0.055 Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

### DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### APPLICATIONS

- DC MOTOR DRIVE
- DC-DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN PORTABLE/DESKTOP PCs



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	30	V
V <sub>DGR</sub>	Drain- gate Voltage (R <sub>GS</sub> = 20 kΩ)	30	V
V <sub>GS</sub>	Gate-source Voltage	± 20	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 25 °C	4	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 100 °C	2.5	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	16	A
P <sub>tot</sub>	Total Dissipation at T <sub>c</sub> = 25 °C	2	W

(●) Pulse width limited by safe operating area

## STT4NF30L

### THERMAL DATA

R <sub>thj-amb</sub>	(*)Thermal Resistance Junction-ambient	Max	62.5	°C/W
T <sub>J</sub>	Maximum Operating Junction Temperature		150	°C
T <sub>stg</sub>	Storage Temperature		-55 to 150	°C

(\*) Mounted on FR-4 board (t ≤ 5 sec)

### ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA V <sub>GS</sub> = 0	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			± 100	nA

ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 μA	1	1.7	2.5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V I <sub>D</sub> = 2 A V <sub>GS</sub> = 4.5V I <sub>D</sub> = 2 A		0.055 0.06	0.065 0.09	Ω Ω
I <sub>D(on)</sub>	On State Drain Current	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> V <sub>GS</sub> = 10 V	4			A

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> I <sub>D</sub> = 6 A		6		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V f = 1 MHz V <sub>GS</sub> = 0		420	550	pF
C <sub>oss</sub>	Output Capacitance			62	80	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			20	30	pF

**ELECTRICAL CHARACTERISTICS** (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	$V_{DD} = 15\text{ V}$ $I_D = 2\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (see test circuit, figure 3)		13	17	ns
$t_r$	Rise Time			30	40	ns
$Q_g$	Total Gate Charge	$V_{DD} = 24\text{ V}$ $I_D = 4\text{ A}$ $V_{GS} = 4.5\text{ V}$		8	12	nC
$Q_{gs}$	Gate-Source Charge			3.2		nC
$Q_{gd}$	Gate-Drain Charge			2.6		nC

**SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 24\text{ V}$ $I_D = 4\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (see test circuit, figure 5)		6	8	ns
$t_f$	Fall Time			9	12	ns
$t_c$	Cross-over Time			20	26	ns

**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				4	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				16	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 4\text{ A}$ $V_{GS} = 0$			1.2	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 4\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, figure 5)		22		ns
$Q_{rr}$	Reverse Recovery Charge			13		nC
$I_{RRM}$	Reverse Recovery Current			1.2		A

(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

(\bullet) Pulse width limited by safe operating area

# STT4NF30L

Fig. 1: Unclamped Inductive Load Test Circuit

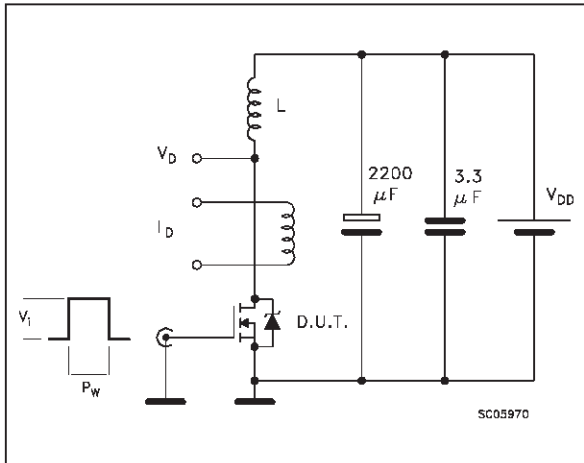


Fig. 2: Unclamped Inductive Waveform

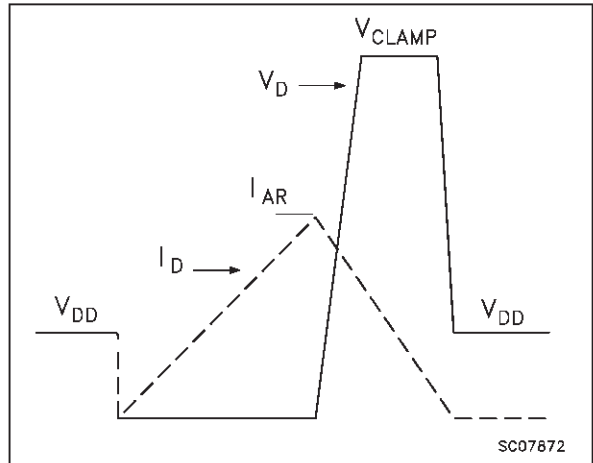


Fig. 3: Switching Times Test Circuits For Resistive Load

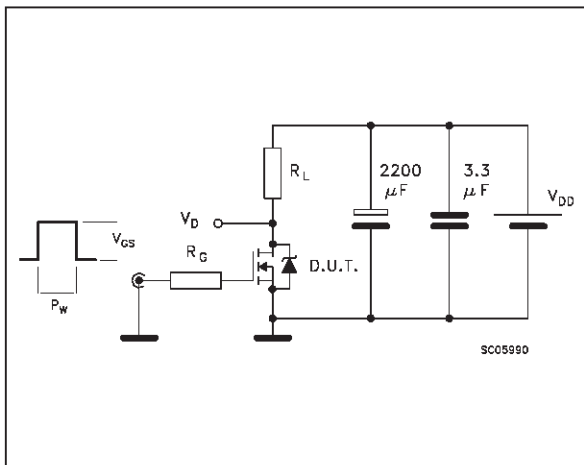


Fig. 4: Gate Charge test Circuit

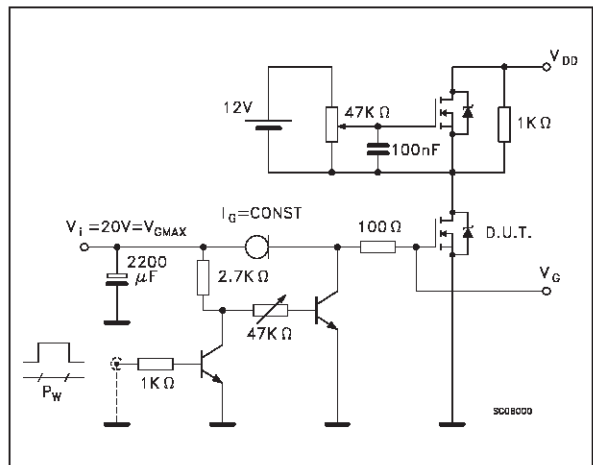
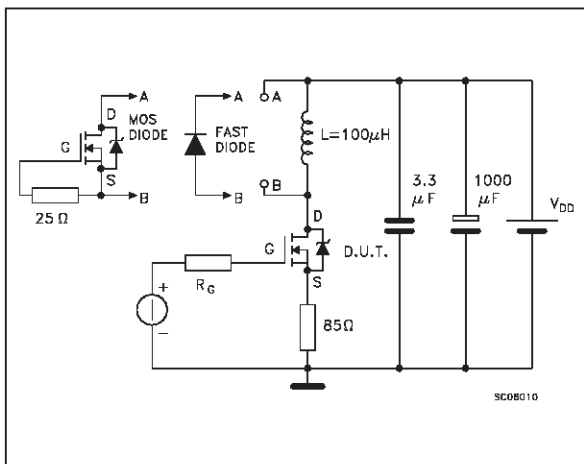


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 1998 STMicroelectronics – Printed in Italy – All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - France - Germany - Italy - Japan - Korea - Malaysia - Malta - Mexico - Morocco - The Netherlands -  
Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.

<http://www.st.com>