SGS-THOMSON MICROELECTRONICS

STV0042A

SATELLITE SOUND AND VIDEO PROCESSORS

PRODUCT PREVIEW

SOUND

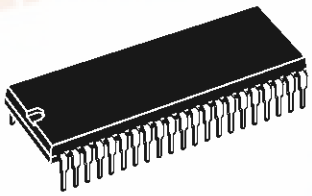
- TWO INDEPENDENT SOUND DEMODULATORS
- PLL DEMODULATION WITH 5-10MHz FREQUENCY SYNTHESIS
- PROGRAMMABLE FM DEMODULATOR BANDWIDTH ACCOMODATING FM DEVIATIONS FROM ±30kHz TILL ±400kHz
- PROGRAMMABLE 50/75µs OR NO DE-EMPHASIS
- DYNAMIC NOISE REDUCTION
- ONE OR TWO AUXILIARY AUDIO INPUTS AND OUTPUTS
- GAIN CONTROLLED AND MUTEABLE AUDIO OUTPUTS
- HIGH IMPEDANCE MODE AUDIO OUTPUTS FOR TWIN TUNER APPLICATIONS

VIDEO

- COMPOSITE VIDEO 6-bit 0 to 12.7dB GAIN CONTROL
- COMPOSITE VIDEO SELECTABLE INVERTER
- TWO SELECTABLE VIDEO DE-EMPHASIS NETWORKS
- 4 x 2 VIDEO MATRIX
- HIGH IMPEDANCE MODE VIDEO OUTPUTS FOR TWIN TUNER APPLICATIONS

MISCELLANEOUS

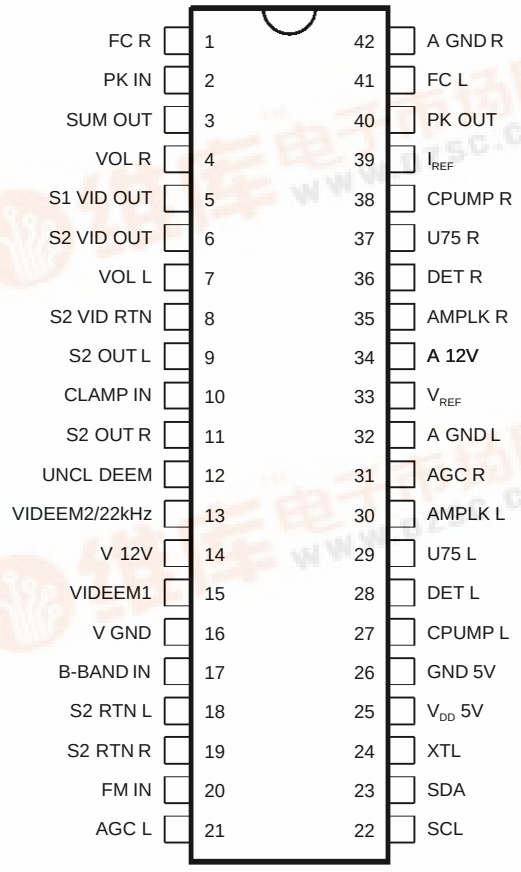
- 22kHz TONE GENERATION FOR LNB CONTROL
- I^2C BUS CONTROL :
  CHIP ADDRESSES = 06_{HEX}
- LOW POWER STAND-BY MODE WITH ACTIVE AUDIO AND VIDEO MATRIXES



SHRINK42
(Plastic Package)

ORDER CODE : STV0042A

PIN CONNECTIONS



0042A-01.EPS

DESCRIPTION

The STV0042A BICMOS integrated circuit realizes all the necessary signal processing from the tuner to the Audio/Video input and output connectors regardless the satellite system.

The STV0042 is intended for low cost satellite receiver application.

PIN ASSIGNMENT

Pin Number	Name	Function
1	FC R	Audio Roll-off Right
3	SUM OUT	Noise Reduction Summing Output
2	PK IN	Noise Reduction Peak Detector Input
4	VOL R	Volume Controlled Audio Out Right
5	S1 VID OUT	TV-Scart 1 Video Output
6	S2 VID OUT	VCR-Scart 2 Video Output
7	VOL L	Volume Controlled Audio Out Left
8	S2 VID RTN	VCR-Scart 2 Video Return
9	S2 OUT L	Fixed Level Audio Output Left
10	CLAMP IN	Sync-Tip Clamp Input
11	S2 OUT R	Fixed Level Audio Output Right
12	UNCL DEEM	Unclamped Deemphasized Video Output
13	VIDEEM2/22kHz	Video Deemphasis 2 or 22kHz Output
14	V 12V	Video 12V Supply
15	VIDEEM1	Video Deemphasis 1
16	V GND	Video Ground
17	B-BAND IN	Base Band Input
18	S2 RTN L	Auxiliary Audio Return Left
19	S2 RTN R	Auxiliary Audio Return Right
20	FM IN	FM Demodulator Input
21	AGC L	AGC Peak Detector Capacitor Left
22	SCL	I^2C Bus Clock
23	SDA	I^2C Bus Data
24	XTL	4/8MHz Quartz Crystal or Clock Input
25	V_{DD} 5V	Digital 5V Power Supply
26	GND 5V	Digital Power Ground
27	CPUMP L	FM PLL Charge Pump Capacitor Left
28	DET L	FM PLL Filter Left
29	U75 L	Deemphasis Time Constant Left
30	AMPLK L	Amplitude Detector Capacitor Left
31	AGC R	AGC Peak Detector Capacitor Right
32	A GND L	Audio Ground
33	V_{REF}	2.4V Reference
34	A 12V	Audio 12V Supply
35	AMPLK R	Amplitude Detector Capacitor Left
36	DET R	FM PLL Filter Right
37	U75 R	Deemphasis Time Constant Right
38	CPUMP R	FM PLL Charge Pump Capacitor Right
39	I_{REF}	Current Reference Resistor
40	PK OUT	Noise Reduction Peak Detector Output
41	FC L	Audio Roll-off Left
42	A GND R	Audio Ground

0042A-01.TBL

PIN DESCRIPTION

1 - Sound Detection

FMIN

This is the input to the two FM demodulators. It feeds two AGC amplifiers with a bandwidth of at least 5-10MHz. There is one amplifier for each channel both with the same input. The AGC amplifiers have a 0dB to +40dB range.
Z_{IN} = 5kΩ, Min input = 2mV_{PP} per subcarrier.
Max input = 500mV_{PP} (max when all inputs are added together, when their phases coincide).

AGC L, AGC R

AGC amplifiers peak detector capacitor connections. The output current has an attack/decay ratio of 1:32. That is the ramp up current is approximately 5µA and decay current is approximately 160µA. 11V gives maximum gain. These pins are also driven by a circuit monitoring the voltage on AMPLK L and AMPLK R respectively.

AMPLK L, AMPLK R

The outputs of amplitude detectors LEFT and RIGHT. Each requires a capacitor and a resistor to GND. The voltage across this is used to decide whether there is a signal being received by the FM detector. The level detector output drives a bit in the detector I^2C bus control block.
AMPLK L and AMPLK R drive also respectively AGC L and AGC R. For instance when the voltage on AMPLK L is > (V_{REF} + 1 V_{BE}) it sinks current to V_{REF} from pin AGCL to reduce the AGC gain.

DET L, DET R

Respectively the outputs of the FM phase detector left and right. This is for the connection of an external loop filter for the PLL. The output is a push-pull current source.

CPUMP L, CPUMP R

The output from the frequency synthesizer is a push-pull current source which requires a capacitor to ground to derive a voltage to pull the VCO to the target frequency. The output is ±100µA to achieve lock and ±2µA during lock to provide a tracking time constant of approximately 10Hz.

VREF

This is the audio processor voltage reference used through out the FM/audio section of the chip. As such it is essential that it is well decoupled to ground to reduce as far as possible the risk of crosstalk and noise injection. This voltage is derived directly from the bandgap reference of 2.4V. The V_{REF} output can sink up to 500µA in normal operation and 100µA when in stand-by.

IREF

This is a buffered V_{REF} output to an off-chip resistor to produce an accurate current reference, within the chip, for the biasing of amplifiers with current outputs into filters. It is also required for the Noise reduction circuit to provide accurate roll-off frequencies.
This pin should not be decoupled as it would inject current noise. The target current is 50µA ±2% thus a 47.5kΩ ±1% is required.

A 12V

Double bonded main power pin for the audio/FM section of the chip. The two bond connections are to the ESD and to power the circuit and on chip regulators/references.

A GND L

This ground pin is double bonded :
1) to channel LEFT : RF section & VCO,
2) to both AGC amplifiers, channel LEFT and RIGHT audio filter section.

A GND R

This ground pin is double bonded :
1) to the volume control, noise reduction system, ESD + Mux + V_{REF}
2) to channel right : RF section & VCO

2 - Baseband Audio Processing

PK OUT

The noise reduction control loop peak detector output requires a capacitor to ground from this pin, and a resistor to V_{REF} pin to give some accurate decay time constant. An on chip 5kΩ ±25 % resistor and external capacitor give the attack time.

PK IN

This pin is an input to a control loop peak detector and is connected to the output of the offchip control loop band pass filter.

SUM OUT

The two audio demodulated signals are summed together by means of an amplifier with a gain of 0.5. If both inputs are 1V then the output is 1V. This amplifier has an input follower buffer which gives a V_{BE} offset in the DC bias voltage. Thus the filter which this amplifier drives must include AC coupling to the next stage (PK IN Pin).

FC L, FC R

The variable bandwidth transconductance amplifier has a current output which is variable depending on the input signal amplitude as defined by the control loop of the noise reduction. The output current is then dumped into an off-chip capacitor which together with the accurate current reference define the min/max rolloff frequencies. A resistor in series with a capacitor is connected to ground from these two pins.

PIN DESCRIPTION (continued)

U75 L, U75 R

External deemphasis networks for channels left and right. For each channel a capacitor and resistor in parallel of 75µs time constant are connected between here and V_{REF} to provide 75µs de-emphasis. Internally selectable is an internal resistor that can be programmed to be added in parallel thereby converting the network to approx 50µs de-emphasis (see control block map). The value of the internal resistors is 30kΩ ±30%. The amplifier for this filter is voltage input, current output; with ±500mV input the output will be ±55µA.

VOL L, VOL R

The main audio output from the volume control amplifier the signal to get output signals as high as $2V_{RMS}$ (+12dB) on a DC bias of 4.8V. Control is from +12dB to -26.75dB plus Mute with 1.25dB steps. This amplifier has short circuit protection and is intended to drive a SCART connector directly via AC coupling and meets the standard SCART drive requirements. These outputs feature high impedance mode for parallel connection.

S2 OUT L, S2 OUT R

These audio outputs are sourced directly from the audio MUX, and as a result do not include any volume control function. They will output a $1V_{RMS}$ signal biased at 4.8V. They are short circuit protected. These outputs feature high impedance mode for parallel connection and meet SCART drive requirement.

S2 RTN L, S2 RTN R

These pins allow auxiliary audio signals to be connected to the audio processor and hence makes use of the on-chip volume control. For additional details please refer to the audio switching table.

3 - Video Processing

B-BAND IN

AC-coupled video input from a tuner.
Z_{IN} > 10kΩ ±25%. This drives an on-chip video amplifier. The other input of this amp is AC grounded by being connected to an internal V_{REF}. The video amplifier has selectable gain from 0dB to 12.7dB in 63 steps and its output signal can be selected normal or inverted.

UNCL DEEM

Deemphasized still unclamped output. It is also an input of the video matrix.

VIDEEM1

Connected to an external de-emphasis network (for instance 625 lines PAL de-emphasis).

VIDEEM2 / 22kHz

Connected to an external de-emphasis network (for instance 525 lines NTSC or other video de-emphasis). Alternatively a precise 22kHz tone may be output by I^2C bus control.

CLAMP IN

This pin clamps the most negative extreme of the input (the sync tips) to $2.7V_{DC}$ (or appropriate voltage). The video at the clamp input is only $1V_{PP}$. This clamped video which is de-emphasised, filtered and clamped (energy dispersal removed) is normal, negative syncs, video. This signal drives the Video Matrix input called Normal Video. It has a weak (1.0µA ±15 %) stable current source pulling the input towards GND. Otherwise the input impedance is very high at DC to 1kHz Z_{IN} > 2MΩ. Video bandwidth through this is -1dB at 5.5MHz. The CLAMP input DC restore voltage is then used as a means for getting the correct DC voltage on the SCART outputs.

S2 VID RTN

External video input $1.0V_{PP}$ AC coupled 75Ω source impedance. This input has a DC restoration clamp on its input. The clamp sink current is 1µA ±15% with the buffer Z_{IN} > 1MΩ. This signal is an input to the Video Matrix.

S1 VID OUT, S2 VID OUT

Video drivers for SCART 1 and SCART 2. An external emitter follower buffer is required to drive a 150Ω load. The average DC voltage to be 1.5V on the O/P. The signal is video $2.0V_{PP}$ 5.5MHz BW with sync tip = 1.2V. These pins get signals from the Video Matrix. The signal selected from the Video Matrix for output on this pin is controlled by a control register. This output also feature a high impedance mode for parallel connection.

V 12V

+12V double bonded : ESD+guard rings and video circuit power.

V GND

Doubled bonded. Clean VID IN GND. Strategically placed video power ground connection to reduce video currents getting into the rest of the circuit.

4 - Control Block

GND 5V

The main power ground connection for the control logic, registers, the I^2C bus interface, synthesizer & watchdog and XTLOSC.

VDD 5V

Digital +5V power supply.

SCL

This is the I^2C bus clock line. Clock = DC to 100kHz. Requires external pull up eg. 10kΩ to 5V.

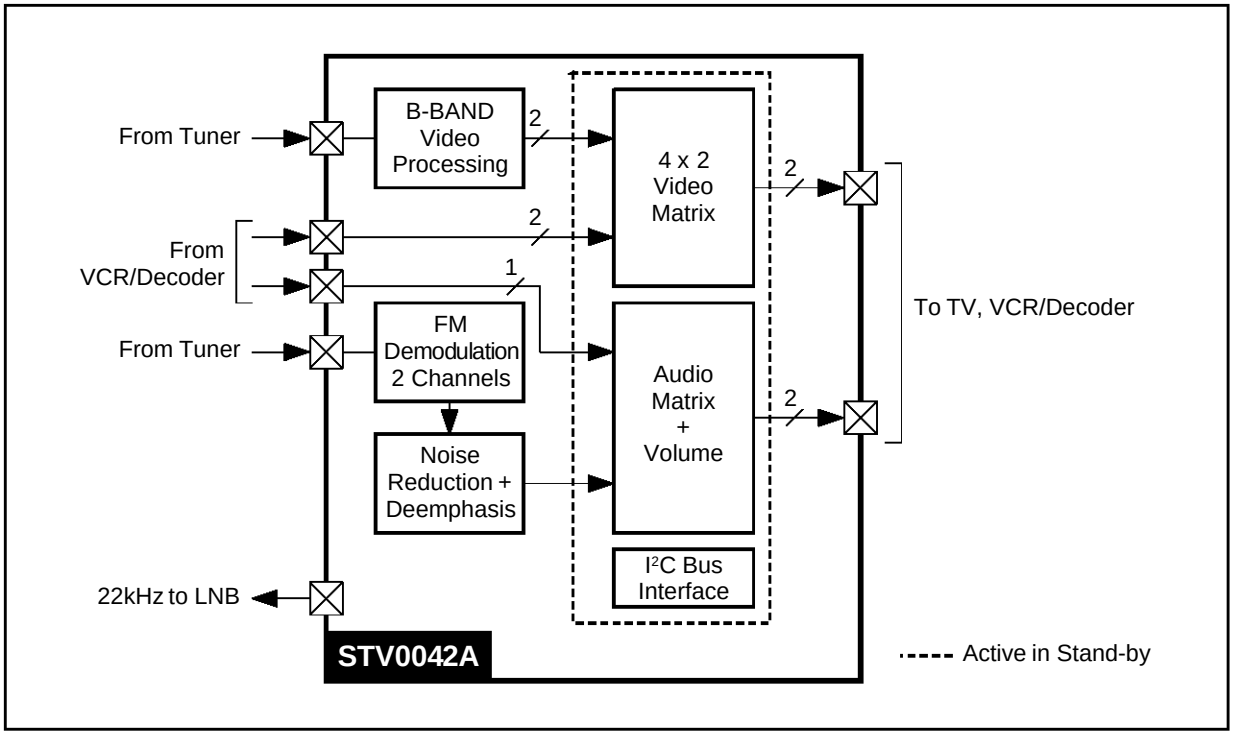
SDA

This is the I^2C bus data line. Requires external pull up eg. 10kΩ to 5V.

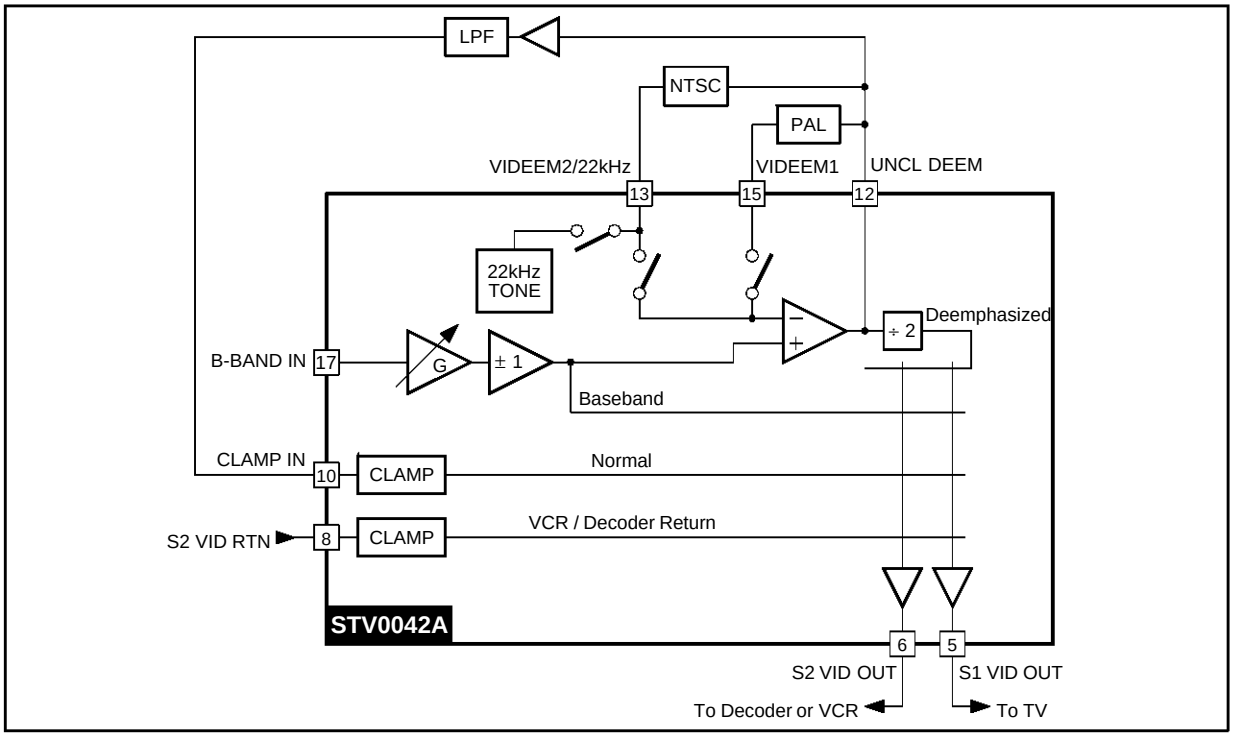
XTL

This pin allows for the on-chip oscillator to be either used with a crystal to ground of 4MHz or 8MHz, or to be driven by an external clock source. The external source can be either 4MHz or 8MHz. A programmable bit in the control block removes a ÷2 block when the 4MHz option is selected.

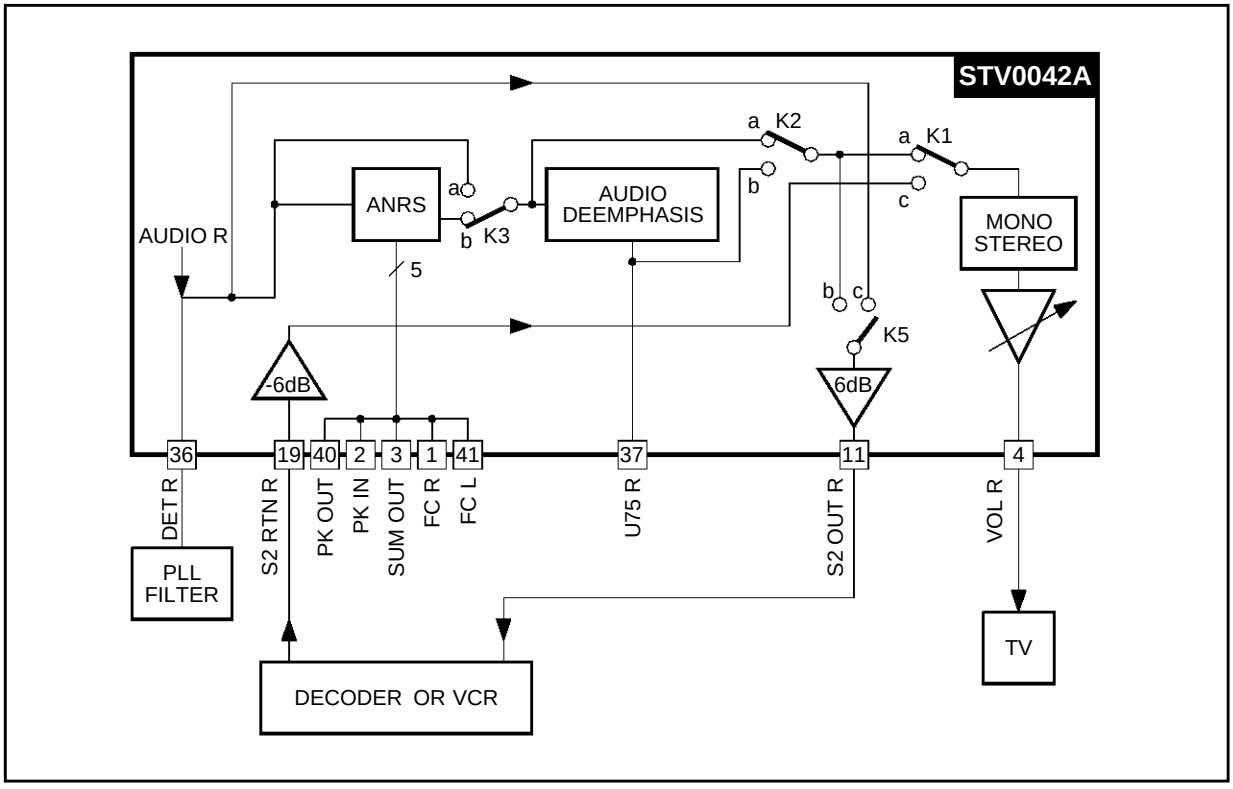
GENERAL BLOCK DIAGRAM



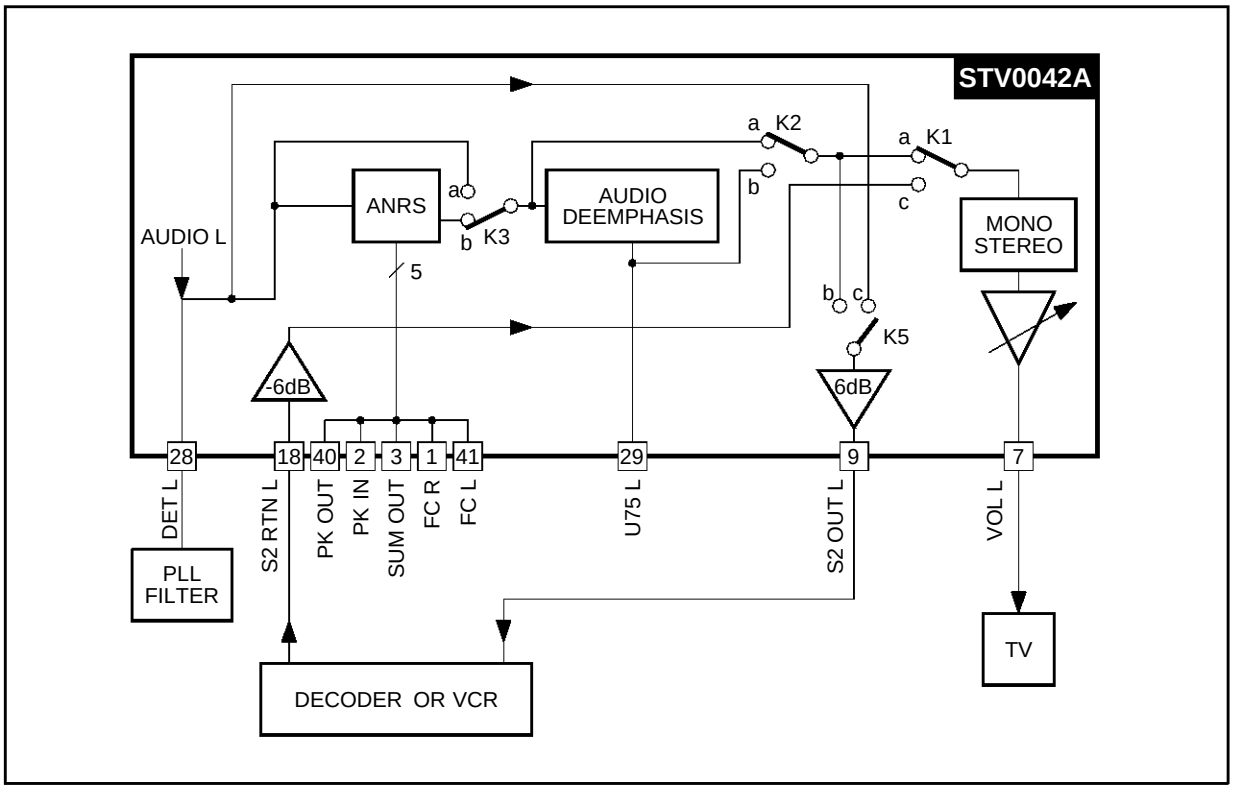
VIDEO PROCESSING BLOCK DIAGRAM



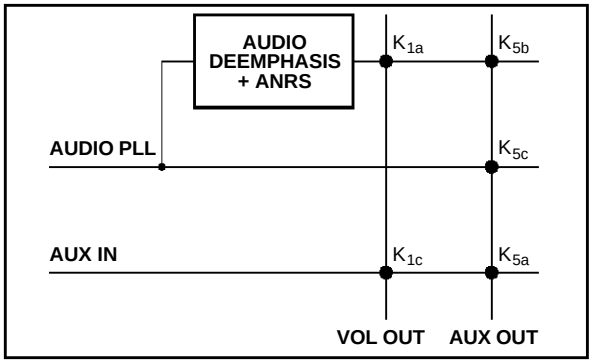
AUDIO PROCESSING BLOCK DIAGRAM (CHANNEL RIGHT)



AUDIO PROCESSING BLOCK DIAGRAM (CHANNEL LEFT)

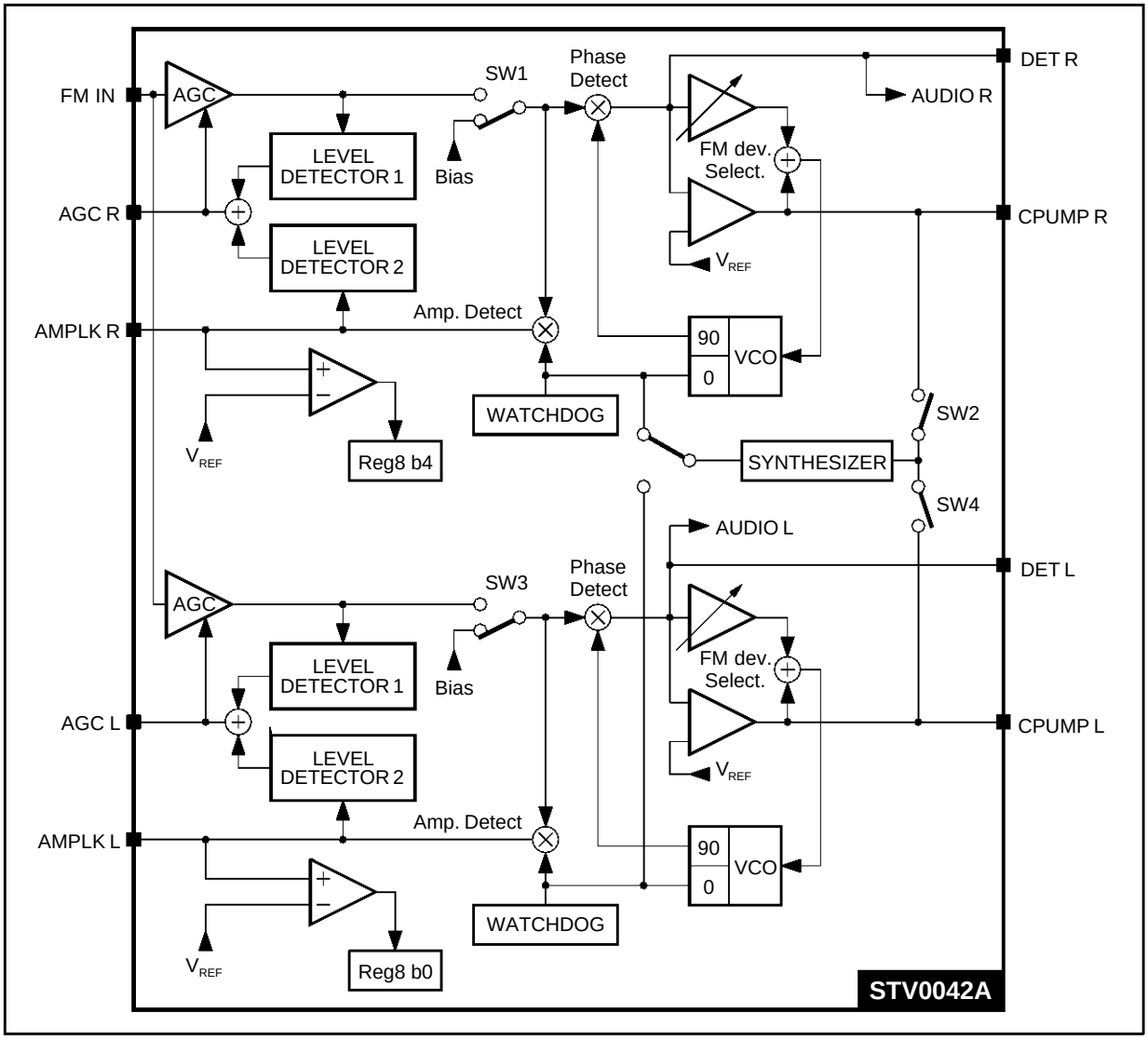


AUDIO SWITCHING



K_2	K_3	
a	ON	No ANRS, No De-emphasis
b_1	ON	No ANRS, 50µs
b_2	ON	No ANRS, 75µs
a	OFF	ANRS, No De-emphasis
b_1	OFF	ANRS, 50µs
b_2	OFF	ANRS, 75µs

FM DEMODULATION BLOCK DIAGRAM



CIRCUIT DESCRIPTION

1 - Video Section

The composite video is first set to a standard level by means of a 64 step gain controlled amplifier. In the case that the modulation is negative, an inverter can be switched in.

One of two different external video de-emphasis networks (for instance PAL and NTSC) is selectable by an integrated bus controlled switch.

Then energy dispersal is removed by a sync tip clamping circuit, which is used on all inputs to a video switching matrix, thus making sure that no DC steps occur when switching video sources.

The matrix can be used to feed video to and from decoders, VCR's and TV's.

Additionaly all the video outputs are tristate type (high impedance mode is supported), allowing a simple parallel connections to the scarts (Twin tuner applications).

2 - Audio Section

The two audio channels are totally independent except for the possibility given to output on both channels only one of the selected input audio channels.

To allow a very cost effective application, each channel uses PLL demodulation. Neither external complex filter nor ceramic filters are needed.

The frequency of the demodulated subcarrier is chosen by a frequency synthesizer which sets the frequency of the internal local oscillator by comparing its phase with the internally generated reference. When the frequency is reached, the microprocessor switches in the PLL and the demodulation starts. At any moment the microprocessor can read from the device (watchdog registers) the actual frequency to which the PLL is locked. It can also verify that a carrier is present at the wanted frequency (by reading AMPLK status bit) thanks to a synchronous amplitude detector, which is also used for the audio input AGC.

In order to maintain constant amplitude of the recovered audio regardless of variations between satellites or subcarriers, the PLL loop gain may be programmed from 56 values.

Any frequency deviation can be accomodated (from ±30kHz till ±400kHz).

In the typical application, the STV0042A offers two audio de-emphasis 75µs and 50µs. When required a J17 de-emphasis can be implemented by using specific application diagram (see Application Note : AN838, Chapter 4.2).

A dynamic noise reduction system (ANRS) is integrated into the STV0042A using a lowpass filter, the cut-off frequency of which is controlled by the amplitude of the audio after insertion of a bandpass filter.

Two types of audio outputs are provided : one is a fixed $1V_{RMS}$ and the other is a gain controlled $2V_{RMS}$ max. The control range being from +12dB to -26.75dB with 1.25dB steps. This output can also be muted.

A matrix is implemented to feed audio to and from decoders VCR's and TV's.

Noise reduction system and de-emphasis can be inserted or by-passed through bus control.

Also all the audio outputs are tristate-type (high impedance mode is supported), allowing a simple parallel connections to the scarts (Twin tuner applications).

3 - Others

A 22kHz tone is generated for LNB control.

It is selectable by bus control and available on one of the two pins connected to the external video de-emphasis networks.

By means of the I^2C bus there is the possibility to drive the ICs into a low power consumption mode with active audio and video matrixes. Independantly from the main power mode, each individual audio and video output can be driven to high impedance mode.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC} V_{DD}	Supply Voltage	15 7.0	V V
P_{tot}	Total Power Dissipation	900	mW
T_{oper}	Operating Ambient Temperature	0, + 70	^{o}C
T_{stg}	Storage Temperature	-55, + 150	^{o}C

0042A-02.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
Rth(j-a)	Thermal Resistance Junction-ambient	60	^{o}C/W

0042A-03.TBL

DC AND AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 12V, V_{DD} = 5V, T_{amb} = 25^{o}C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC} V_{DD}	Sypply Voltage		11.4 4.75	12 5.0	12.6 5.25	V V
IQ_{CC} IQ_{DD}	Supply Current	All audio and all video outputs activated		55 8	70 15	mA mA
$IQLP_{CC}$ $IQLP_{DD}$	Supply Current at Low Power Mode	All audio and all video outputs are in high impedance mode		27 6	35 9	mA mA
AUDIO DEMODULATOR						
FMIN	FM Subcarrier Input Level (Pin FMIN for AGC action)	VCO locked on carrier at 6MHz 560kΩ load on AMPLOCK Pins 180kΩ load on DET Pins	5		500	mV_{PP}
DETH	Detector 1 and 2 (AMPLOCK Pins) (Threshold for activating Level Detector 2)	$8mV_{PP} \leq FMIN \leq 500mV_{PP}$ Carrier without modulation	2.90	3.10	3.30	V
VCOMI	VCO Mini Frequency	V_{CC} : 11.4 to 12.6V, T_{amb} : 0 to 70^{o}C			5	MHz
VCOMA	VCO Maxi Frequency		10			MHz
AP50	1kHz Audio Level at PLL output (DET Pins)	$0.5V_{PP}$ 50kHz dev. FM input, Coarse deviation set to 50kHz (Reg. 05 = 36_{HEX})	0.6	1	1.35	V_{PP}
APA50	1kHz Audio Level at PLL output (DET Pins)	$0.5V_{PP}$ 50kHz dev. FM input, Coarse and fine settings used	0.92	1	1.08	V_{PP}
FMBW	FM Demodulator Bandwidth	Gain at 12kHz versus 1kHz 180kΩ, 82kΩ 22pF on DET Pins	0	0.3	1	dB
DPCO	Digital Phase Comparator Output Current (CPUMP Pins)	Average sink and source current to external capacitor		60		µA
AUTOMATIC NOISE REDUCTION SYSTEM						
LRS	Output Level (Pin SUMOUT)	$1V_{PP}$ on left and right channel	0.9	1	1.1	V_{PP}
LDOR	Level Detector Output Resistance (Pins PK OUT)		4.0	5.4	6.8	kΩ
NDFT	Level Detector Fall Time Constant (Pins PK OUT)	External 22nF to GND and 1.2MΩ to V_{REF}		26.4		ms
NDLL	Bias Level (Pins PK OUT)	No audio in		2.40		V
LLCF	Noise Reduction Cut-off Frequency at Low Level Audio	$100mV_{PP}$ on DET Pins, External capacitor 330pF (FC Pins)		0.85		kHz
HLCF	Noise Reduction Cut-off Frequency at High Level Audio	$1V_{PP}$ on DET Pins, External capacitor 330pF (FC Pins)		7		kHz

0042A-04.TBL

DC AND AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 12V, V_{DD} = 5V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AUDIO OUTPUT (Pins VOL OUT R, VOL OUT L)						
DCOL	DC Output Level			4.8		V
AOLN	Audio Output Level with Reg 00 = 1A	FM input as for APA50 No de-emphasis, No pre-emphasis No noise reduction	1.5	1.9	2.34	V_{PP}
AOL50	Audio Output Level with Reg 00 = 1A	FM input as for APA50 50µs de-emphasis, 27kΩ//2.7nF load No pre-emphasis, No noise reduction	2.0	3.3	4.0	V_{PP}
AOL75	Audio Output Level with Reg 00 = 1A	FM input as for APA50 75µs de-emphasis, 27kΩ//2.7nF load No pre-emphasis, No noise reduction	2.0	3.3	4.0	V_{PP}
AMA1	Audio Output Attenuation with Mute-on. Reg 00 = 00.	$1V_{PP}$ - 1kHz from S2 RTN Pins	60	65		dB
MXAT	Max Attenuation before Mute. Reg 00 = 01.	1kHz, from S2 RTN Pins		32.75		dB
MXAG	Audio Gain. Reg 00 = 1F.	1kHz, from S2 RTN Pins	5	6	7	dB
ASTP	Attenuation of each of the 31 steps	1kHz		1.25		dB
THDA1	THD with Reg 00 = 1A	$1V_{PP}$ -1kHz from S2 RTN Pins		0.15		%
THDA2	THD with Reg 00 = 1A	$2V_{PP}$ -1kHz from S2 RTN Pins		0.3	1	%
THDFM	THD with Reg 00 = 1A	FM input as for APA50 75µs de-emphasis, ANRS ON		0.3	1	%
ACS	Audio Channel Separation	$1V_{PP}$ -1kHz on S2 RTN Pins	60	74		dB
ACSFM	Audio Channel Separation at 1kHz	- 0.5 V_{PP} - 50kHz deviation FM input on one channel - $0.5V_{PP}$ no deviation FM input on the other channel - Reg 05 = 36_{HEX} - 75µs de-emphasis, no ANRS		60		dB
SNFM	Signal to Noise Ratio	FM input as for APA50, 75µs de-emphasis, no ANRS, Unweighted		56		dB
SNFMNR	Signal to Noise Ratio	FM input as for APA50 75µs de-emphasis, ANRS ON, Unweighted		69		dB
$Z_{OUT\,L}$ $Z_{OUT\,H}$	Audio Output Impedance	Low impedance mode High impedance mode	 30	18 44	 55	Ω kΩ
AUXILIARY AUDIO OUTPUT (Pins S2 OUT R, S2 OUT L)						
DCOLAO	DC output level	Aux. input pins open circuit		4.8		V
AOLNS	Audio Output Level on S2	FM input as for APA50 No de-emphasis, No pre-emphasis No noise reduction	1.55	2	2.42	V_{PP}
AOL50S	Audio Output Level on S2	FM input as for APA50 50µs de-emphasis, 27kΩ//2.7nF load No pre-emphasis, No noise reduction	2.0	3.4	4.0	V_{PP}
AOL75S	Audio Output Level on S2	FM input as for APA50 75µs de-emphasis, 27kΩ//2.7nF load No pre-emphasis, No noise reduction	2.0	3.4	4.0	V_{PP}
THDAOFM	THD on S2	FM input as for APA50 75µs de-emphasis, no ANRS		0.3	1	%
$Z_{OUT\,L}$ $Z_{OUT\,H}$	Audio Output Impedance	Low impedance mode High impedance mode	 30	60 44	100 55	Ω kΩ

0042A-05.TBL

DC AND AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 12V, V_{DD} = 5V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
RESET						
RTCCU	End of Reset Threshold for V_{CC}	V_{DD} = 5V, V_{CC} going up		8.7		V
RTCCD	Start of Reset Threshold for V_{CC}	V_{DD} = 5V, V_{CC} going down		7.9		V
RTDDU	End of Reset Threshold for V_{DD}	V_{CC} = 12V, V_{DD} going up		3.8		V
RTDDD	Start of Reset Threshold for V_{DD}	V_{CC} = 12V, V_{DD} going down		3.5		V
COMPOSITE SIGNAL PROCESSING						
VIDC	VID IN	External load current < 1µA	2.25	2.45	2.65	V
ZVI	VID IN Input Impedance		7	11	14	kΩ
DEODC	DC Output Level (Pins VIDEEM)		2.25	2.45	2.65	V
DEOMX	Max AC Level before Clipping (Pins VIDEEM)	GV = 0dB, Reg 01 = 00	2			V_{PP}
DGV	Gain error vs GV @ 100kHz	GV = 0 to 12.7dB, Reg 01 = 00 → 3F	-0.5	0	0.5	dB
INVG	Inverter Gain		-0.9	-1	-1.1	
VISOG	Video Input to SCART Output Gain	De-emphasis amplifier mounted in unity gain, Normal video selected	-1	0	1	dB
DEBW	Bandwidth for $1V_{PP}$ input measured on Pins VIDEEM	@ - 3dB with GV = 0dB, Reg 01 = 00	10			MHz
DFG	Differential Gain on Sync Pulses measured on Pins VIDEEM	GV = 0dB, $1V_{PP}$ CVBS + $0.5V_{PP}$ 25Hz sawtooth (input : VID IN)			1	%
ITMOD	Intermodulation of FM subcarriers with chroma subcarrier	7.02 and 7.2MHz sub-carriers, 12.2dB lower than chroma		-60		dB
CLAMP STAGES (Pins CLAMP IN, S2)						
ISKC	Clamp Input Sink Current	V_{IN} = 3V	0.5	1	1.5	µA
ISCC	Clamp Input Source Current	V_{IN} = 2V	40	50	60	µA
VIDEO MATRIX						
XTK	Output Level on any Output when $1V_{PP}$ CVBS input is selected for any other output	@ 5MHz		-60		dB
BFG	Output Buffer Gain (Pins S1 VID OUT, S2 VID OUT)	@ 100kHz	1.87	2	2.13	
DCOLVH	DC Output Level	High impedance mode		0	0.2	V
$Z_{OUT\ HV}$	Video Output Impedance	High impedance mode	16	23	30	kΩ
VCL	Sync Tip Level on Selected Outputs (Pins S1 VID OUT, S2 VID OUT)	$1V_{PP}$ CVBS through 10nF on input	1.05	1.3	1.55	V

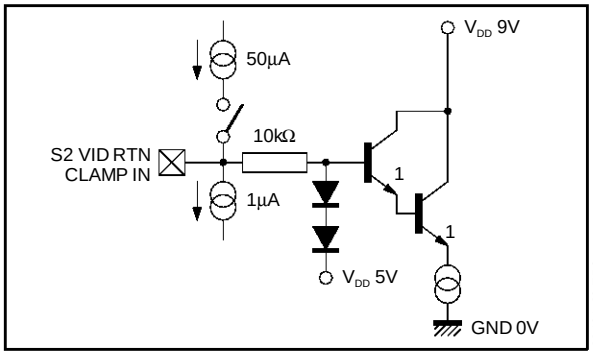
0042A-06.TBL

PIN INTERNAL CIRCUITRY

S2 VID RTN, CLAMP IN

50µA source is active only when VIDIN < 2.7V.

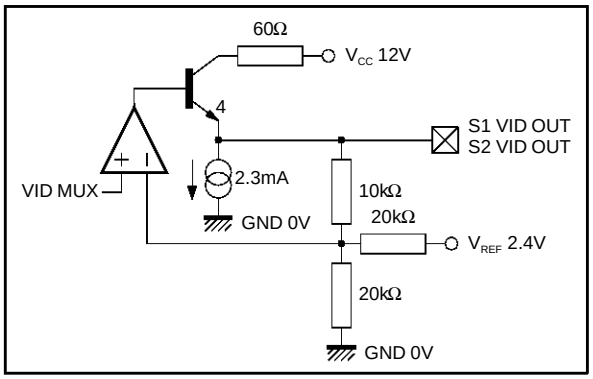
Figure 1



S1 VID OUT, S2 VID OUT

Same as above but with no black level adjustment.

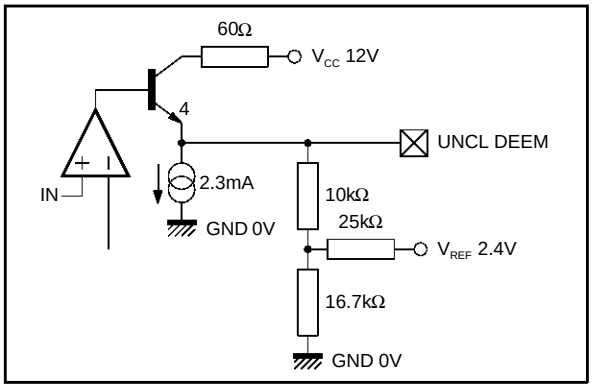
Figure 3



UNCL DEEM

Same as above but with no black level adjustment and slightly different gain.

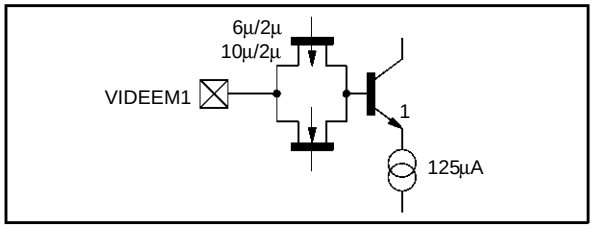
Figure 4



VIDEEM1

Ron of the transistor gate is ≈10kΩ.

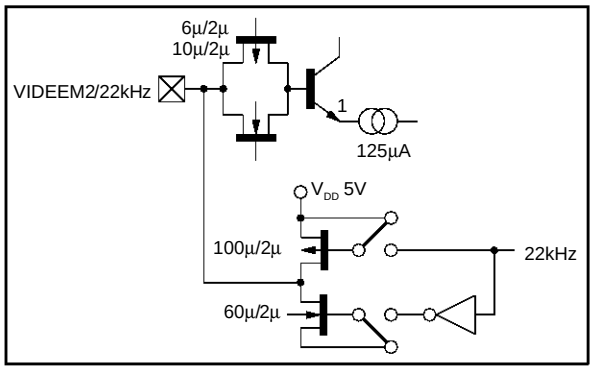
Figure 5



VIDEEM2 / 22kHz

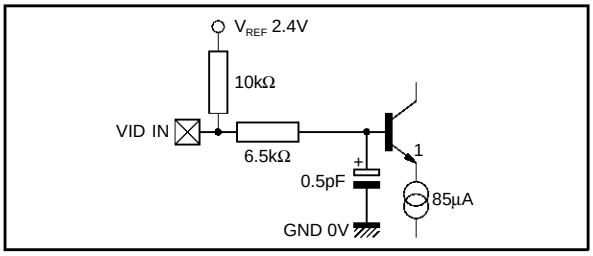
Ron of the transistor gate is ≈10kΩ.

Figure 6



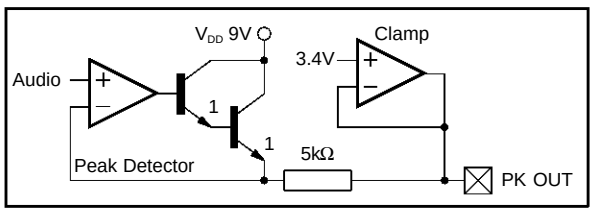
VID IN

Figure 7



PK OUT

Figure 8

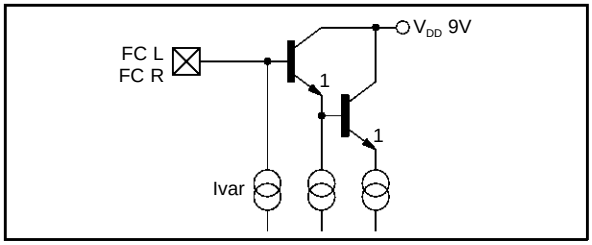


PIN INTERNAL CIRCUITRY (continued)

FC L, FC R

Ivar is controlled by the peak det audio level max. ±15µA (1V_{PP} audio).

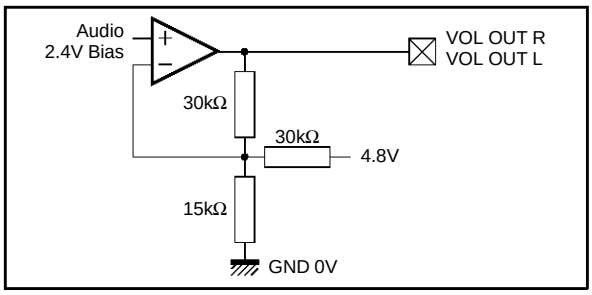
Figure 9



VOL OUT R, VOL OUT L

Audio output with volume and scart driver with +12dB of gain for up to 2V_{RMS}. The opamp has a push-pull output stage.

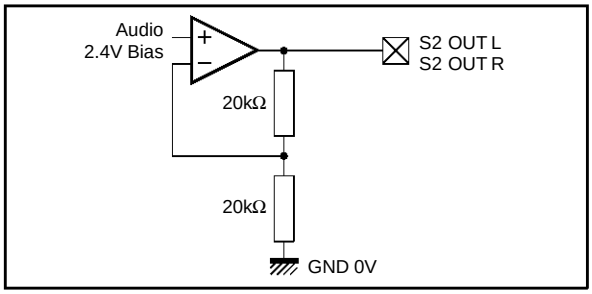
Figure 10



S2 OUT L, S2 OUT R

Same as above but with gain fixed at +6dB.

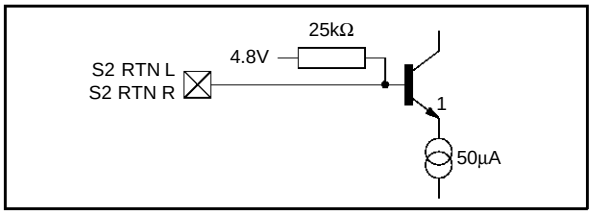
Figure 11



S2 RTN L, S2 RTN R

4.8V bias voltage is the same as the bias level on the audio outputs.

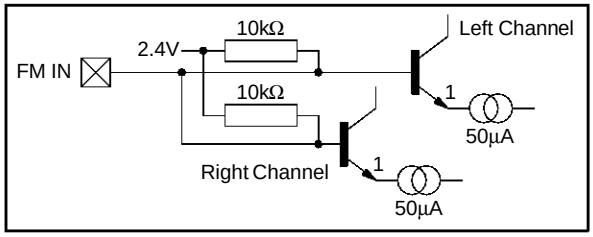
Figure 12



FM IN

The other input for each channel is internally biased in the same way via 10kΩ to the 2.4V V_{REF}.

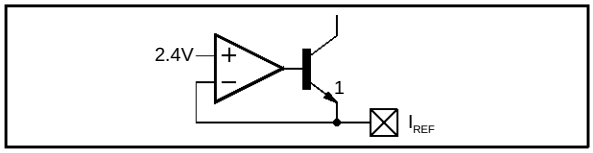
Figure 13



I_{REF}

The optimum value if I_{REF} is 50µA ±2% so an external resistor of 47.5kΩ ±1% is required.

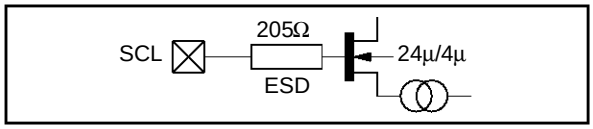
Figure 14



SCL

This is the input to a Schmitt input buffer made with a CMOS amplifier.

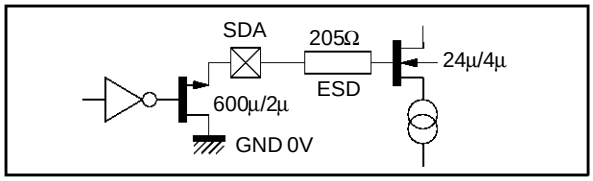
Figure 15



SDA

Input same as above. Output pull down only : relies on external resistor for pull-up.

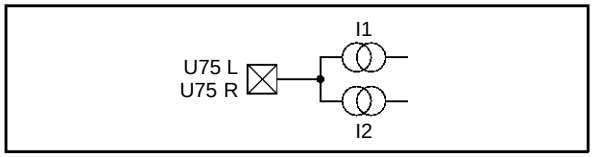
Figure 16



U75 L, U75 R

I1 - I2 = 2 x audio / 18kΩ. eg 1V_{PP} audio : ±55µA. The are internal switches to match the audio level of the different standards.

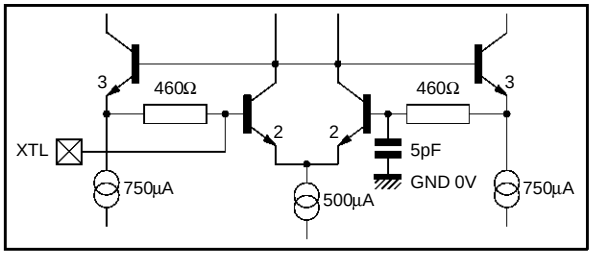
Figure 17



PIN INTERNAL CIRCUITRY (continued)

XTL

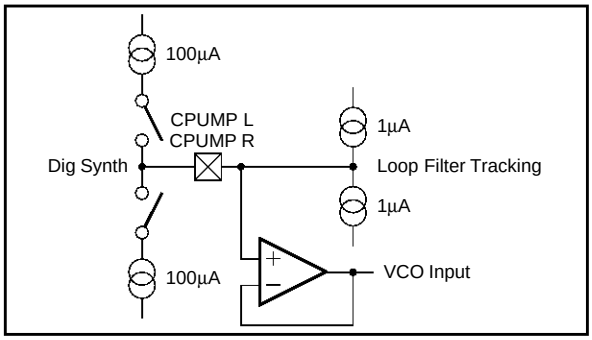
Figure 18



CPUMP L, CPUMP R

An offset on the PLL loop filter will cause an offset in the two 1µA currents that will prevent the PLL from drifting-off frequency.

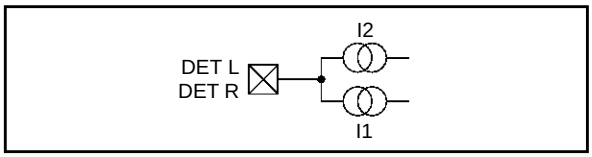
Figure 19



DET L, DET R

I2 - I1 = f (phase error).

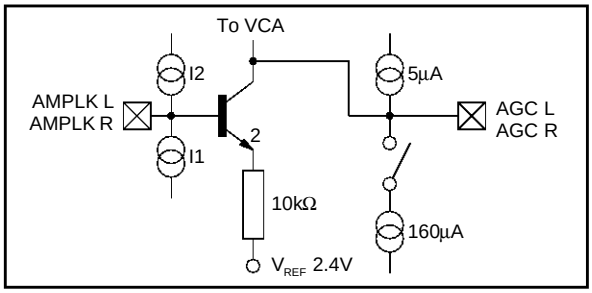
Figure 20



AMPLK L, AMPLK R, AGC L, AGC R

I2 and I1 from the amplitude detecting mixer.

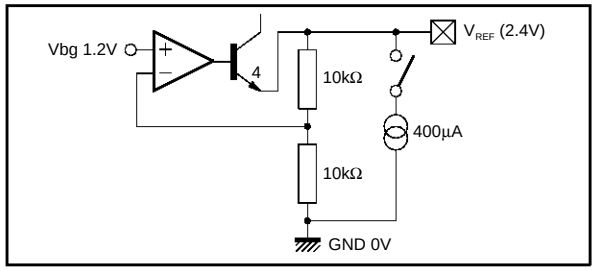
Figure 21



V_{REF}

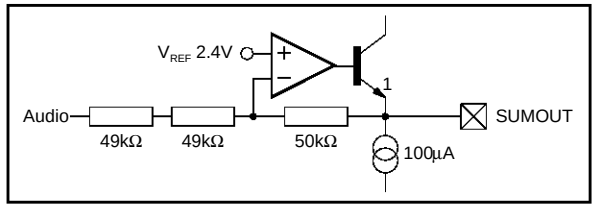
The 400µA source is off during stand-by mode.

Figure 22



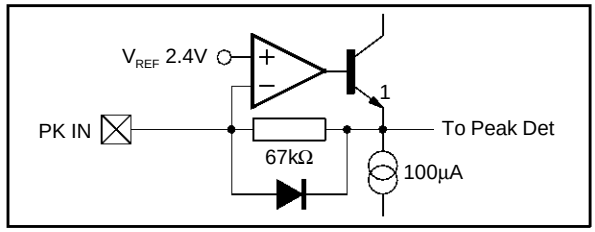
SUMOUT

Figure 23



PK IN

Figure 24



V 12V

Doubled bonded (two bond wires and two pads for one package pin) :

- One pad is connected to all of the 12V ESD and video guard rings.
- The second pad is connected to power up the video block.

V GND

Doubled bonded :

- One pad is connected to power-up all of the video mux and I/O.
- The second pad is only as a low noise GND for the video input.

V_{DD} 5V, GND 5V

Connected to XTL oscillator and the bulk of the CMOS logic and 5V ESD.

PIN INTERNAL CIRCUITRY (continued)

A GND L

Doubled bonded :

- One pad connected to the left VCO, dividers, mixers and guard ring. the guard connection is star connected directly to the pad.
- The second pad is connected to both AGC amps and the deemphasis amplifiers, frequency synthesis and FM deviation selection circuit for both channels.

A 12V

Doubled bonded :

- One pad connected to the ESD and guard ring.
- The second pad is connected to the main power for all of the audio parts.

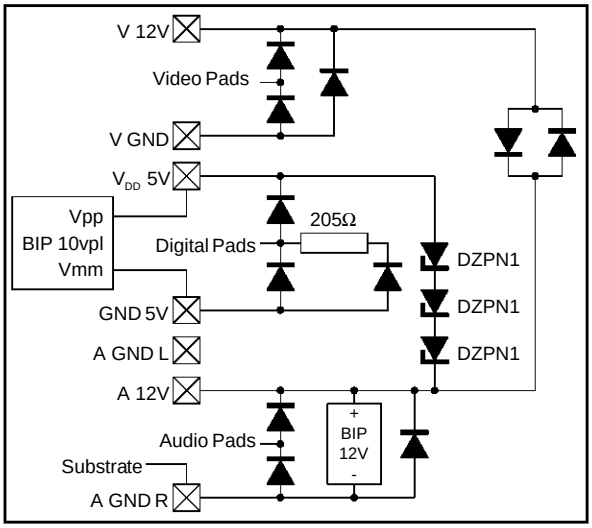
A GND R

Boubled bonded :

- One pad connected to the right VCO, dividers, mixers and guard ring. The guard connection is star connected directly to the pad.
- The second pad is connected to the bias block, audio noise reduction, volume, mux and ESD.

A third bond wire on this pin is connected directly to the die pad (substrate).

Figure 25



I²C PROTOCOL

1) WRITING to the chip

S-Start Condition

P-Stop Condition

CHIP ADDR - 7 bits. 06H

W-Write/Read bit is the 8th bit of the chip address.

A-ACKNOWLEDGE after receiving 8 bits of data/adress.

REG ADDR	Address of register to be written to, 8 bits of which bits 3, 4, 5, 6 & 7 are 'X' or don't care ie *only the first 3 bits are used*.
DATA	8 bits of data being written to the register. All 8 bits must be written to at the same time.
REG ADDR/A/DATA/A	can be repeated, the write process can continue untill terminated with a STOP condition. If the **REG ADDR** is higher than 07 then IIC PROTOCOL will still be met (ie an **A** generated).

Example :

S	06	W	A	00	A	55	A	01	A	8F	// //	A	P

2) READING from the chip

When reading, there is an auto-incrementfeature. This means any read command always starts by reading Reg 8 and will continue to read the following registers in order after each acknowledge or until there is no acknowledge or a stop. This function is cyclic that is it will read the same set of registers without re-addressing the chip. There are two modes of operation as set by writing to bit 7 of register 0. Read 3 registers in a cyclic fashion or all 5 registers in a cyclic fashion. Note only the last 5 of the 11 registers can be read.

Reg0 bit 7 = L ⇒ Start / chip add / R / A / Reg 8 / A/ Reg 9 / A / Reg 0A / A/ Reg 8 / A / Reg 9 / A / Reg 0A /... / P /

Reg0 bit 7 = H ⇒ Start / chip add / R / A / Reg 8 / A/ Reg 9 / A / Reg 0A / A / Reg 7 / A/ Reg 6 / A / Reg 8 / A/ Reg 9 / A / Reg 0A / A / Reg 7 / A / Reg 6 / ... / P /

CONTROL REGISTERS

Reg 0 write only

Bit (default 00_{HEX})

0 L Select 5 bits audio volume control 00H = MUTE
1 L Select 5 bits audio volume control 01H = -26.75dB
2 L Select 5 bits audio volume control : : : : :
3 L Select 5 bits audio volume control 1.25dB steps up to
4 L Select 5 bits audio volume control 1FH = +12dB
5 L Not to be used
6 L Audio mux switch K3 - ANRS select (L = no ANRS, H = ANRS)
7 L L = read 3 registers, H = read 5 registers

Reg 1 write only

Bit (default 00_{HEX})

0 L Select video gain bits
1 L Select video gain bits 00H = 0dB
2 L Select video gain bits 01H = +0.202dB
3 L Select video gain bits 02H = +0.404dB
4 L Select video gain bits n = + 0.202 dB * n
5 L Select video gain bits 3FH = + 12.73 dB
6 L Selected video invert (H = inverted, L = non inverted)
7 L Video deemphasis 1 / Video deemphasis 2 (L : V_{ID} De-em 1)

CONTROL REGISTERS (continued)

Reg 2 write only

Bit (default $F7_{HEX}$)
0 H Select video source for scart 1 O/P
1 H Select video source for scart 1 O/P
2 H Select video source for scart 1 O/P
3 L Select 4.000MHz or 8.000MHz clock speed (L = 8MHz)
4 H Select audio source for volume output (Switch K1)
5 H Select audio source for volume output (Switch K1)
6 H Select Left/Right/Stereo for volume output
7 H Select Left/Right/Stereo for volume output

Reg 3 write only

Bit (default $F7_{HEX}$)
0 H Select video source for scart 2 O/P
1 H Select video source for scart 2 O/P
2 H Select video source for scart 2 O/P
3 L Video deemphais 2 / 22kHz (H : 22kHz)
4 H Select audio source for Scart 2 output (Switch K5)
5 H Select audio source for Scart 2 output (Switch K5)
6 H Audio deemphasis select (Switch K2)
7 H Audio deemphasis select (Switch K2)

Reg 4 write only

Bit (default BF_{HEX})
0 H Not to be used
1 H Not to be used
2 H Not to be used
3 H Stand-by or low power mode (H = low power)
4 H Not to be used
5 H Not to be used
6 L Not to be used
7 H Not to be used

Reg 5 write only

Bit (default $B5_{HEX}$)
0 H FM deviation selection -- default value for 50kHz modulation
1 L FM deviation selection
2 H FM deviation selection
3 L FM deviation selection
4 H FM deviation selection
5 H FM deviation selection (L = double the FM deviation)
6 L Not to be used
7 H Not to be used

Reg 6 write/read

Bit (default 86_{HEX})
0 L Status of I/O
1 H Select data direction of I/O 1 (H = output)
2 H Select frequency synthesizer 1 OFF/ON (L = OFF)
3 L Select frequency synthesizer 2 OFF/ON (L = OFF)
4 L Select RF source (L = OFF) to FM det 1
5 L Select RF source (L = OFF) to FM det 2
6 L Select frequency for PLL synthesizer - LSB (bit 0) of 10-bit value
7 H Select frequency for PLL synthesizer - bit 1 of 10-bit value

CONTROL REGISTERS (continued)

Reg 7 write/read

Bit (default AF_{HEX})

0 H Select frequency for PLL synthesizer - bit 2 of 10-bit value
1 H Select frequency for PLL synthesizer
2 H Select frequency for PLL synthesizer
3 H Select frequency for PLL synthesizer
4 L Select frequency for PLL synthesizer
5 H Select frequency for PLL synthesizer
6 L Select frequency for PLL synthesizer
7 H Select frequency for PLL synthesizer - bit 9, MSB (10th bit) of 10-bit value

Reg 8 read only

Bit

0 Subcarrier detection (DET 1) (L = No subcarrier)
1 Not used
2 Read frequency of watchdog 1 - LSB (bit 0) of 10-bit value
3 Read frequency of watchdog 1 - bit 1 of 10-bit value
4 Subcarrier detection (DET 2) (L = No subcarrier)
5 Not used
6 Read frequency of watchdog 2 - bit 0 of 10-bit value
7 Read frequency of watchdog 2 - bit 1 of 10-bit value

Reg 9 read only

Bit (default AF_{HEX})

0 Read frequency of watchdog 1 - bit 2 of 10-bit value
1 Read frequency of watchdog 1
2 Read frequency of watchdog 1
3 Read frequency of watchdog 1
4 Read frequency of watchdog 1
5 Read frequency of watchdog 1
6 Read frequency of watchdog 1
7 Read frequency of watchdog 1 - bit 9, MSB (10th bit) of 10-bit

Reg 0A read only

Bit

0 Read frequency of watchdog 2 - bit 2 of 10-bit value
1 Read frequency of watchdog 2
2 Read frequency of watchdog 2
3 Read frequency of watchdog 2
4 Read frequency of watchdog 2
5 Read frequency of watchdog 2
6 Read frequency of watchdog 2
7 Read frequency of watchdog 2 - bit 9, MSB (10th bit) of 10-bit

CONTROL REGISTERS (continued)

Video Mux Truth Tables

Register 2 <0:2> ⇒ Scart 1 video output control
Register 3 <0:2> ⇒ Scart 2 video output control

The truth table for the three scart outputs are the same.

Register 2/3			Video Output
Bit<2>	Bit<1>	Bit<0>	
0	0	0	Baseband video
0	0	1	De-emphasized video
0	1	0	Normal video
0	1	1	Not to be used
1	0	0	Scart 2 return
1	0	1	Not to be used
1	1	0	Nothing selected
1	1	1	High Z or low power (default)

Audio Mux Truth Tables

Register 2			Switch K1/Audio Source Selection for Volume Output
Bit <5>	Bit <4>		**Volume Output**
0	0	A	Audio deemphasis (K2 switch O/P)
1	0	C	Scart 2 return
0	1	B	Not to be used
1	1	-	High Z or low power (default)

Register 3			Switch K2/Audio Deemphasis
Bit <7>	Bit <6>		**Audio Deemphasis**
0	0	A	No deemphasis
1	0	C	Not to be used
0	1	B	50µs
1	1	B	75µs (default)

Register 0			Switch K3 & K4
Bit <6>	Bit <5>		**ANRS I/O Select**
0	X	A	Noise reduction OFF
1	X	B	Noise reduction ON (default)
X	0	A	Not to be used
X	1	B	Not to be used

Register 3			Switch K5/Audio Source Selection for Scart 2
Bit <5>	Bit <4>		**Aux Audio Output**
0	0	C	PLL output
1	0	A	Not to be used
0	1	B	Audio deemphasis (K2 switch O/P)
1	1	-	High Z or low power state (default)

Register 2		Left / Right / Stereo on Volume Output
Bit <7>	Bit <6>	
0	0	Mono left / channel 1
1	0	Mono right / channel 2
1	1	Stereo left & right (default)

CONTROL REGISTERS (continued)

Register 5 : FM Deviation Selection

4	3	2	1	0	Selected Nominal Carrier Modulation	
					Bit 5 = 0	**Bit 5 = 1**
0	0	0	0	0	Do not use	cal : do not use = 0.3373V offset on VCO
0	0	0	0	1	Do not use	cal : do not use = 0.3053V offset on VCO
0	0	0	1	0	Do not use	cal : do not use = 0.2763V offset on VCO
0	**0**	**0**	**1**	**1**	Cal. set. (2V)	**calibration setting (1V offset on VCO)**
0	0	1	0	0	592kHz	296kHz modulation
0	0	1	0	1	534kHz	267kHz modulation
0	0	1	1	0	484kHz	242kHz
0	0	1	1	1	436kHz	218kHz
0	1	0	0	0	396kHz	198kHz
0	1	0	0	1	358kHz	179kHz
0	1	0	1	0	322kHz	161kHz
0	1	0	1	1	292kHz	146kHz
0	1	1	0	0	266kHz	133kHz
0	1	1	0	1	240kHz	120kHz
0	1	1	1	0	218kHz	109kHz
0	1	1	1	1	196kHz	98.3kHz
1	0	0	0	0	179kHz	89.7kHz
1	0	0	0	1	161kHz	80.9kHz
1	0	0	1	0	146kHz	73.1kHz
1	0	0	1	1	122kHz	66.0kHz
1	0	1	0	0	120kHz	60.0kHz
1	**0**	**1**	**0**	**1**	109kHz	**54.4kHz = default power up state**
1	0	1	1	0	98kHz	49.1kHz
1	0	1	1	1	89kHz	44.3kHz
1	1	0	0	0	78kHz	39.8kHz
1	1	0	0	1	71kHz	35.9kHz
1	1	0	1	0	65kHz	32.4kHz
1	1	0	1	1	58kHz	29.1kHz
1	1	1	0	0	53kHz	26.7kHz
1	1	1	0	1	48.6kHz	24.3kHz
1	1	1	1	0	43.8kHz	21.9kHz
1	1	1	1	1	39.6kHz	19.7kHz

Example : Default power up state 54.4kHz $\Rightarrow$ ±54.4kHz.

Register 1 Bit <7>	Register 3 Bit <3>	Video Deemphasis/22kHz
0	0	Deemphasis 1 (default)
0	1	Deemphasis 1 + 22kHz (Pin 13)
1	0	Deemphasis 2
1	1	Deemphasis 2

FM DEMODULATION SOFTWARE ROUTINE

With the STV0042A circuit, for each channel, three steps are required to acheive a FM demodulation :

- 1st step : To set the demodulation parameters :
  - FM deviation selection,
  - Subcarrier frequency selection.
- 2nd step : To implement a waiting loop to check the actual VCO frequency.
- 3rd step : To close the demodulation phase locked loop (PLL).

Refering to the FM demodulation block diagram (page 12), the frequency synthesis block is common to both channels (left and right) ; consequently two complete sequences have to be done one after the other when demodulating stereo pairs.

Detailed Description

Conventions :

- R = Stands for Register
- B = Stands for Bit

Example : R05 B2 = Register 05, Bit 2

For clarity, the explanations are based on the following example : stereo pair 7.02MHz/L 7.20MHz/R, deviation ±50kHz max.

FM DEMODULATION SOFTWARE ROUTINE (continued)

1st Step (Left) : Setting the Demodulation Parameters

A. The FM deviation is selected by loading R5 with the appropriate value. (see R5 truth table).
NB : Very wide deviations (up to ±592kHz) can be accomodated when R5 B5 is low.

Corresponding bandwidth can be calculated as follows :
Bw ≈ 2 (FM deviation + audio bandwidth)
Bw ≈ 2 (value given in table + audio bandwidth)
In the example :

R5 Bits	7	6	5	4	3	2	1	0
	X	X	1	1	0	1	1	0

B. The subcarrier frequency is selected by launching a frequency synthesis (the VCO is driven to the wanted frequency). This operation requires two actions :
- To connect the VCO to the frequency synthesis loop. Refering to the FM block diagram (page 12):
  - SW4 closed ⇒ R6 B2 = H
  - SW3 to bias ⇒ R6 B4 = L
  - SW2 to bias ⇒ R6 B3 = L
  - SW1 opened ⇒ R6 B5 = L
- To load R7 and R6 B6 B7 with the value corresponding to the left channel frequency. This 10 bits value is calculated as follows :
  Subcarrier frequency = coded value x 10kHz
  (10kHz is the minimum step of the frequency synthesis function) . Considering that the tunning range is comprised between 5 to 10MHz, the coded value is a number between 500 and 1000 (2^{10} = 1024) then 10 bits are required.
  Example :
  7.02MHz = 702 x 10kHz
  702 ⇒ 1010 1111 10 ⇒ AF + 10
  R7 is loaded with AF and R6 B6 : L, R6 B7 : H.

The Table 1 gives the setting for the most common subcarrier frequencies.

2nd Step (Left) : *VCO Frequency Checking (VCO)*

This second step is actually a waiting loop in which the actual running frequency of the VCO is measured.
To exit of this loop is allowed when : Subcarrier Frequency - 10kHz ≤ Measured Frequency ≤ Subcarrier Frequency +10kHz (± 10kHz is the maximum dispersion of the frequency synthesis function).
In practice, R8 B2 B3 and R9 are read and compared to the value loaded in R6 B6 B7 and R7 ±1 bit.

Note :
The duration of this step depends on how large is frequency difference between the start frequency and the targeted frequency. Typically :
- the rate of change of the VCO frequency is about 3.75MHz/s (C_{pump} = 10µF)
- In addition to this settling time, 100ms must be added to take into account the sampling period of the watchdog.

3rd Step (Left)

The FM demodulation can be started by connecting the VCO to the phase locked loop (PLL).
In practice :
- SW3 closed ⇒ R6 B4 = H
- SW4 opened ⇒ R6 B2 = L

After this sequence of 3 steps for left channel, a similar sequence is needed for the right channel.

Note :
In the sequence for the right, there is no need to again select the FM deviation (once is enough for the pair).

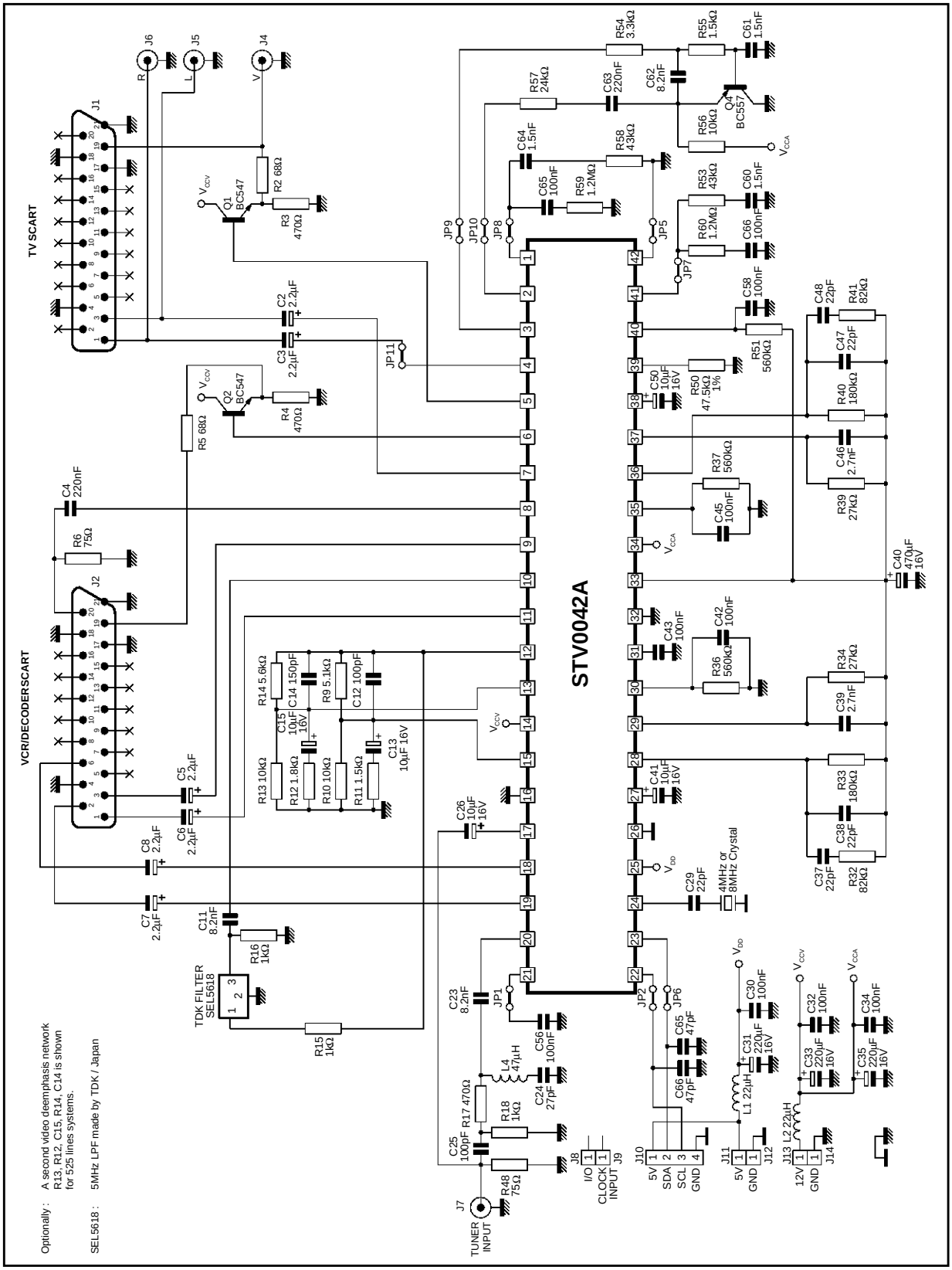
General Remark
Before to enable the demodulated signal to the audio output, it is recommanded to keep the muting and to check whether a subcarrier is present at the wanted frequency. Such an information is available in R8 B0 and R8 B4 which can be read.

Two different strategies can be adopted when enabling the output :
- Either both left and right demodulated signals are simultaneously authorized when both channel are ready.
- Or while the right channel sequence is running, the already ready left signal is sent to the left and right outputs and the real stereo sound L/R is output when both channels are ready. This second option gives sound a few hundreds of ms before the first one.

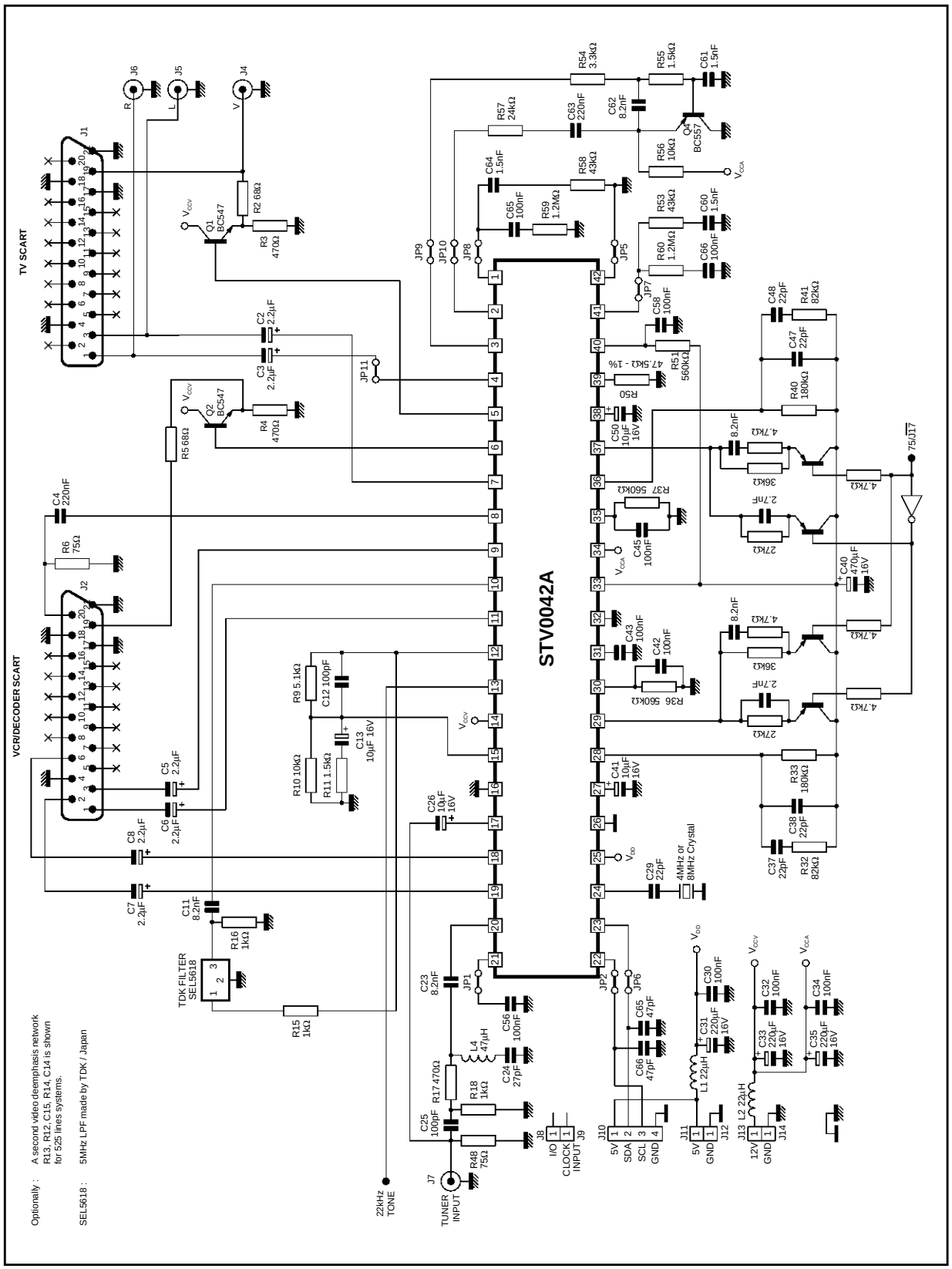
Table 1 : Frequency Synthesis Register Setting for the Most Common Subcarrier Frequencies

Subcarrier Freq. (MHz)	Register 7 (Hex)	Register 6	
		Bit 7	Bit 6
5.58	8B	1	0
5.76	90	0	0
5.8	91	0	0
5.94	94	1	0
6.2	9B	0	0
6.3	9D	1	0
6.4	A0	0	0
6.48	A2	0	0
6.5	A2	1	0
6.6	A5	0	0
6.65	A6	0	1
6.8	AA	0	0
6.85	AB	0	1
7.02	AF	1	0
7.20	B4	0	0
7.25	B5	0	1
7.38	B8	1	0
7.56	BD	0	0
7.74	C1	1	0
7.85	C4	0	1
7.92	C6	0	0
8.2	CD	0	0
8.65	D8	0	1

TYPICAL APPLICATION (with 2 video deemphasis network)

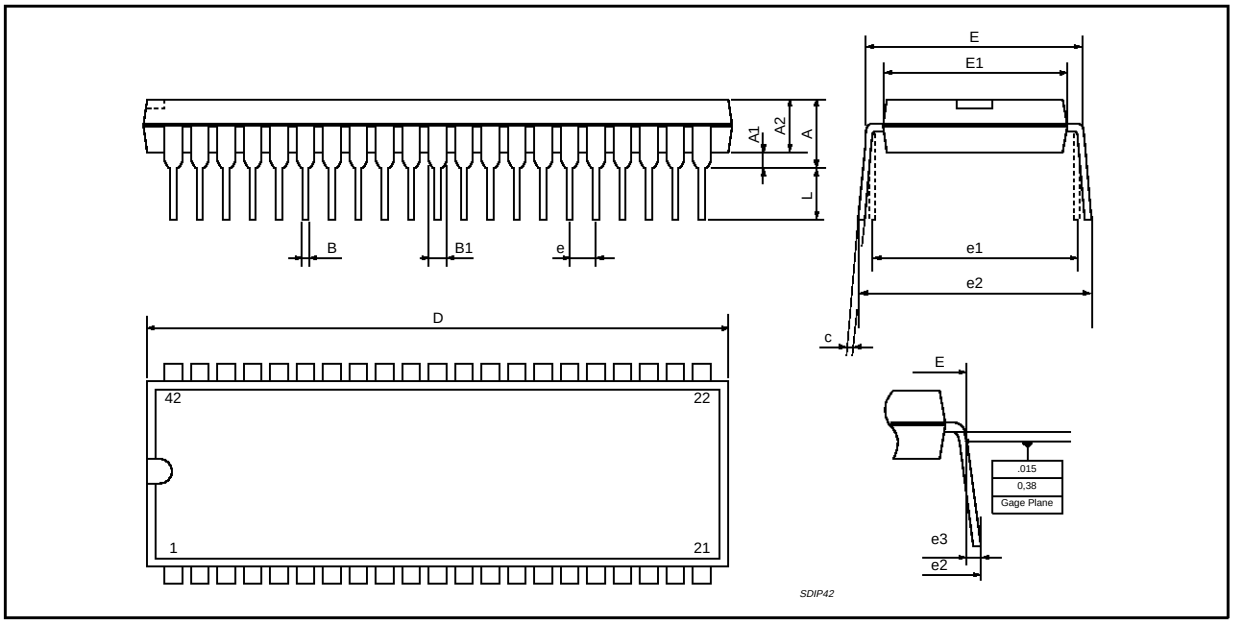


TYPICAL APPLICATION (with 22kHz tone and three audio de-emphasis 50µs, 75µs, J17)



PACKAGE MECHANICAL DATA

42 PINS - PLASTIC SHRINK DIP



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.200
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.120	0.150	0.180
B	0.38	0.46	0.56	0.0149	0.0181	0.0220
B1	0.89	1.02	1.14	0.035	0.040	0.045
c	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	36.58	36.83	37.08	1.440	1.450	1.460
E	15.24		16.00	0.60		0.629
E1	12.70	13.72	14.48	0.50	0.540	0.570
e		1.778			0.070	
e1		15.24			0.60	
e2			18.54			0.730
e3			1.52			0.060
L	2.54	3.30	3.56	0.10	0.130	0.140

SDIP42.TBL