



New Product

**SUD50P04-13L**  
Vishay Siliconix

**P-Channel 40-V (D-S), 175 °C MOSFET**

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
-40	0.013 @ V <sub>GS</sub> = -10 V	-60°
	0.022 @ V <sub>GS</sub> = -4.5 V	-48

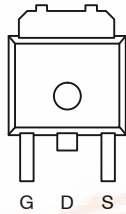
**FEATURES**

- TrenchFET® Power MOSFET
- 175 °C Maximum Junction Temperature

**APPLICATIONS**

- Automotive Such As:
  - High-Side Switch
  - Motor Drive
  - 12-V Boardnet

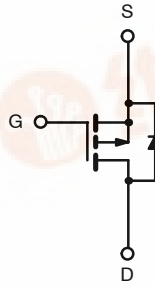
TO-252



Top View

Order Number:  
SUD50P04-13L—E3

Drain Connected to Tab



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V <sub>DS</sub>	-40	V
Gate-Source Voltage		V <sub>GS</sub>	± 20	
Continuous Drain Current <sup>b</sup>	T <sub>C</sub> = 25 °C	I <sub>D</sub>	-60°	A
	T <sub>C</sub> = 100 °C		-43	
Pulsed Drain Current		I <sub>DM</sub>	-100	
Continuous Source Current (Diode Conduction)		I <sub>S</sub>	-60°	
Avalanche Current		I <sub>AS</sub>	-40	
Avalanche Energy		E <sub>AS</sub>	80	mJ
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	P <sub>D</sub>	93.7 <sup>b</sup>	W
	T <sub>A</sub> = 25 °C		3 <sup>a</sup>	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	t ≤ 10 sec.	R <sub>thJA</sub>	15	18	°C/W
	Steady State		40	50	
Maximum Junction-to-Case		R <sub>thJC</sub>	1.3	1.6	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. See SOA curve for voltage derating.
- c. Calculated based on maximum allowable Junction Temperature. Package limitation current is 50 A.

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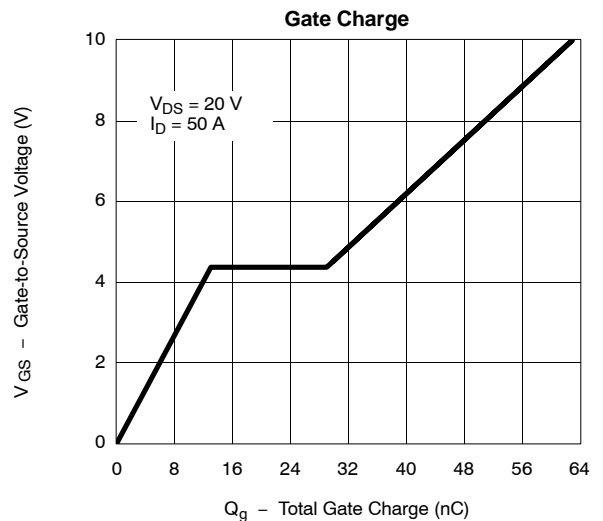
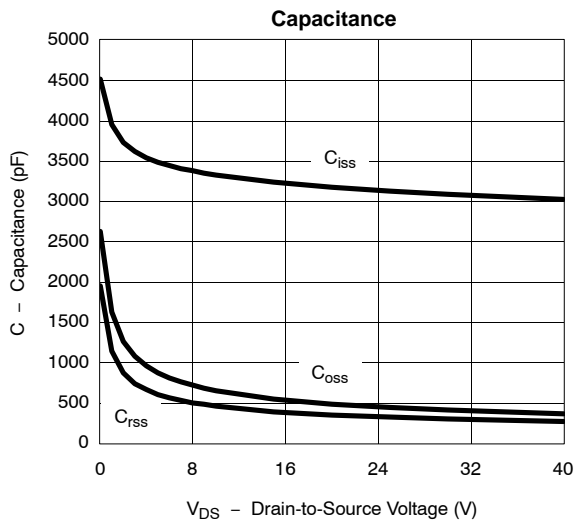
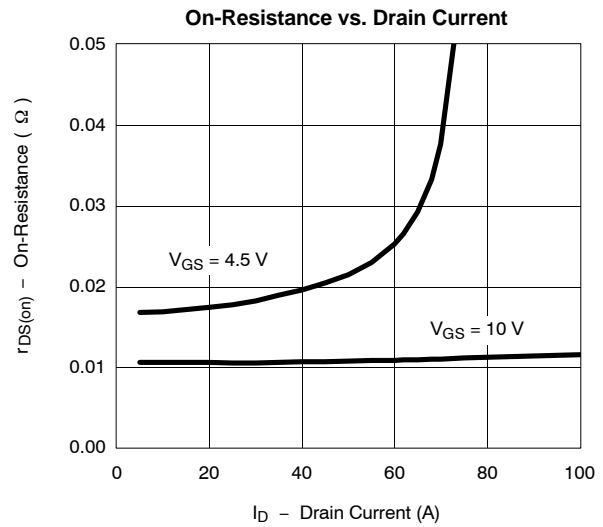
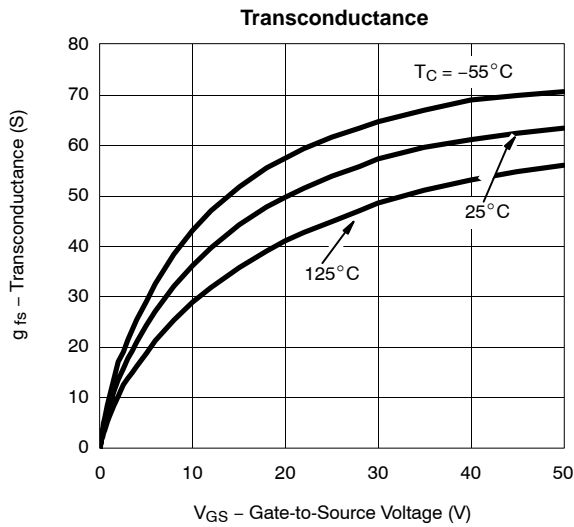
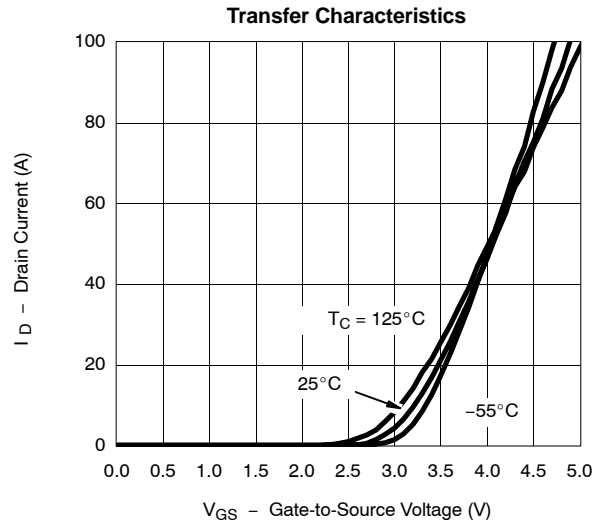
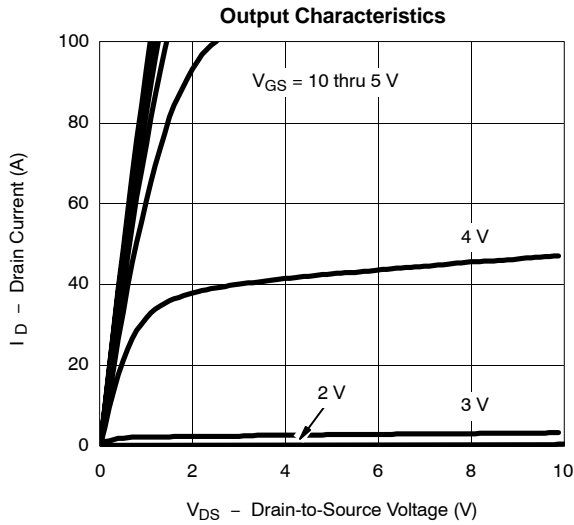
SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-40			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-1.0		-3.0	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -40 V, V <sub>GS</sub> = 0 V			-1	μA
		V <sub>DS</sub> = -40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			-50	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = -5 V, V <sub>GS</sub> = -10 V	-50			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -30 A		0.0105	0.013	Ω
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -30 A, T <sub>J</sub> = 125 °C			0.020	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -20 A		0.017	0.022	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -30 A	15			S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -25 V, f = 1 MHz		3120		pF
Output Capacitance	C <sub>oss</sub>			440		
Reverse Transfer Capacitance	C <sub>rss</sub>			320		
Gate Resistance	R <sub>g</sub>	f = 1.0 MHz		4.3		Ω
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = -20 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -50 A		63	95	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			13		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			16		
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = -20 V, R <sub>L</sub> = 0.4 Ω I <sub>D</sub> ≅ -50 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 2.5 Ω		15	25	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			18	30	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			60	90	
Fall Time <sup>c</sup>	t <sub>f</sub>			47	70	
<b>Source-Drain Diode Ratings and Characteristic (T<sub>C</sub> = 25 °C)</b>						
Pulsed Current	I <sub>SM</sub>				-100	A
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = -50 A, V <sub>GS</sub> = 0 V		-1.0	-1.5	V
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -50 A, di/dt = 100 A/μs		36	55	ns

**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

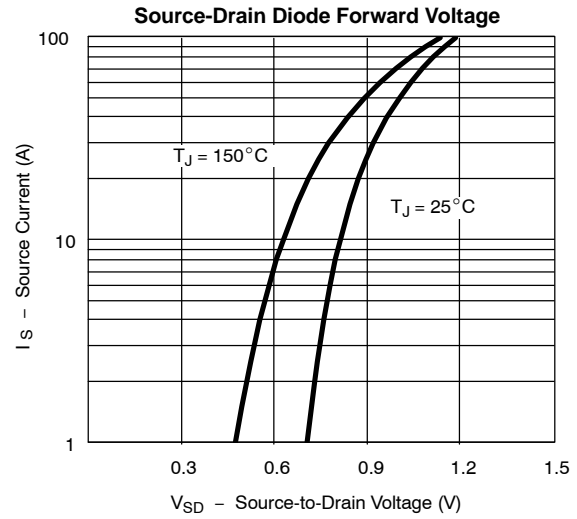
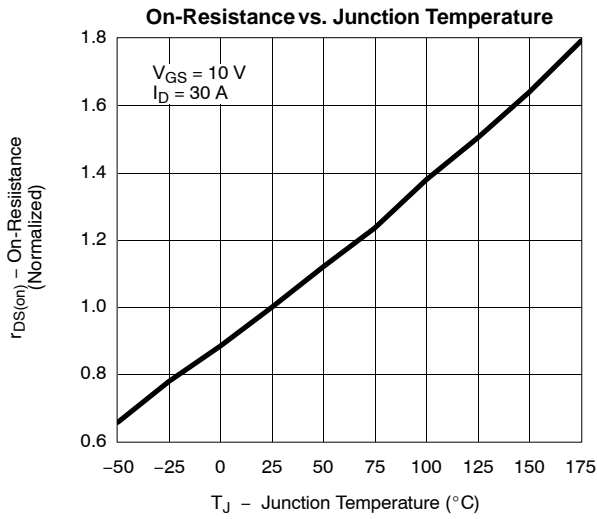


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

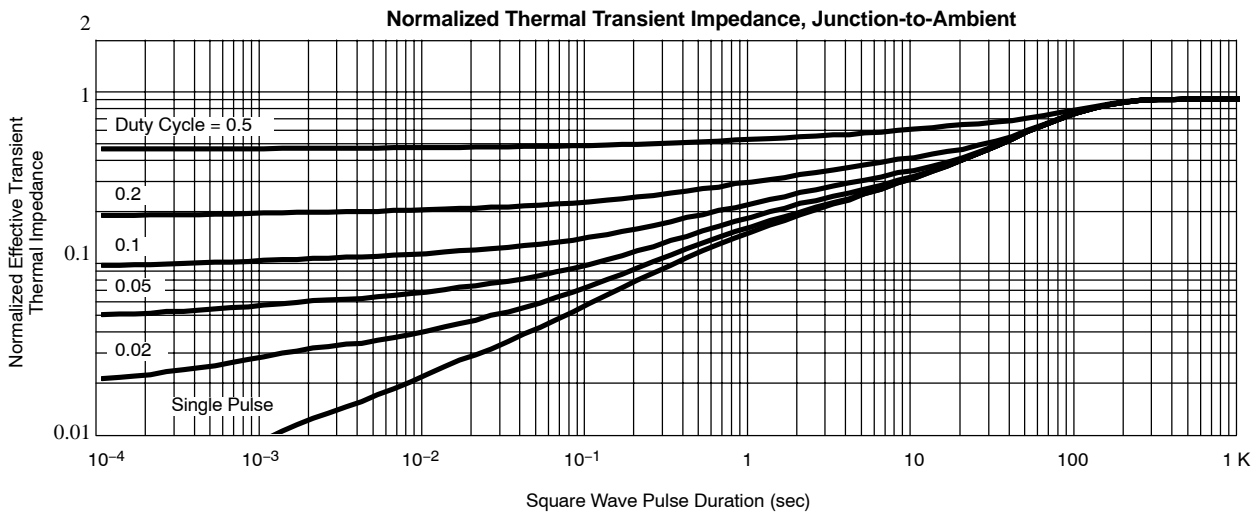
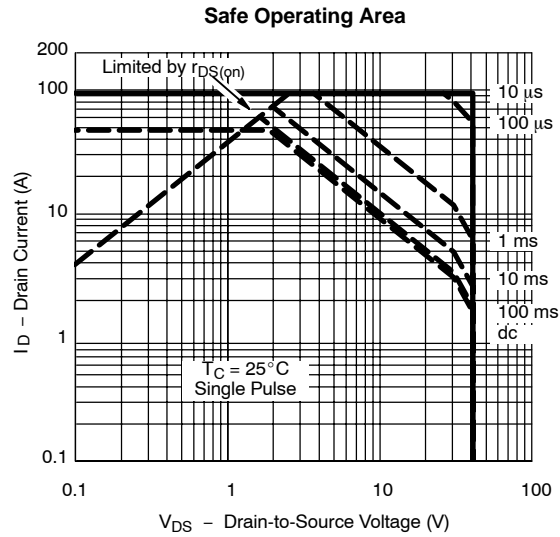
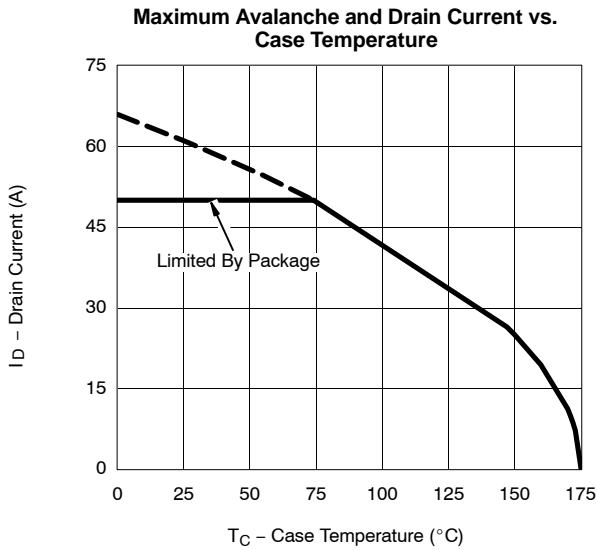




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