AUK Semiconductor

SUF520J

N-Channel Enhancement-Mode MOSFET

Description

- High speed switching application.
- Analog switch application.

Features

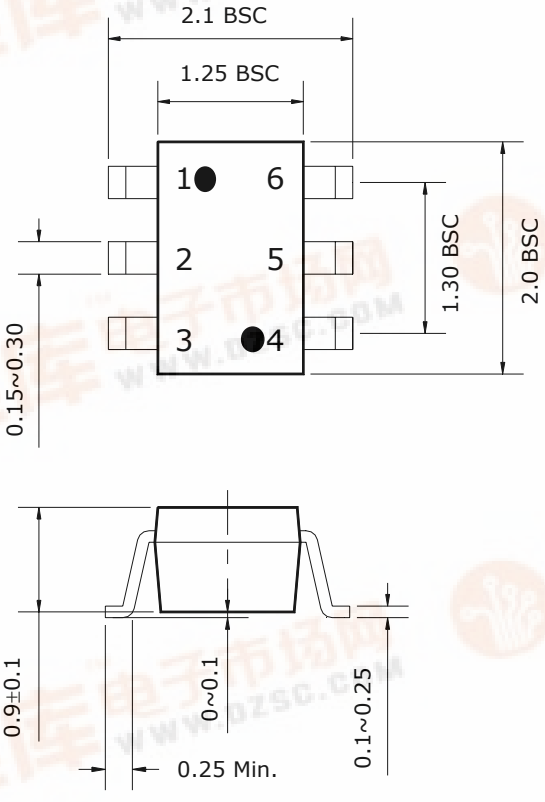
- 2.5V Gate drive.
- Low threshold voltage : Vth = 0.5~1.5V.
- Two STK1828 Chips in SOT-363 Package.

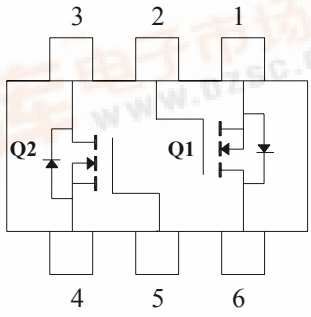
Ordering Information

Type NO.	Marking	Package Code
SUF520J	H	SOT-363

Outline Dimensions

unit : mm





PIN Connections

1. Source 1
2. Gate 1
3. Drain 2
4. Source 2
5. Gate 2
6. Drain1

Absolute maximum ratings (Q1, Q2 Common) (Ta=25°C)

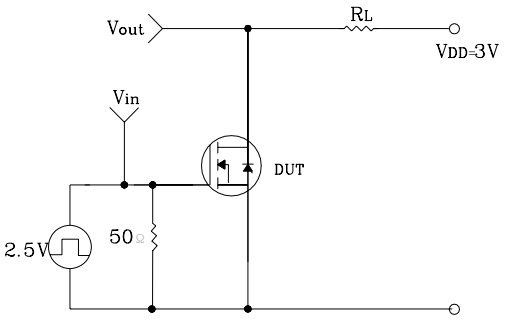
Characteristic	Symbol	Ratings	Unit
Drain-Source voltage	V_{DS}	20	V
Gate-Source voltage	V_{GSS}	10	V
DC Drain current	I_D	50	mA
Power dissipation	P_D*	200	mW
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	-55~150	°C

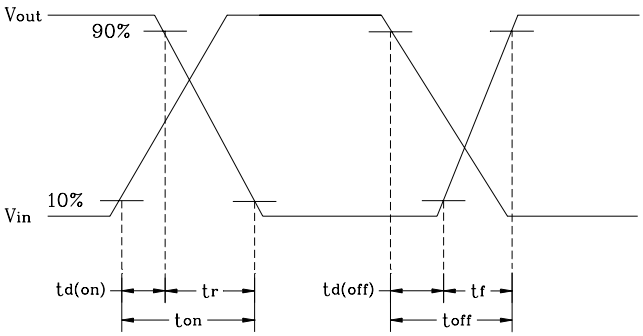
* : Total rating

Electrical Characteristics (Ta=25°C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drian-Source breakdown voltage	BV_{DSS}	I_D=100μA, V_{GS}=0	20			V
Gate-Threshold voltage	V_{th}	I_D=0.1mA, V_{DS}=3V	0.5		1.5	V
Drain cut-off current	I_{DSS}	V_{DS}=20V, V_{GS}=0			1	μA
Gate leakage current	I_{GSS}	V_{GS}=10V, V_{DS}=0			1	μA
Drain-Source on-resistance	$R_{DS(ON)}$	V_{GS}=2.5V, I_D=10mA		20	40	Ω
Forward transfer admittance	$\lvert Y_{fs} \rvert$	V_{DS}=3V, I_D=10mA	20			mS
Input capacitance	C_{iss}	V_{DS}=3V, V_{GS}=0, f=1MHz		5.5		pF
Output capacitance	C_{oss}	V_{DS}=3V, V_{GS}=0, f=1MHz		6.5		pF
Reverse Transfer capacitance	C_{rss}	V_{DS}=3V, V_{GS}=0, f=1MHz		1.6		pF
Turn-on time	t_{ON}	V_{DD}=3V, I_D=10mA V_{GEN}=0~2.5V		0.14		μs
Turn-off time	t_{OFF}	V_{DD}=3V, I_D=10mA V_{GEN}=0~2.5V		0.14		μs

* Switching Time Test Circuit





Electrical Characteristic Curves

Fig.1 I_D - V_{DS}

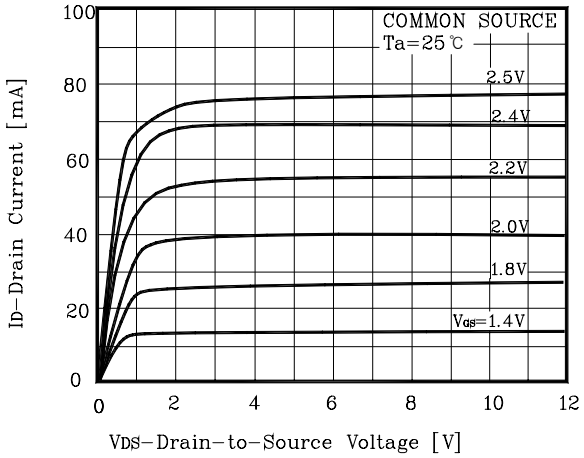


Fig.2 P_D^* - Ta

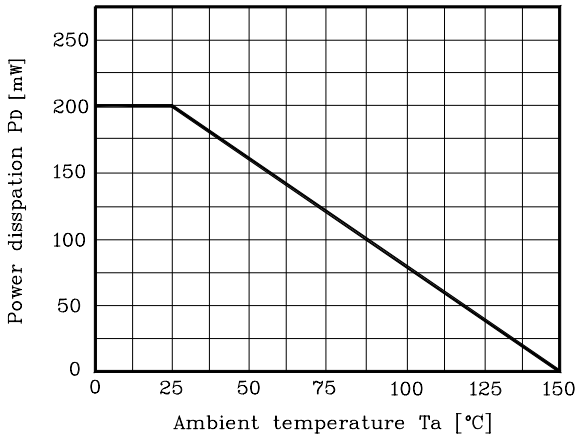


Fig.3 I_{DR} - V_{DS}

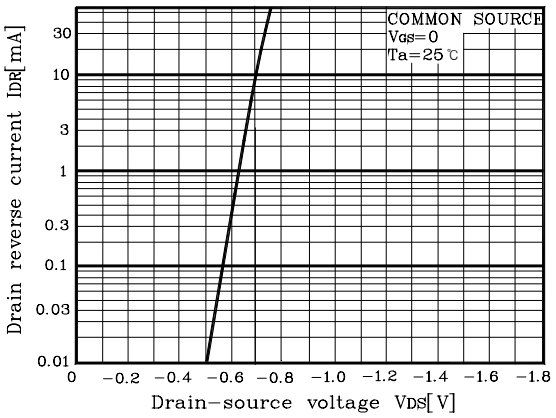


Fig.4 I_D - V_{GS}

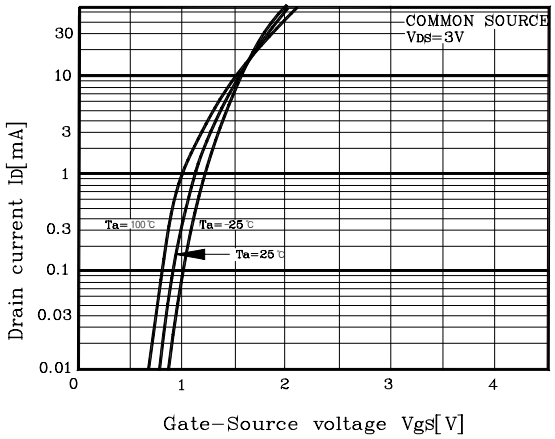


Fig.5 $|Y_{fs}|$ - I_D

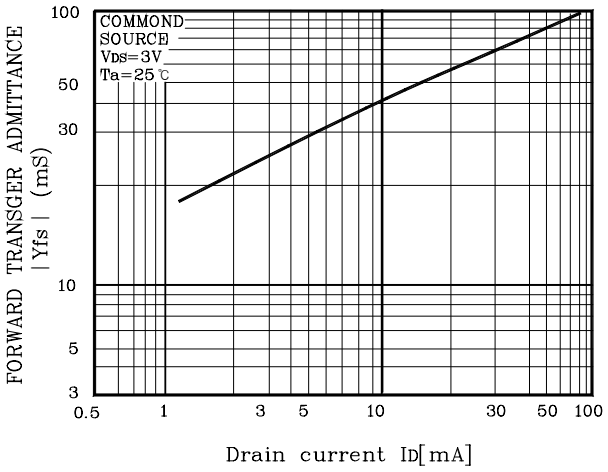
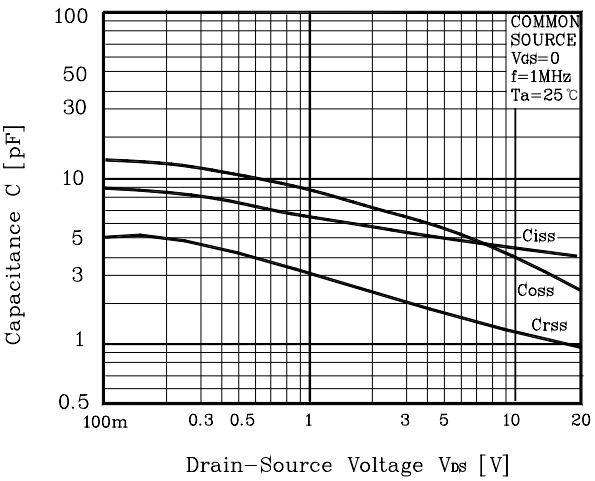


Fig.6 C - V_{DS}



Electrical Characteristic Curves

Fig.7 V_{DS} - I_D

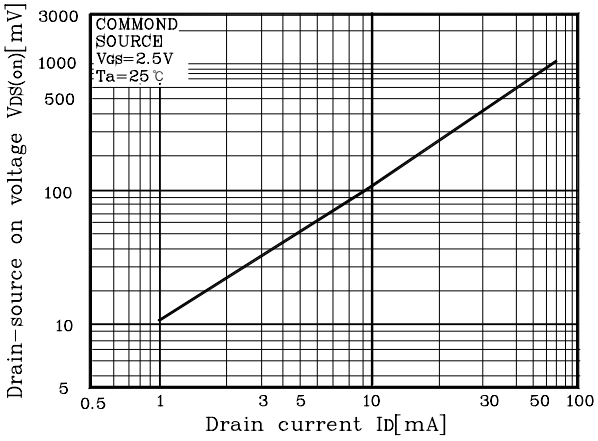


Fig.8 t - I_D