MICREL
The Infinite Bandwidth Company™

TRIPLE LVPECL-TO-PECL OR PECL-TO-LVPECL TRANSLATOR

SY100EL92

FEATURES

- **5V and 3.3V power supplies required**
- **Also, supports LVPECL-to-PECL translation**
- **500ps propagation delays**
- **Fully differential design**
- **Differential line receiver capability**
- **Application note**
- **Available in 20-pin SOIC package**

DESCRIPTION

The SY100EL92 is a triple LVPECL-to-PECL or PECL-to-LVPECL translator. The device receives standard PECL signals and translates them to differential LVPECL output signals (or vice versa). SY100EL92 can also be used as a differential line receiver for PECL-to-PECL or LVPECL-to-LVPECL signals. However, please note that for the latter we will need two different power supplies. Please refer to Function Table for more details.

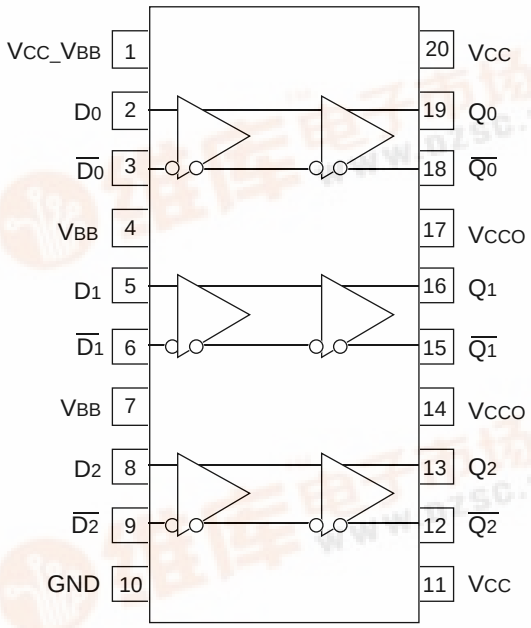
V_{BB} outputs are provided for interfacing single ended input signals. If a single ended input is to be used, the V_{BB} output should be connected to the $\overline{D}$ input and the active signal will drive the D input. When used, the V_{BB} should be bypassed to V_{CC} via a 0.01µF capacitor. The V_{BB} is designed to act as a switching reference for the SY100EL92 under single ended input conditions. As a result, the pin can only source/sink 0.5mA of current.

To accomplish the PECL-to-LVPECL level translation, the SY100EL92 requires three power rails. The V_{CC} and V_{CC_VBB} supply is to be connected to the standard PECL supply, the 3.3V supply is to be connected to the V_{CCO} supply, and GND is connected to the system ground plane. Both the V_{CC} and V_{CCO} should be bypassed to ground with a 0.01µF capacitor.

To accomplish the LVPECL-to-PECL level translation, the SY100EL92 requires three power rails as well. The 5.0V supply is connected to the V_{CC} and V_{CCO} pins, 3.3V supply is connected to the V_{CC_VBB} pin and GND is connected to the system ground plane. V_{CC_VBB} is used to provide a proper V_{BB} output level if a single ended input is used. For differential LVPECL input V_{CC_VBB} can be either 3.3V or 5V.

Under open input conditions, the $\overline{D}$ input will be biased at a $V_{CC}/2$ voltage level and the D input will be pulled to GND. This condition will force the "Q" output low, ensuring stability.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

FUNCTION TABLE

Function	Vcc	Vcco	Vcc_VBB
PECL-to-LVPECL	5.0V	3.3V	5.0V
LVPECL-to-PECL	5.0V	5.0V	3.3V
PECL-to-PECL	5.0V	5.0V	5.0V
LVPECL-to-LVPECL	5.0V	3.3V	3.3V

PIN NAMES

Pin	Function
Dn	PECL / LVPECL Inputs
Qn	PECL / LVPECL Outputs
VBB	PECL / LVPECL Reference Voltage Output
VCCO	VCC for Output
VCC_VBB	VCC for VBB Output
GND	Common Ground Rail
VCC	VCC for Internal Circuitry

PECL INPUT DC ELECTRICAL CHARACTERISTICS

V_{CC_VBB} = V_{CC} = +4.5V to +5.5V; V_{CCO} = +3.0V to +3.8V

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CC}	Power Supply Voltage	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	V
V_{IH}	Input HIGH Voltage(1)	3.835	—	4.120	3.835	—	4.120	3.835	—	4.120	3.835	—	4.120	V
V_{IL}	Input LOW Voltage(1)	3.190	—	3.515	3.190	—	3.525	3.190	—	3.525	3.190	—	3.525	V
V_{PP}	Minimum Peak-to-Peak Input	150	—	—	150	—	—	150	—	—	150	—	—	mV
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current Dn $\overline{Dn}$	0.5 –600	— —	— —	0.5 –600	— —	— —	0.5 –600	— —	— —	0.5 –600	— —	— —	µA
V_{BB}	Output Reference(1)	3.620	—	3.740	3.620	—	3.740	3.620	—	3.740	3.620	—	3.740	V
I_{CC}	Power Supply Current	—	—	12	—	—	12	—	8.0	12	—	—	12	mA

NOTE:

1. These levels are for V_{CC_VBB} = 5.0V. Level specifications will vary 1:1 with V_{CC_VBB}.

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS

V_{CC_VBB} = V_{CC} = +4.5V to +5.5V; V_{CCO} = +3.0V to +3.8V

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CCO}	Power Supply Voltage	3.0	—	3.8	3.0	—	3.8	3.0	3.3	3.8	3.0	—	3.8	V
V_{OH}	Output HIGH Voltage(1)	2.215	—	2.420	2.275	—	2.420	2.275	2.350	2.420	2.275	—	2.420	V
V_{OL}	Output LOW Voltage(1)	1.470	—	1.745	1.490	—	1.680	1.490	1.600	1.680	1.490	—	1.680	V
I_{CCO}	Power Supply Current	—	—	20	—	—	20	—	15	20	—	—	21	mA

NOTE:

1. These levels are for V_{CCO} = 3.3V. Level specifications will vary 1:1 with V_{CCO}.

LVPECL INPUT DC ELECTRICAL CHARACTERISTICS

V_{CC_VBB} = +3.0V to +3.8V(1); V_{CC} = V_{CCO} = +4.5V to +5.5V

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CC}	Power Supply Voltage	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	V
V_{IH}	Input HIGH Voltage(2)	2.135	—	2.420	2.135	—	2.420	2.135	—	2.420	2.135	—	2.420	V
V_{IL}	Input LOW Voltage(2)	1.490	—	1.825	1.490	—	1.825	1.490	—	1.825	1.490	—	1.825	V
V_{PP}	Minimum Peak-to-Peak Input	150	—	—	150	—	—	150	—	—	150	—	—	mV
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current Dn $\overline{Dn}$	0.5 –600	— —	— —	0.5 –600	— —	— —	0.5 –600	— —	— —	0.5 –600	— —	— —	µA
V_{BB}	Output Reference(2)	1.92	—	2.04	1.92	—	2.04	1.92	—	2.04	1.92	—	2.04	V
I_{CC}	Power Supply Current	—	—	12	—	—	12	—	8.0	12	—	—	12	mA

NOTES:

1. V_{CC_VBB} = 3.3V is only required for single-ended LVPECL input. For differential LVPECL input, V_{CC_VBB} can be either 3.3V or 5V.
2. These levels are for V_{CC_VBB} = 3.3V. Level specifications will vary 1:1 with V_{CC_VBB}.

PECL OUTPUT DC ELECTRICAL CHARACTERISTICS

V_{CC}_V_{BB} = +3.0V to +3.8V; V_{CC} = V_{CCO} = +4.5V to +5.5V

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CCO}	Power Supply Voltage	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	V
V_{OH}	Output HIGH Voltage(1)	3.915	—	4.120	3.975	—	4.120	3.975	—	4.120	3.975	—	4.120	V
V_{OL}	Output LOW Voltage(1)	3.170	—	3.445	3.190	—	3.380	3.190	—	3.380	3.190	—	3.380	V
I_{CCO}	Power Supply Current	—	—	20	—	—	20	—	15	20	—	—	21	mA

NOTE:

1. These levels are for V_{CCO} = 5.0V. Level specifications will vary 1:1 with V_{CCO}.

AC ELECTRICAL CHARACTERISTICS(1)

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Diff. D to Q S.E.	430 410	520 540	630 710	430 410	520 540	630 710	430 410	520 540	630 710	430 410	520 540	630 710	ps
t_{skew}	Within-Device Skew Output-to-Output(2) Part-to-Part (Diff.)(2) Duty Cycle (Diff.)(3)	 — — —	 20 20 25	 100 200 —	 — — —	 20 20 25	 100 200 —	 — — —	 20 20 25	 100 200 —	 — — —	 20 20 25	 100 200 —	ps
V_{PP}	Minimum Input Swing(4)	150	—	—	150	—	—	150	—	—	150	—	—	mV
V_{CMR}	Common Mode Range(5) V_{PP} < 500mV V_{PP} ≥ 500mV	 1.3 1.5	 — —	 V_{CC}–0.2 V_{CC}–0.2	 1.2 1.4	 — —	 V_{CC}–0.2 V_{CC}–0.2	 1.2 1.4	 — —	 V_{CC}–0.2 V_{CC}–0.2	 1.2 1.4	 — —	 V_{CC}–0.2 V_{CC}–0.2	V
tr tf	Output Rise/Fall Times Q (20% to 80%)	320	—	580	320	—	580	320	—	580	320	—	580	ps

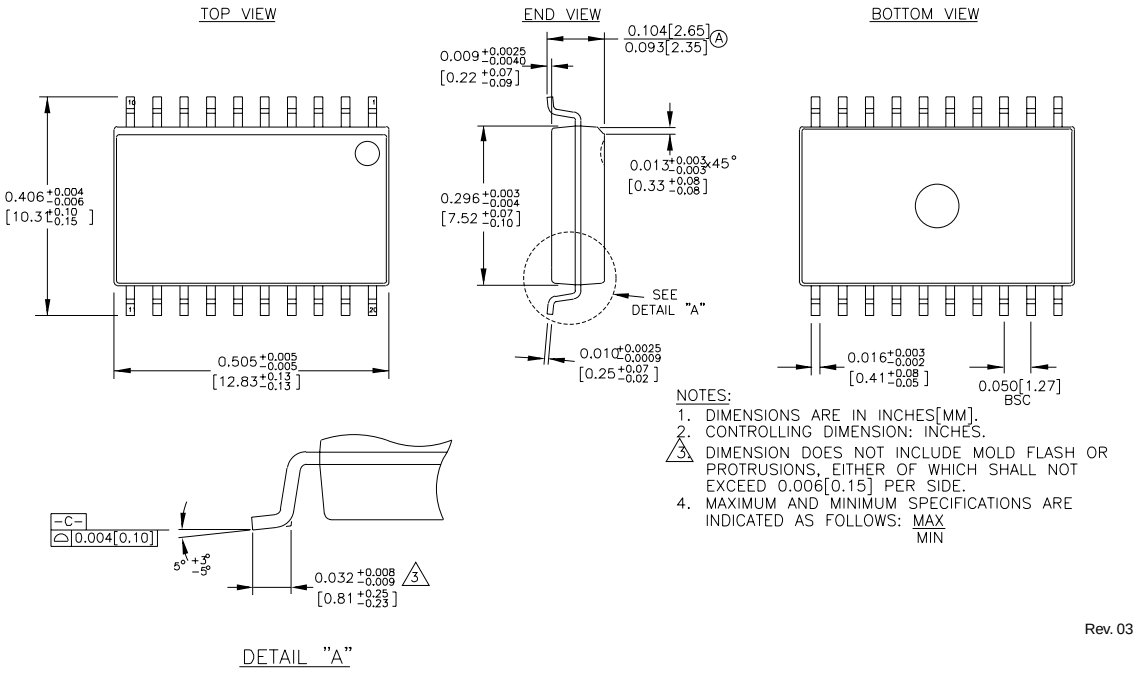
NOTES:

1. Power supply requirements applies as indicated in the DC electrical characteristics tables.
2. Skew is measured between outputs under identical transitions.
3. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device Common Mode Range.
4. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ~40.
5. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100EL92ZC	Z20-1	Commercial
SY100EL92ZCTR	Z20-1	Commercial

20 LEAD SOIC .300" WIDE (Z20-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.
4. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN

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