MICREL
The Infinite Bandwidth Company™

3.3V DUAL DIFFERENTIAL LVPECL-to-LVTTL TRANSLATOR

ClockWorks™
SY10ELT23L
SY100ELT23L

FEATURES

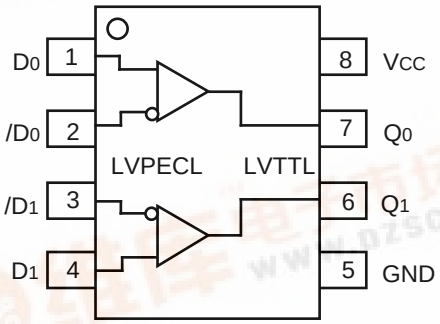
- **3.3V power supply**
- **2.0ns typical propagation delay**
- **<500ps typical output-to-output skew**
- **Differential LVPECL inputs**
- **24mA LVTTL outputs**
- **Flow-through pinouts**
- **Available in 8-pin SOIC package**

DESCRIPTION

The SY10/100ELT23L are dual differential LVPECL-to-LVTTL translators with +3.3V power supply. Because LVPECL (Low Voltage Positive ECL) levels are used, only +3.3V and ground are required. The small outline 8-lead SOIC package and the low skew, dual gate design of the ELT23L makes it ideal for applications which require the translation of a clock and a data signal.

The ELT23L is available in both ECL standards: the 10ELT is compatible with positive ECL 10H logic levels, while the 100ELT is compatible with positive ECL 100K logic levels.

PIN CONFIGURATION/BLOCK DIAGRAM



PIN NAMES

Pin	Function
Q_n	LVTTL Outputs
D_n	Differential LVPECL Inputs
V_{CC}	+3.3V Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Paramter	Value	Unit
V_{CC}	Power Supply Voltage	–0.5 to +3.8	V
V_I	PECL Input Voltage	0V to V_{CC}+0.5	V
V_O	Voltage Applied to Output at HIGH State	–0.5 to V_{CC}	V
I_O	Current Applied to Output at LOW State	Twice the Rated I_{OL}	mA
T_{store}	Storage Temperature	–65 to +150	°C
T_{amb}	Operating Temperature	–40 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

TRUTH TABLE

D	$\overline{D}$	Q
L	H	L
H	L	H
Open	Open	L

LVTTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±5%

		T_A = -40°C		T_A = 0°C		T_A = +25°C		T_A = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	2.0	—	2.0	—	2.0	—	2.0	—	V	I_{OH} = –3.0mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	—	0.5	V	I_{OL} = 24mA
I_{CC}	Power Supply Current	—	30	—	30	—	30	—	30	mA	
I_{OS}	Output Short Circuit Current	–80	–240	–80	–240	–80	–240	–80	–240	mA	V_{OUT} = 0V

LVPECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±5%

		T_A = -40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	0.5	—	—	µA
V_{CMR}	Common Mode Range	1.5	—	V_{CC}	1.5	—	V_{CC}	1.5	—	V_{CC}	1.5	—	V_{CC}	V
V_{PP}	Minimum Peak-to-Peak Input(1)	200	—	—	200	—	—	200	—	—	200	—	—	mV
V_{IH}	Input HIGH Voltage(2)													mV
	10ELT	2070	—	2410	2130	—	2460	2170	—	2490	2130	—	2565	
	100ELT	2135	—	2420	2135	—	2420	2135	—	2420	2135	—	2420	
V_{IL}	Input LOW Voltage(2)													mV
	10ELT	1350	—	1800	1350	—	1820	1350	—	1820	1350	—	1820	
	100ELT	1490	—	1825	1490	—	1825	1490	—	1825	1490	—	1825	

NOTES:

1. 200mV input guarantees full logic at output.
2. These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC}.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±5%

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay	1.5	2.5	1.5	2.5	1.5	2.5	1.5	2.5	ns	C_L = 20pF
t_{skpp}	Part-to-Part Skew(1,4)	—	0.5	—	0.5	—	0.5	—	0.5	ns	C_L = 20pF
t_{skew++}	Within-Device Skew(2,4)	—	0.3	—	0.3	—	0.3	—	0.3	ns	C_L = 20pF
t_{skew--}	Within-Device Skew(3,4)	—	0.3	—	0.3	—	0.3	—	0.3	ns	C_L = 20pF
t_r t_f	Output Rise/Fall Time 1.0V to 2.0V	0.5	1.0	0.5	1.0	0.5	1.0	0.5	1.0	ns	C_L = 20pF
f_{MAX}	Maximum Input Frequency(5,6)	160	—	160	—	160	—	160	—	MHz	C_L = 20pF

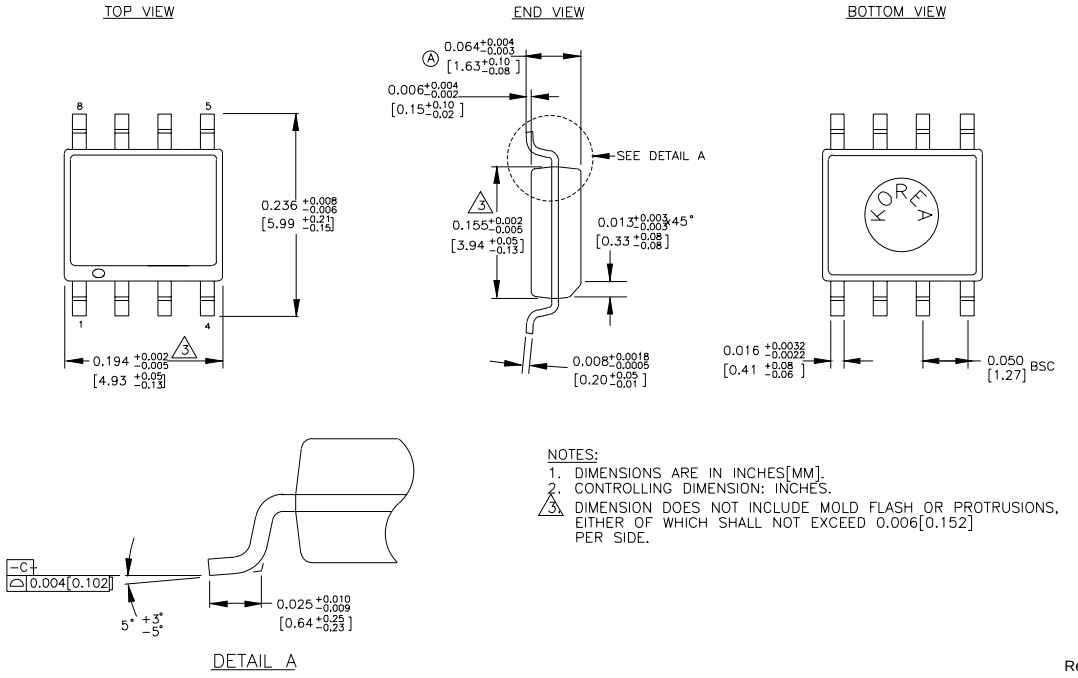
NOTES:

1. Device-to-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
2. Within-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
3. Within-Device Skew considering LOW-to-LOW transitions at common V_{CC} level.
4. All skew parameters are guaranteed but not tested.
5. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.
6. The f_{MAX} value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range	V_{CC} Range (V)
SY10ELT23LZC	Z8-1	Commercial	+3.3 ±5%
SY10ELT23LZCTR	Z8-1	Commercial	+3.3 ±5%
SY100ELT23LZC	Z8-1	Commercial	+3.3 ±5%
SY100ELT23LZCTR	Z8-1	Commercial	+3.3 ±5%

8 LEAD SOIC .150" WIDE (Z8-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.152] PER SIDE.

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