



**3.3V, 2.0GHz ANY DIFFERENTIAL IN-TO-LVDS  
PROGRAMMABLE CLOCK DIVIDER AND  
1:2 FANOUT BUFFER W/ INTERNAL TERMINATION**

**Precision Edge®  
SY89876L**

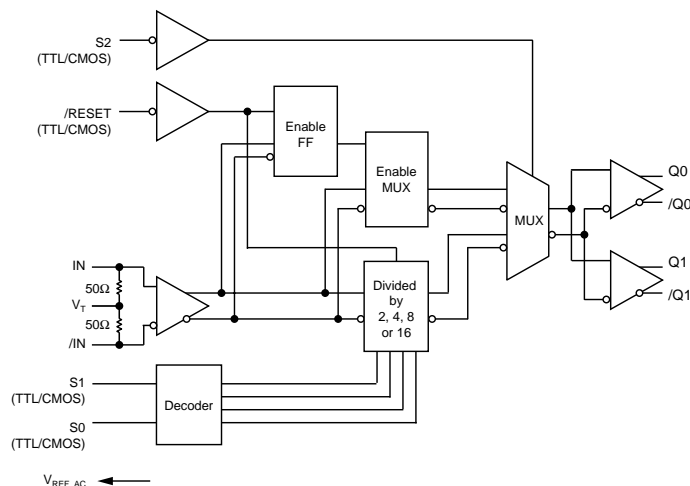
## FEATURES

- Integrated programmable clock divider and 1:2 fanout buffer
- Guaranteed AC performance over temperature and voltage:
  - >2.0GHz  $f_{MAX}$
  - <190ps  $t_r / t_f$
  - <15ps within device skew
- Low jitter design:
  - <10ps<sub>PP</sub> total jitter
  - <1ps<sub>RMS</sub> cycle-to-cycle jitter
- Unique input termination and VT Pin for DC- and AC-coupled inputs; CML, PECL, LVDS and HSTL
- LVDS-compatible outputs
- TTL/CMOS inputs for select and reset
- Parallel programming capability
- Programmable divider ratios of 1, 2, 4, 8 and 16
- Low voltage operation 3.3V
- Output disable function
- -40°C to 85°C industrial temperature range
- Available in 16-pin (3mm x 3mm) MLF™ package

## APPLICATIONS

- SONET/SDH line cards
- Transponders
- High-end, multiprocessor servers

## FUNCTIONAL BLOCK DIAGRAM



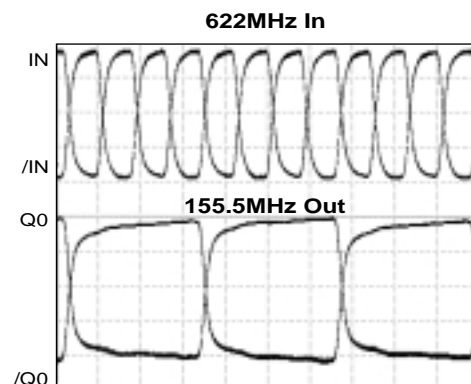
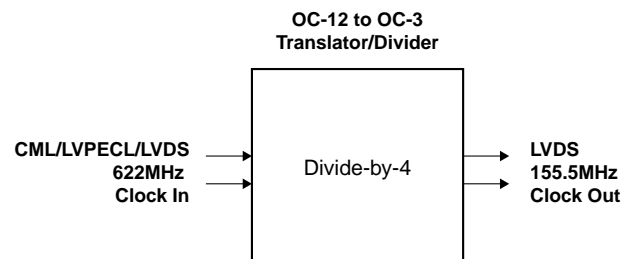
## DESCRIPTION

This low-skew, low-jitter device is capable of accepting a high-speed (e.g., 622MHz or higher) CML, LVPECL, LVDS or HSTL clock input signal and dividing down the frequency using a programmable divider ratio to create a lower speed version of the input clock. Available divider ratios are 2, 4, 8 and 16, or straight pass-through.

The differential input buffer has a unique internal termination design that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards. A  $V_{REF-AC}$  reference is included for AC-coupled applications.

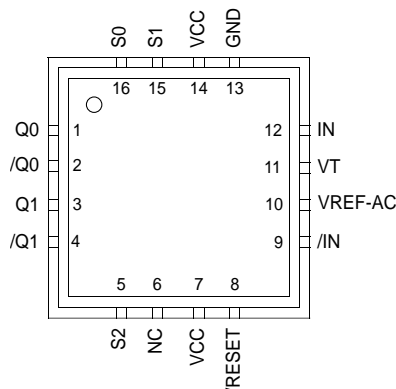
The /RESET input asynchronously resets the divider. In the pass-through function (divide by 1) the /RESET synchronously enables or disables the outputs on the next falling edge of IN (rising edge of /IN).

## TYPICAL PERFORMANCE



Precision Edge is a registered trademark of Micrel, Inc.  
MicroLeadFrame and MLF are trademarks of Amkor Technology, Inc.

**PACKAGE/ORDERING INFORMATION**



**16-Pin MLF™ (MLF-16)**

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89876LMI	MLF-16	Industrial	876L	Sn-Pb
SY89876LMITR <sup>(2)</sup>	MLF-16	Industrial	876L	Sn-Pb
SY89876LMG <sup>(3)</sup>	MLF-16	Industrial	876L with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY89876LMGTR <sup>(2, 3)</sup>	MLF-16	Industrial	876L with Pb-Free bar-line indicator	Pb-Free NiPdAu

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at  $T_A = 25^\circ\text{C}$ , DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

**PIN DESCRIPTION**

Pin Number	Pin Name	Pin Function
12, 9	IN, /IN	Differential Input: Internal 50Ω termination resistors to $V_T$ input. Flexible input accepts any differential input. See “Input Interface Applications” section.
1, 2, 3, 4	Q0, /Q0 Q1, /Q1	Differential Buffered LVDS Outputs: Divided by 1, 2, 4, 8 or 16. See “Truth Table.” Unused output pairs must be terminated with 100Ω across the different pair.
16, 15, 5	S0, S1, S2	Select Pins: See “Truth Table.” LVTTTL/CMOS logic levels. Internal 25kΩ pull-up resistor. Logic HIGH if left unconnected (divided by 16 mode.) Input threshold is $V_{CC}/2$ .
6	NC	No Connect.
8	/RESET, /DISABLE	LVTTTL/CMOS Logic Levels: Internal 25kΩ pull-up resistor. Logic HIGH if left unconnected. Apply LOW to reset the divider (divided by 2, 4, 8 or 16 mode). Also acts as a disable/enable function. The reset and disable function occurs on the next high-to-low clock input transition. Input threshold is $V_{CC}/2$ .
10	VREF-AC	Reference Voltage: Equal to $V_{CC}-1.4\text{V}$ (approx.). Used for AC-coupled applications only. Decouple the VREF-AC pin with a 0.01μF capacitor. See “Input Interface Applications” section.
11	VT	Termination Center-Tap: For CML or LVDS inputs, leave this pin floating. Otherwise, See Figures 4a to 4f “Input Interface Applications” section.
7, 14	VCC	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitor.
13	GND, Exposed pad	Ground. Exposed pad must be connected to the same potential as the GND pin.

**TRUTH TABLE**

/RESET <sup>(1)</sup>	S2	S1	S0	Outputs
1	0	X	X	Reference Clock (pass through)
1	1	0	0	Reference Clock ÷2
1	1	0	1	Reference Clock ÷4
1	1	1	0	Reference Clock ÷8
1	1	1	1	Reference Clock ÷16
0 <sup>(1)</sup>	X	X	X	Q = LOW, /Q = HIGH Clock Disable

**Note:**

1. Reset/Disable function is asserted on the next clock input (IN, /IN) high-to-low transition.

### Absolute Maximum Ratings<sup>(Note 1)</sup>

Supply Voltage ( $V_{CC}$ )	.....	-0.5V to +4.0V
Input Voltage ( $V_{IN}$ )	.....	-0.5V to $V_{CC}+0.3$
ECL Output Current ( $I_{OUT}$ )		
Continuous	.....	50mA
Surge	.....	100mA
Input Current $I_N$ , $/I_N$ ( $I_{IN}$ )	.....	$\pm 50$ mA
$V_T$ Current ( $I_{VT}$ )	.....	$\pm 100$ mA
$V_{REF-AC}$ Sink/Source Current ( $I_{VREF-AC}$ ), <b>Note 3</b>	.....	$\pm 2$ mA
Lead Temperature (soldering 20 sec.)	.....	260°C
Storage Temperature ( $T_S$ )	.....	-65°C to +150°C

### Operating Ratings<sup>(Note 2)</sup>

Supply Voltage ( $V_{CC}$ )	.....	+3.3V $\pm 10\%$
Ambient Temperature ( $T_A$ )	.....	-40°C to +85°C
Package Thermal Resistance		
MLF™ ( $\theta_{JA}$ )		
Still-Air	.....	60°C/W
500lfpm	.....	54°C/W
MLF™ ( $\psi_{JB}$ ), <b>Note 4</b>		
Junction-to-Board	.....	32°C/W

- Note 1.** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- Note 2.** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
- Note 3.** Due to the limited drive capability use for input of the same package only.
- Note 4.** Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

## DC ELECTRICAL CHARACTERISTICS<sup>(Notes 1, 2)</sup>

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{CC}$	Power Supply		3.0		3.6	V
$I_{CC}$	Power Supply Current	No load, max. $V_{CC}$		75	100	mA
$R_{IN}$	Differential Input Resistance (IN-to-/IN)		90	100	110	$\Omega$
$V_{IH}$	Input High Voltage (IN, /IN)	<b>Note 2</b>	0.1	–	$V_{CC}+0.3$	V
$V_{IL}$	Input Low Voltage (IN, /IN)	<b>Note 2</b>	-0.3	–	$V_{CC}+0.2$	V
$V_{IN}$	Input Voltage Swing	<b>Note 3</b>		–	1.8	V
$V_{DIFF\_IN}$	Differential Input Voltage Swing	<b>Note 4</b>	0.1	–		V
$ I_{IN} $	Input Current (IN, /IN)	<b>Note 2</b>	–	–	45	mA
$V_{REF-AC}$	Reference Voltage	<b>Note 5</b>	$V_{CC}-1.525$	$V_{CC}-1.425$	$V_{CC}-1.325$	V

- Note 1.** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
- Note 2.** Specification for packaged product only.
- Note 3.** Due to the internal termination (see Figure 2a) the input current depends on the applied voltages at IN, /IN and  $V_T$  inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit!
- Note 4.** See "Timing Diagram" for  $V_{IN}$  definition.  $V_{IN}$  (Max) is specified when  $V_T$  is floating.
- Note 5.** See "Typical Operating Characteristics" section for  $V_{DIFF}$  definition.
- Note 6.** Operating using  $V_{IN}$  is limited to AC-coupled PECL or CML applications only. Connect directly to  $V_T$  pin.

**LVDS DC ELECTRICAL CHARACTERISTICS(Notes 1, 2)**

$V_{CC} = 3.3V \pm 10\%$ ;  $R_L = 100\Omega$  across the outputs;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OUT}$	Output Voltage Swing	<b>Note 3, 4</b>	250	350	400	mV
$V_{OH}$	Output High Voltage	<b>Note 3</b>			1.475	V
$V_{OL}$	Output Low Voltage	<b>Note 3</b>	0.925			V
$V_{OCM}$	Output Common Mode Voltage	<b>Note 4</b>	1.125		1.375	V
$\Delta V_{OCM}$	Change in Common Mode Voltage		-50		50	mV

**Note 1.** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

**Note 2.** Specification for packaged product only.

**Note 3.** Measured as per Figure 3a,  $100\Omega$  across Q and /Q outputs.

**Note 4.** Measured as per Figure 3b.

**LVTTTL/CMOS DC ELECTRICAL CHARACTERISTICS(Notes 1, 2)**

$V_{CC} = 3.3V \pm 10\%$ ;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IH}$	Input HIGH Voltage		2.0			V
$V_{IL}$	Input LOW Voltage				0.8	V
$I_{IH}$	Input HIGH Current		-125		20	$\mu\text{A}$
$I_{IL}$	Input LOW Current				-300	$\mu\text{A}$

**Note 1.** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

**Note 2.** Specification for packaged product only.

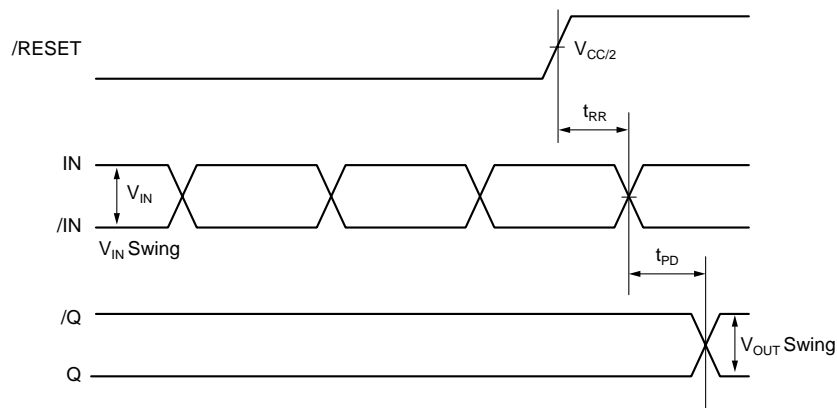
**AC ELECTRICAL CHARACTERISTICS(Notes 1)**

$V_{CC} = 3.3V \pm 10\%$ ;  $R_L = 100\Omega$  across the outputs;  $T_A = -40^\circ C$  to  $+85^\circ C$ ; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{MAX}$	Maximum Input Frequency	$V_{OUT} \geq 200mV$	2.0	2.5		GHz
$t_{PD}$	Differential Propagation Delay IN to Q	Input Swing < 400mV	590	690	870	ps
		Input Swing $\geq 400mV$	540	640	820	ps
$t_{SKEW}$	Within-Device Skew (diff.)	<b>Note 2</b>		5	15	ps
	Part-to-Part Skew (diff.)	<b>Note 2</b>			280	ps
$t_{RR}$	Reset Recovery Time	<b>Note 3</b>	600			ps
$T_{jitter}$	Cycle-to-Cycle Jitter	<b>Note 4</b>			1	ps <sub>RMS</sub>
	Total Jitter	<b>Note 5</b>			10	ps <sub>PP</sub>
$t_r, t_f$	Rise/Fall Time (20% to 80%)		60	110	190	ps

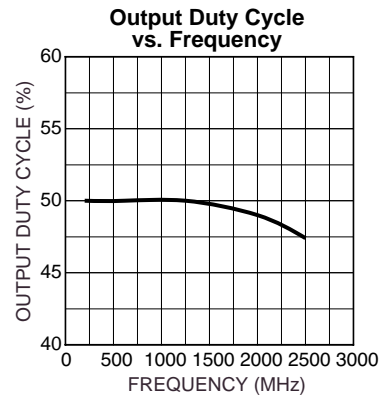
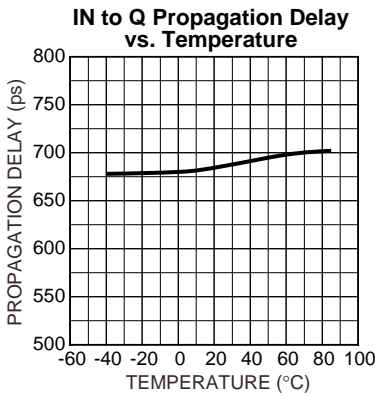
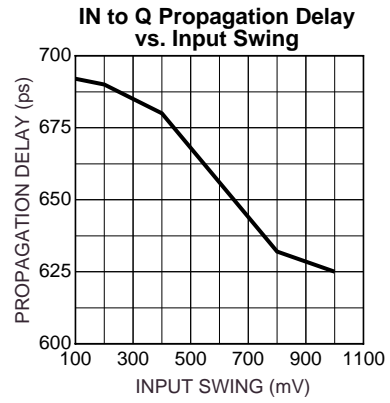
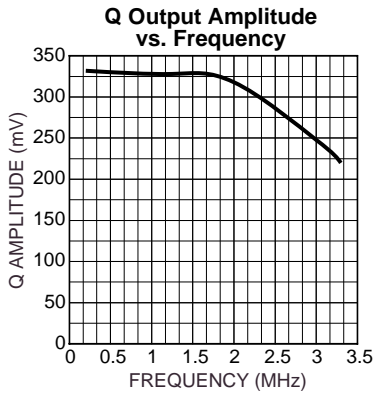
- Note 1.** Measured with 400mV input signal, 50% duty cycle, all outputs loaded with 100Ω across each output pair, unless otherwise stated.
- Note 2.** Skew is measured between outputs under identical transitions.
- Note 3.** See "Timing Diagram."
- Note 4.** Cycle-to-cycle jitter definition: the variation in period between adjacent cycles over a random sample of adjacent cycle pairs.  $T_{jitter\_cc} = T_n - T_{n+1}$ , where T is the time between rising edges of the output signal.
- Note 5.** Total jitter definition: with an ideal clock input of frequency  $\leq f_{MAX}$ , no more than one output edge in  $10^{12}$  output edges will deviate by more than the specified peak-to-peak jitter value.

**TIMING DIAGRAM**



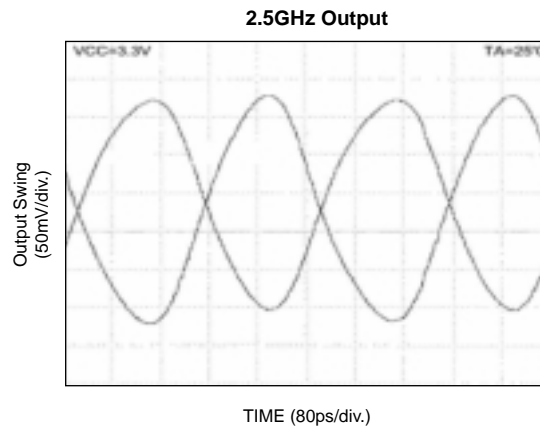
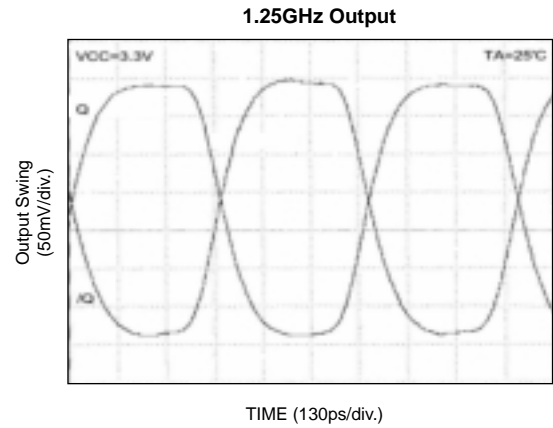
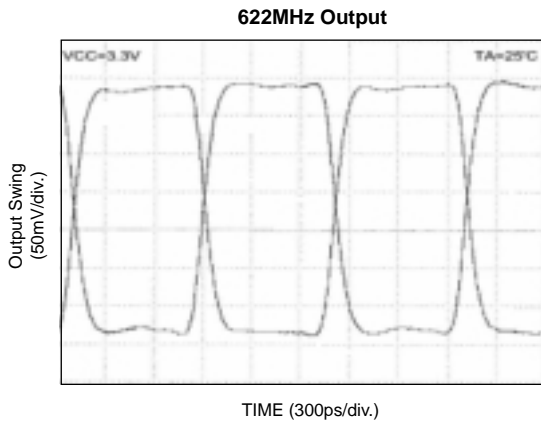
**TYPICAL OPERATING CHARACTERISTICS**

$V_{CC} = 3.3V$ ,  $R_L = 100\Omega$  across the output;  $T_A = 25^\circ C$ , unless otherwise stated.

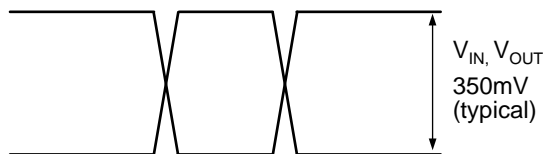


**TYPICAL OPERATING CHARACTERISTICS (Continued)**

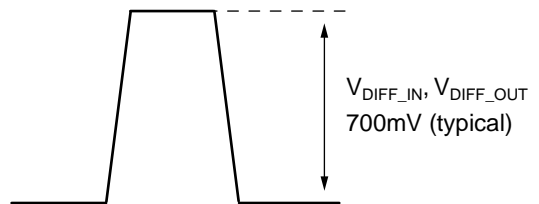
$V_{CC} = 3.3V$ ,  $V_{IN} = 100mV$ ,  $R_L = 100\Omega$  across the output;  $T_A = 25^\circ C$ , unless otherwise stated.



**DEFINITION OF SINGLE-ENDED AND DIFFERENTIAL SWINGS**



**Figure 1a. Single-Ended Swing**



**Figure 1b. Differential Swing**

**INPUT INTERFACE APPLICATIONS**

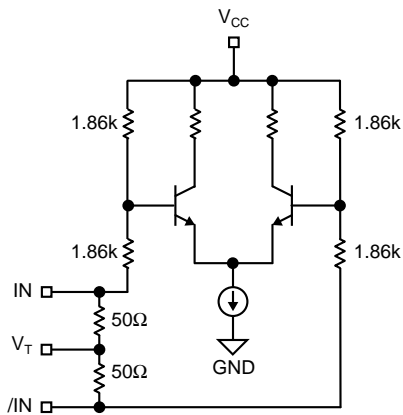


Figure 2a. Simplified Differential Input Buffer

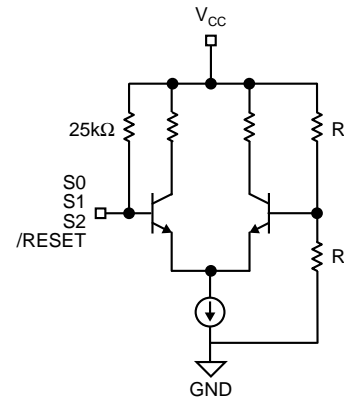


Figure 2b. Simplified TTL/CMOS Input Buffer

**LVDS OUTPUTS**

LVDS (Low Voltage Differential Swing) specifies a small swing of 350mV typical, on a nominal 1.25V common mode above ground. The common mode voltage has tight limits

to permit large variations in ground between an LVDS driver and receiver.

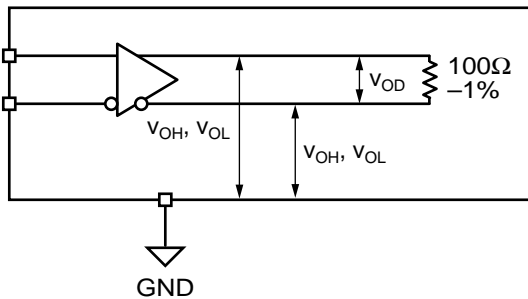


Figure 3a. LVDS Differential Measurement

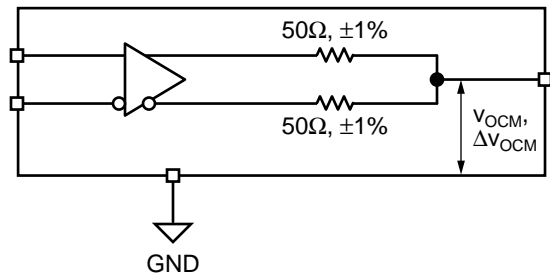
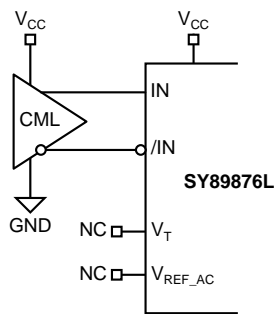


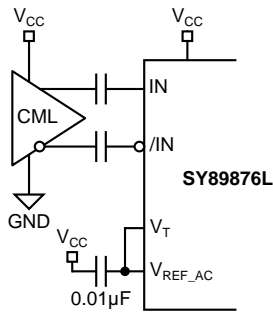
Figure 3b. LVDS Common Mode Measurement



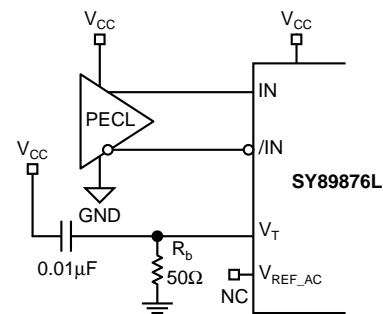
**INPUT INTERFACE APPLICATIONS**



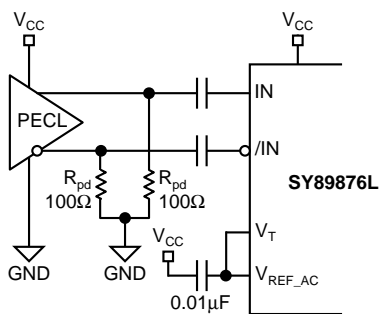
**Figure 4a. DC-Coupled CML Input Interface**



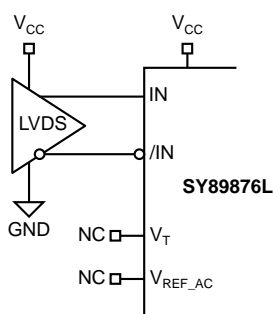
**Figure 4b. AC-Coupled CML Input Interface**



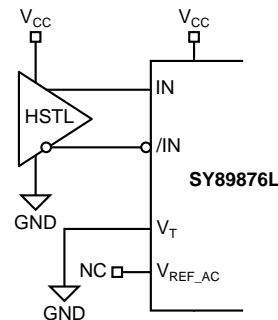
**Figure 4c. DC-Coupled PECL Input Interface**



**Figure 4d. AC-Coupled PECL Input Interface**



**Figure 4e. LVDS Input Interface**

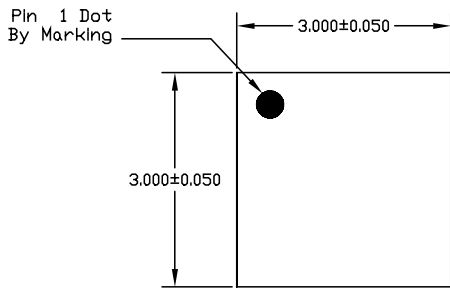


**Figure 4f. HSTL Input Interface**

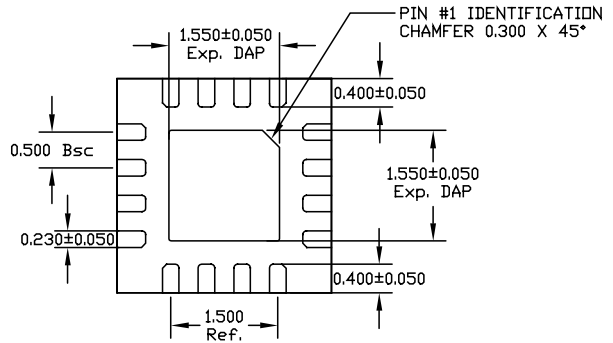
**RELATED PRODUCT AND SUPPORT DOCUMENTATION**

Part Number	Function	Data Sheet Link
SY89873L	3.3V, 2.5GHz Any Diff. IN-to-LVDS Programmable Clock Divider/Fanout Buffer w/ Internal Termination	<a href="http://www.micrel.com/product-info/products/sy89873l.shtml">http://www.micrel.com/product-info/products/sy89873l.shtml</a>
	MLF™ Application Note	<a href="http://www.amkor.com/products/notes_papers/mlf_appnote.pdf">http://www.amkor.com/products/notes_papers/mlf_appnote.pdf</a>
HBW Solutions	New Products and Applications	<a href="http://www.micrel.com/product-info/products/solutions.shtml">http://www.micrel.com/product-info/products/solutions.shtml</a>

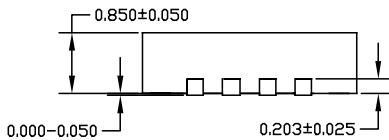
**16 LEAD *MicroLeadFrame*™ (MLF-16)**



TOP VIEW

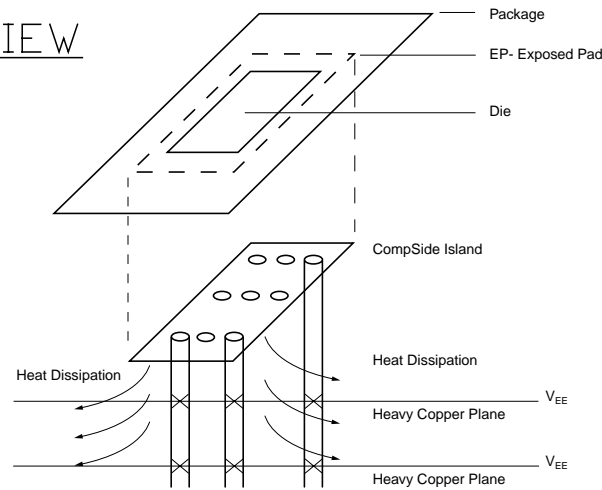


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. MAX. PACKAGE WARPAGE IS 0.05 mm.
  3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
  4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



**PCB Thermal Consideration for 16-Pin MLF™ Package  
(Always solder, or equivalent, the exposed pad to the PCB)**

**Package Notes:**

- Note 1.** Package meets Level 2 moisture sensitivity classification, and are shipped in dry-pack form.  
**Note 2.** Exposed pads must be soldered to a ground for proper thermal management.

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