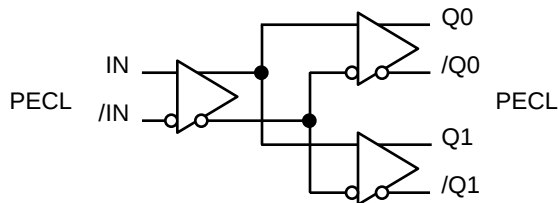




FEATURES

- 2.5V, 3.3V and 5V power supply
- Guaranteed AC parameters over temperature:
 - $f_{MAX} > 3.0\text{GHz}$
 - $< 20\text{ps}$ output-to-output skew
 - $< 200\text{ps}$ t_r / t_f
 - $< 300\text{ps}$ propagation delay
- 100K compatible I/O
- Wide temperature range: -40°C to $+85^\circ\text{C}$
- Available in ultra-small 8-pin MLF™ (2mm x 2mm) package

BLOCK DIAGRAM

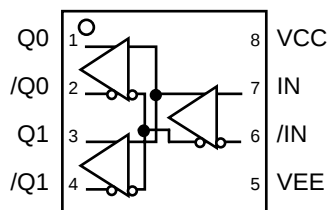


DESCRIPTION

The SY89311U is a precision, high-speed 1:2 differential fanout buffer. Having within-device skews and output transition times significantly improved over the EL11V, the SY89311U is ideally suited for those applications which require the ultimate in AC performance in a small package.

The differential inputs of the SY89311U employ clamping circuitry to maintain stability under open input conditions. If the inputs are left open, the Q outputs will be LOW.

The differential inputs can accept 10/100K ECL/PECL signals (external termination required) and the outputs are 100K ECL/PECL compatible.

PACKAGE/ORDERING INFORMATION**8-Pin MLF™****Ultra-Small Outline (2mm × 2mm)****Ordering Information**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89311UMITR	MLF-8	Industrial	HP11	Sn-Pb
SY89311UMGTR	MLF-8	Industrial	HP11 with Pb-Free bar-line indicator	Pb-Free NiPdAu

PIN DESCRIPTION

Pin Number	Pin Name	Type	Pin Function
1, 2, 3, 4	Q0, /Q0, Q1, /Q1	100K Output	Differential PECL/ECL Outputs: Default to LOW if IN inputs are left open. See "Output Interface Applications" section for recommendations on terminations. Unused output pairs may be left floating without any impact on skew or jitter.
5	VEE, Exposed Pad	Negative Power Supply	Negative Power Supply: V_{EE} and exposed pad must be tied to most negative supply. For PECL/LVPECL connect to ground.
6	/IN	100K Input	Differential PECL/ECL Input: Internal 75k Ω pull-up and pull-down resistors. If left floating, pin defaults to $V_{CC}/2$. When not used, this input can be left open. See "Input Interface Applications" section for single-ended inputs.
7	IN	100K Input	Differential PECL/ECL Input: Internal 75k Ω pull-down resistor. If left open, pin defaults LOW. Q output will be LOW. Accepts differential 10K and 100K ECL/PECL. See "Input Interface Applications" section for single-ended inputs.
8	VCC	Positive Power Supply	Positive Power Supply: Bypass with 0.1 μ F//0.01 μ F low ESR capacitors.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC})	–0.5V to +6.0V
Input Voltage (V_{IN})	–0.5V to V_{CC}
LVPECL Output Current (I_{OUT})	
Continuous	50mA
Surge	100mA
Input Current	
Source or sink current on IN, /IN	±50mA
Lead Temperature (soldering, 20 sec.)	+260°C
Storage Temperature (T_S)	–65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage $ V_{CC}-V_{EE} $	+2.375V to +2.625V
	+3.0V to +3.6V
	+4.5V to +5.5V
Ambient Temperature (T_A)	–40°C to +85°C
Package Thermal Resistance, Note 3	
MLF™ (θ_{JA})	
Still-Air	93°C/W
500lfpm	87°C/W
MLF™ (Ψ_{JB})	
Junction-to-Board	60°C/W

DC ELECTRICAL CHARACTERISTICS⁽⁴⁾ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	LVPECL	2.375	2.5	2.625	V
		LVPECL	3.0	3.3	3.6	V
		PECL	4.5	5.0	5.5	V
		ECL	–5.5	–5.0	–4.5	V
		LVECL	–3.6	–3.3	–3.0	V
		LVECL	–2.625	–2.5	–2.375	V
I_{EE}	Power Supply Current	Max. V_{CC} , no load		30	44	mA
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH}$			150	μA
I_{IL}	Input LOW Current	IN	0.5			μA
		/IN	–150			μA
C_{IN}	Input Capacitance			1.0		pF

(100K) ECL/LVECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +2.5V \pm 5\%$ or $+3.3V \pm 10\%$ or $+5.0V \pm 10\%$ and $V_{EE} = 0V$; $V_{CC} = 0V$ and $V_{EE} = -2.5V \pm 5\%$ or $-3.3V \pm 10\%$ or $-5.0V \pm 10\%$;
 $R_L = 50\Omega$ to $V_{CC}-2V$; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage		$V_{CC}-1.145$		$V_{CC}-0.895$	V
V_{OL}	Output LOW Voltage		$V_{CC}-1.945$		$V_{CC}-1.695$	V
V_{IH}	Input HIGH Voltage		$V_{CC}-1.225$		$V_{CC}-0.88$	V
V_{IL}	Input LOW Voltage		$V_{CC}-1.945$		$V_{CC}-1.625$	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range	Note 5	$V_{EE}+1.2$		V_{CC}	V
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH}$			150	μA
I_{IL}	Input LOW Current (IN)	$V_{IN} = V_{IL}$	0.5			μA
	Input LOW Current (/IN)	$V_{IN} = V_{IL}$	–150			μA

Notes:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package Thermal Resistance values assume exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
4. This circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. V_{IHCMR} (min) varies 1:1 with V_{EE} , (max) varies 1:1 with V_{CC} .

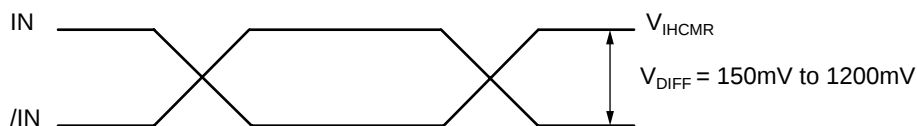
AC ELECTRICAL CHARACTERISTICS (6)

$V_{CC} = +2.5V \pm 5\%$ or $+3.3V \pm 10\%$ or $+5.0V \pm 10\%$ and $V_{EE} = 0V$; $V_{CC} = 0V$ and $V_{EE} = -2.5V \pm 5\%$ or $-3.3V \pm 10\%$ or $-5.0V \pm 10\%$;
 $R_L = 50\Omega$ to $V_{CC} - 2V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.

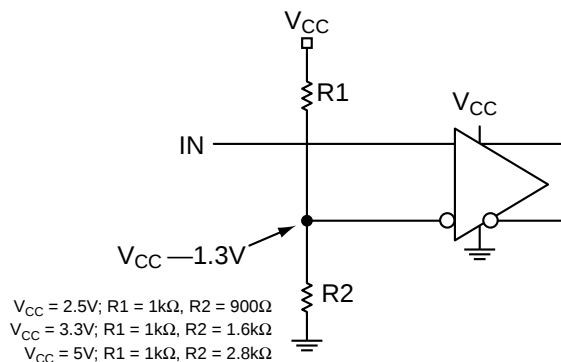
Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Toggle Frequency		3			GHz
t_{pd}	Propagation Delay (Differential) IN to Q, /Q IN to Q, /Q	$V_{CC} = 3.3V/5V$	140	220	300	ps
		$V_{CC} = 2.5V$	170	240	360	ps
t_{SKEW}	Within-Device Skew Q, /Q	Note 7		5	20	ps
	Part-to-Part Skew	$V_{CC} = 3.3V/5V$, Note 7 $V_{CC} = 2.5V$, Note 7			150 120	ps ps
t_{JITTER}	Cycle-to-Cycle Jitter (rms)				1	ps _(rms)
V_{DIFF}	Input Swing	Note 8	150	800	1200	mV
t_r, t_f	Output Rise/Fall Time (20% to 80%)		70	120	200	ps

Notes:

6. Measured with 750mV input signal, 50% duty cycle. V_{DIFF_OUT} is $\geq 400mV$.
7. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
8. See "Input Waveform."

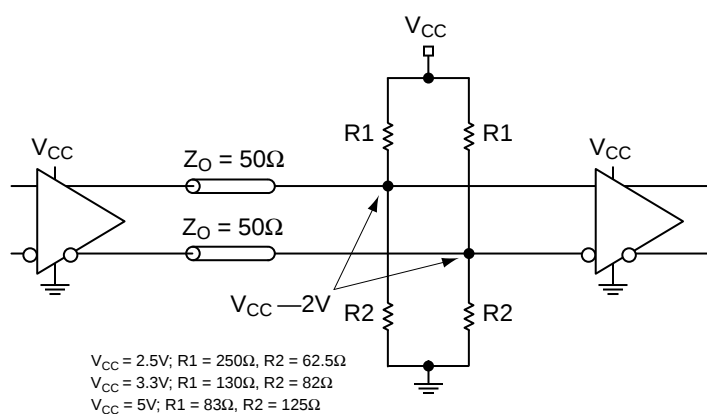
INPUT WAVEFORM

INPUT INTERFACE APPLICATIONS

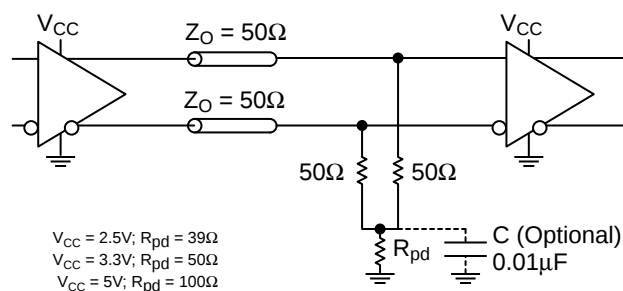


**Figure 1. Single-Ended Input
(Terminating unused input)**

LVPECL OUTPUT INTERFACE APPLICATIONS



**Figure 2a. Parallel Thevenin-Equivalent
Termination**



**Figure 2b. Three Resistor
"Y Termination"**

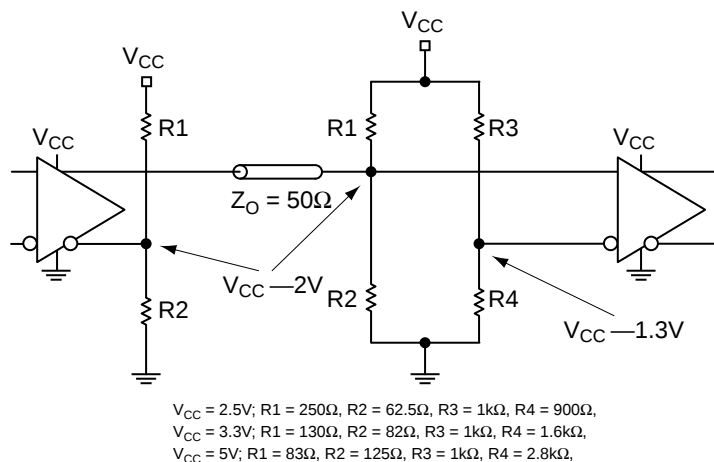
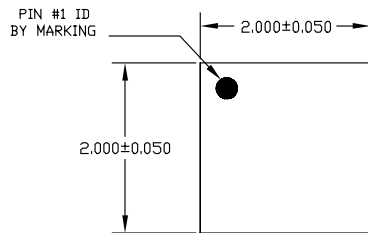
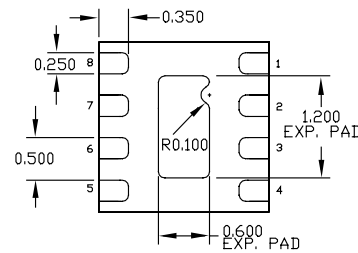


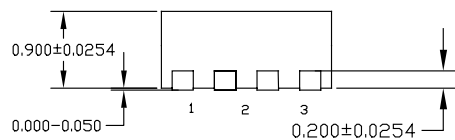
Figure 2c. Terminating Unused I/O

8 LEAD ULTRA-SMALL EPAD-MicroLeadFrame™ (MLF-8)

TOP VIEW

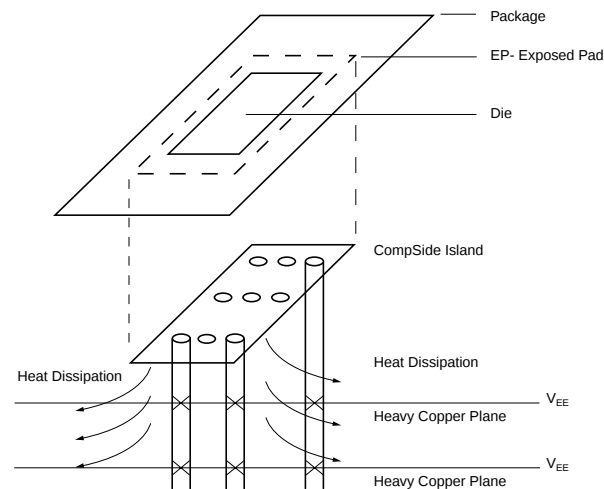


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. MAX. PACKAGE WARPAGE IS 0.05 mm.
 3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
 4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

**PCB Thermal Consideration for 8-Pin MLF™ Package****Package Notes:**

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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