



5V/3.3V PROGRAMMABLE FREQUENCY SYNTHESIZER (25MHz to 400MHz)

ClockWorks™
SY89429V

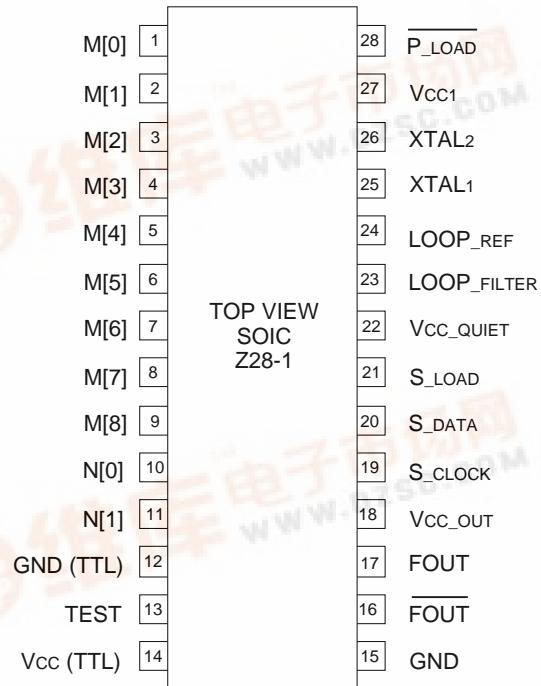
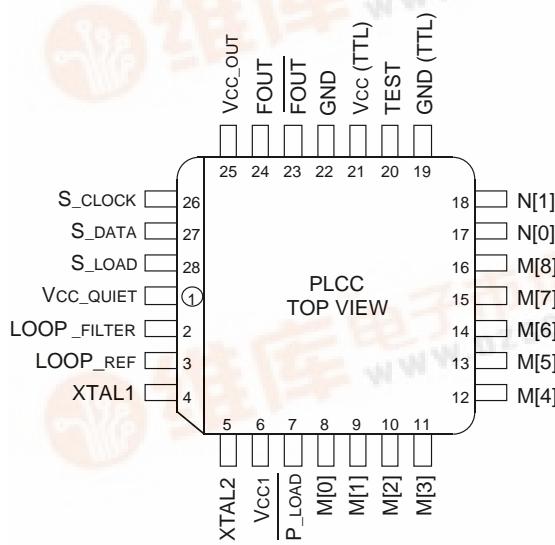
FEATURES

- 3.3V and 5V power supply options
- 25MHz to 400MHz differential PECL outputs
- $\pm 25\text{ps}$ peak-to-peak output jitter
- Minimal frequency over-shoot
- Synthesized architecture
- Serial 3 wire interface
- Parallel interface for power-on
- Internal quartz reference oscillator driven by quartz crystal
- External loop filter optimizes performance/cost
- Applications note (AN-07) for ease of design-ins
- Available in 28-pin PLCC and SOIC packages

DESCRIPTION

The SY89429V is a general purpose, synthesized clock source targeting applications that require both serial and parallel interfaces. Its internal VCO will operate over a range of frequencies from 400MHz to 800MHz. The differential PECL output can be configured to be the VCO frequency divided by 2, 4, 8 or 16. With the output configured to divide the VCO frequency by 2, and with a 16MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 1MHz steps.

PIN CONFIGURATION

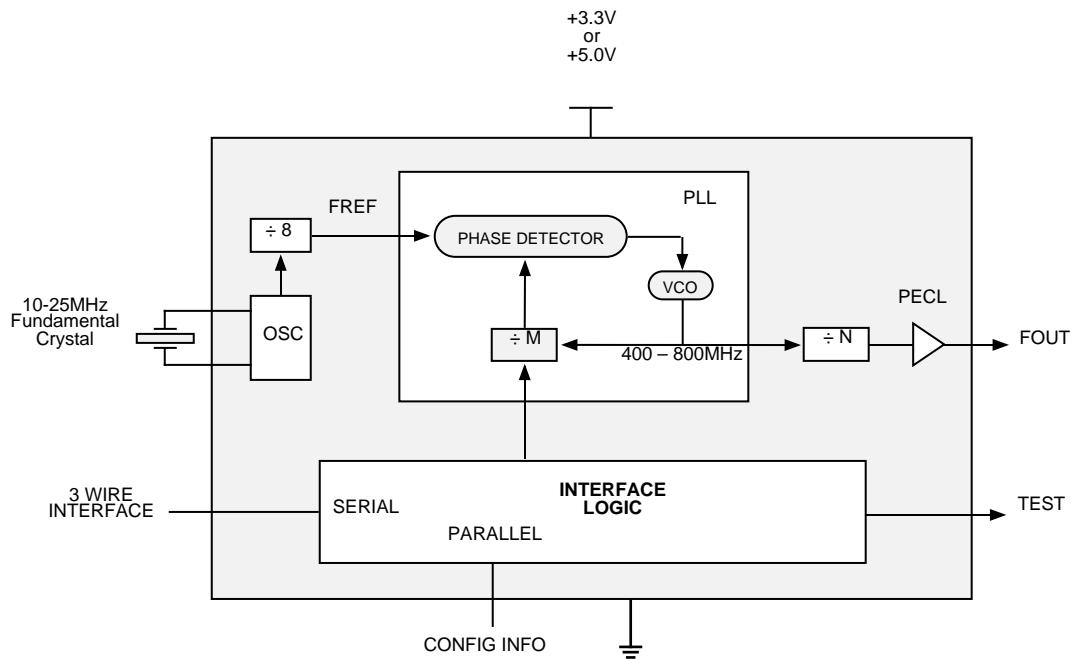


APPLICATIONS

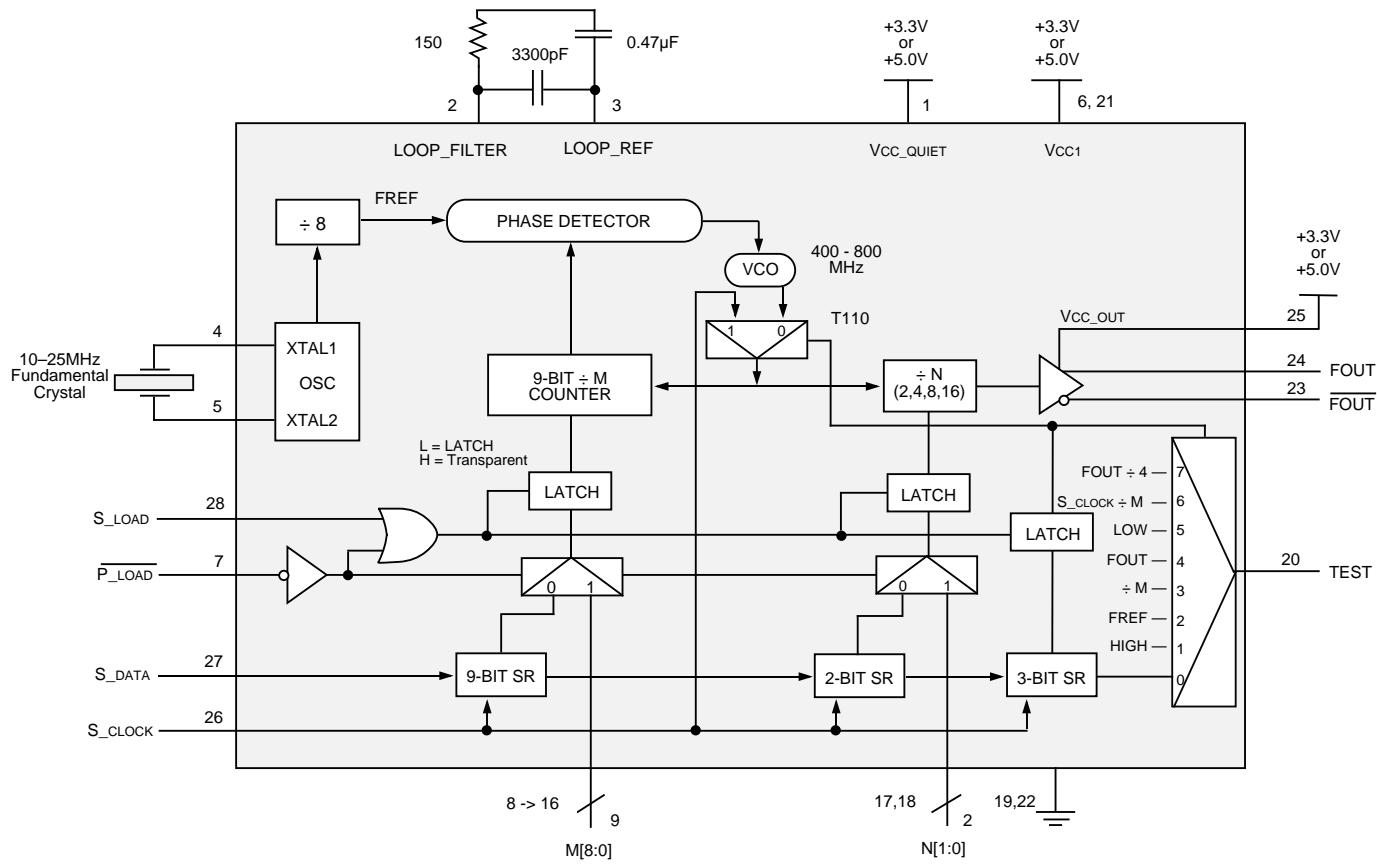
- Workstations
- Advanced communications
- High end consumer
- High-performance computing
- RISC CPU clock
- Graphics pixel clock
- Test equipment
- Other high performance processor-based applications



BLOCK DIAGRAM



DETAILED BLOCK DIAGRAM



NOTE:

Pin numbers reference PLCC pinout.

PIN DESCRIPTIONS

INPUTS

XTAL1, XTAL2

These pins form an oscillator when connected to an external crystal. The crystal is series resonant.

S_LOAD

This TTL pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH; thus, the register data must be stable on the HIGH-to-LOW transition of S_LOAD for proper operation.

S_DATA

This TTL pin is the input to the serial configuration shift registers.

S_CLOCK

This TTL pin clocks the serial configuration shift registers. On the rising edge of this signal, data from S_DATA is sampled.

P_LOAD

This TTL pin loads the configuration latches with the contents of the parallel inputs. The latches will be transparent when this signal is LOW; thus, the parallel data must be stable on the LOW-to-HIGH transition of P_LOAD for proper operation.

M[8:0]

These TTL pins are used to configure the PLL loop divider. They are sampled on the LOW-to-HIGH transition of P_LOAD. M[8] is the MSB, M[0] is the LSB. The binary count on the M pins equates to the divide-by value for the PLL.

N[1:0]

These TTL pins are used to configure the output divider modulus. They are sampled on the LOW-to-HIGH transition of P_LOAD.

OUTPUTS

FOUT, FOUT

These differential positive-referenced ECL signals (PECL) are the output of the synthesizer.

TEST

The function of this TTL output is determined by the serial configuration bits T[2:0].

POWER

Vcc1

This is the positive supply for the chip and is normally connected to +3.3V or +5.0V.

Vcc_OUT

This is the positive reference for the PECL outputs, FOUT and FOUT. It is constrained to be less than or equal to VCC1.

Vcc QUIET

This is the positive supply for the PLL and should be as noise-free as possible for low-jitter operation.

GND

These pins are the negative supply for the chip and are normally all connected to ground.

OTHER

LOOP FILTER

This is an analog I/O pin that provides the loop filter for the PLL.

LOOP REF

This is an analog I/O pin that provides a reference voltage for the PLL.

N[1:0]	Output Division
0 0	2
0 1	4
1 0	8
1 1	16

WITH 16MHZ INPUT

VCO Frequency (MHz)	M Count	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
400	200	0	1	1	0	0	1	0	0	0
402	201	0	1	1	0	0	1	0	0	1
404	202	0	1	1	0	0	1	0	1	0
406	203	0	1	1	0	0	1	0	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
794	397	1	1	0	0	0	1	1	0	1
796	398	1	1	0	0	0	1	1	1	0
798	399	1	1	0	0	0	1	1	1	1
800	400	1	1	0	0	1	0	0	0	0

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter		Value	Unit
Vcc	Power Supply Voltage		-0.5 to +7.0	V
VI	Input Voltage		-0.5 to +7.0	V
I _{OUT}	Output Source Continuous Surge		50 100	mA
T _{store}	Storage Temperature		-65 to +150	°C
T _A	Operating Temperature		-0 to +75	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by eight before being sent to the phase detector. With a 16MHz crystal, this provides a reference frequency of 2MHz.

The VCO within the PLL operates over a range of 400-800MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and loop filter force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock. External loop filter components are utilized to allow for optimal phase jitter performance.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. The output divider is configured through either the serial or the parallel interfaces and can provide one of four divider ratios (2, 4, 8 or 16). This divider extends the performance of the part while providing a 50% duty cycle.

The output driver is driven differentially from the output divider and is capable of driving a pair of transmission lines terminated

in 50Ω to Vcc - 2 volts. The positive reference for the output driver is provided by a dedicated power pin (V_{CC_OUT}) to reduce noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. Normally upon system reset, the P_{_LOAD} input is held LOW until sometime after power becomes valid. With S_{_LOAD} held LOW, on the LOW-to-HIGH transition of P_{_LOAD}, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pull-up resistors are provided on the M[8:0] and N[1:0] inputs to reduce component count.

The serial interface logic is implemented with a 14-bit shift register scheme. The register shifts once per rising edge of the S_{_CLOCK} input. The serial input S_{_DATA} must meet set-up and hold timing as specified in the AC parameters section of this data sheet. With P_{_LOAD} held HIGH, the configuration latches will capture the value in the shift register on the HIGH-to-LOW edge of the S_{_LOAD} input. See the programming section for more information.

The TEST output reflects various internal node values and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.

PROGRAMMING INTERFACE

Programming the device is accomplished by properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can be represented by this formula:

$$F_{OUT} = \left(\frac{F_{XTAL}}{8} \right) \times \frac{M}{N}$$

Where F_{XTAL} is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $200 \leq M \leq 400$ for a 16MHz input reference.

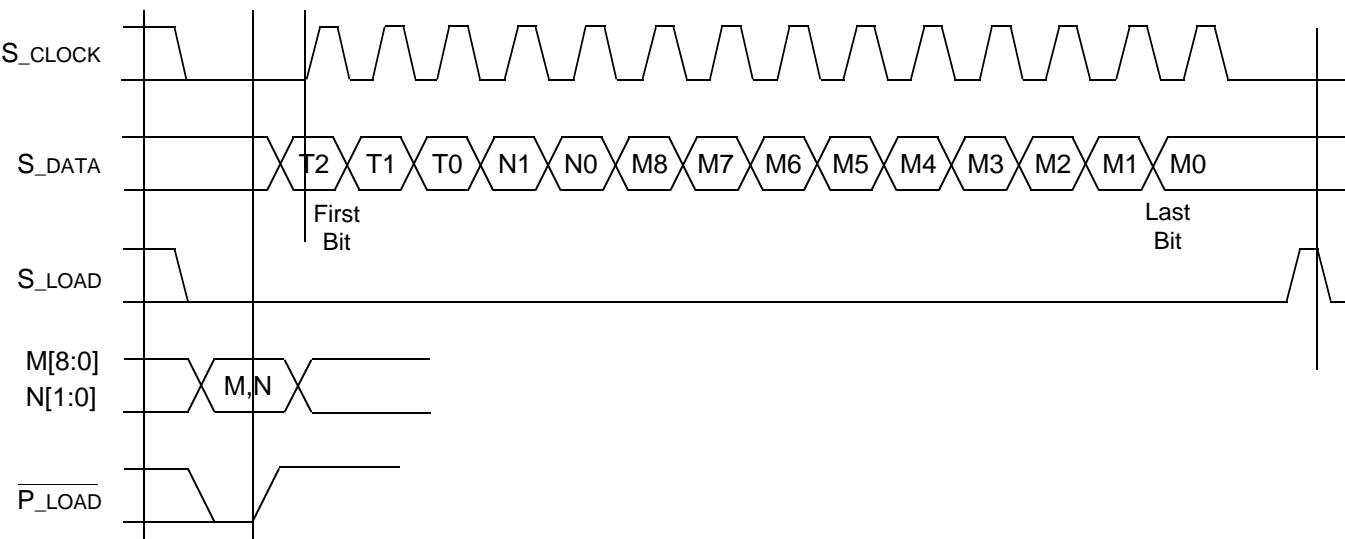
$M[8:0]$ and $N[1:0]$ are normally specified once at power-on, through the parallel interface, and then possibly again through the serial interface. This approach allows the designer to bring up the application at one frequency and then change or fine-tune the clock, as the ability to control the serial interface becomes available. To minimize transients in the frequency domain, the output should be varied in the smallest step size possible.

T2	T1	T0	TEST	FOUT / FOUT
0	0	0	Data Out – Last Bit SR	$F_{VCO} \div N$
0	0	1	HIGH	$F_{VCO} \div N$
0	1	0	FREF	$F_{VCO} \div N$
0	1	1	M Counter Output	$F_{VCO} \div N$
1	0	0	FOUT	$F_{VCO} \div N$
1	0	1	LOW	$F_{VCO} \div N$
1	1	0	$S_{CLOCK} \div M$	$S_{CLOCK} \div N$
1	1	1	$F_{OUT} \div 4$	$F_{VCO} \div N$

The TEST output provides visibility for one of several internal nodes (as determined by the T[1:0] bits in the serial configuration stream). It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the TTL output may not be able to toggle fast enough for some of the higher output frequencies. The T2, T1, T0 configuration latches are preset to 000 when P_{LOAD} is low, so that the FOUT outputs are as jitter-free as possible. The serial configuration port can be used to select one of the alternate functions for this pin.

The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M8).

When T[2:0] is set to 100 the SY89429V is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree (See detailed Block Diagram). Because the S_CLOCK is a TTL level the input frequency is limited to 250MHz or less. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 125MHz as the minimum divide ratio of the N counter is 2. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.



100H ECL DC ELECTRICAL CHARACTERISTICS

VCC1 = VCC QUIET = VCC TTL = VCC OUT = +3.3V to +5.0V ±5%; TA = 0°C to +75°C

Symbol	Parameter	Min.	Max.	Unit	Condition
VOH	Output HIGH Voltage	VCC_OUT -1.075	VCC_OUT -0.830	V	50Ω to VCC_OUT -2V
VOL	Output LOW Voltage	VCC_OUT -1.860	VCC_OUT -1.570	V	50Ω to VCC_OUT -2V

TTL DC ELECTRICAL CHARACTERISTICS

VCC1 = VCC QUIET = VCC TTL = VCC OUT = +3.3V to +5.0V ±5%; TA = 0°C to +75°C

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +75°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
VIH	Input HIGH Voltage	2.0	—	2.0	—	2.0	—	V	—
VIL	Input LOW Voltage	—	0.8	—	0.8	—	0.8	V	—
IIH	Input HIGH Current	—	50	—	50	—	50	µA	VIN = 2.7V
IIL	Input LOW Current	—	-0.6	—	-0.6	—	-0.6	mA	VIN = 0.5V
V _{IK}	Input Clamp Voltage	—	-1.2	—	-1.2	—	-1.2	V	IIN = -12mA
VOH	Output HIGH Voltage	—	2.0	—	2.0	—	2.0	V	IOH = -2.0mA
VOL	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	IOL = 8mA
I _{OS}	Output Short Circuit Current	-100 (Typ.)		-100 (Typ.)		-100 (Typ.)		mA	V _{OUT} = 0V
I _{CC1}	Supply Current	—	190	—	190	—	190	mA	5.0V ±5%
		0.89X of 5V Val.		0.89X of 5V Val.		0.89X of 5V Val.		mA	3.3V ±5%
	Typical % of I _{CC1}	V _{CC1}	33%	V _{CC_OUT}	33%	V _{CC QUIET}	33%		
		V _{CC1}	9%	V _{CC_OUT}	9%	V _{CC QUIET}	9%		
		V _{CC1}	14%	V _{CC_OUT}	14%	V _{CC QUIET}	14%		
		V _{CC1}	44%	V _{CC_OUT}	44%	V _{CC QUIET}	44%		

AC ELECTRICAL CHARACTERISTICS

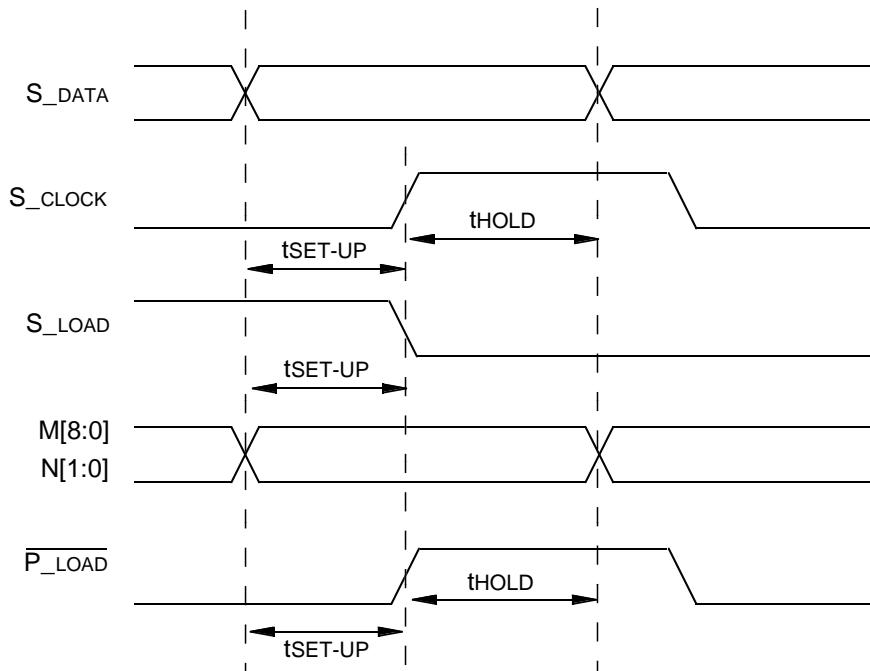
VCC1 = VCC QUIET = VCC TTL = VCC OUT = +3.3V to +5.0V ±5%; TA = 0°C to +75°C

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +75°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f _{MAXI}	Maximum Input Frequency ⁽¹⁾ S_CLOCK Xtal Oscillator	— 10	10 25	— 10	10 25	— 10	10 25	MHz	Fundamental Cyrstal
f _{MAXO}	Maximum Output Frequency VCO (Internal) F _{OUT}	400 25	800 400	400 25	800 400	400 25	800 400	MHz	
t _{LOCK}	Maximum PLL Lock Time	—	10	—	10	—	10	ms	
t _{jitter}	Cycle-to-Cycle Jitter (Peak-toPeak)	—	±25	—	±25	—	±25	ps	Test output static
t _S	Setup Time S _{_DATA} to S _{_CLOCK} S _{_CLOCK} to S _{_LOAD} M, N to P _{_LOAD}	20 20 20	— 20 20	20 — 20	— 20 20	20 — 20	— 20 —	ns	
t _H	Hold Time S _{_DATA} to S _{_CLOCK} S _{_CLOCK} to S _{_LOAD} M, N to P _{_LOAD}	20 20 20	— 20 20	20 — 20	— 20 20	20 — 20	— 20 —	ns	
t _{pw(MIN)}	Minimum Pulse Width S _{_LOAD} P _{_LOAD}	50 50	— 50	50 —	— 50	50 —	— 50	ns	
t _{DC}	F _{OUT} Duty Cycle	45	55	45	55	45	55	%	
t _r t _f	Output Rise/Fall 20% to 80%	F _{OUT}	300	800	300	800	300	800	ps

NOTE:

1. 10MHz is the maximum frequency to load the feedback divide registers. S_CLOCK can be switched at high frequencies when used as a test clock in TEST MODE 6.

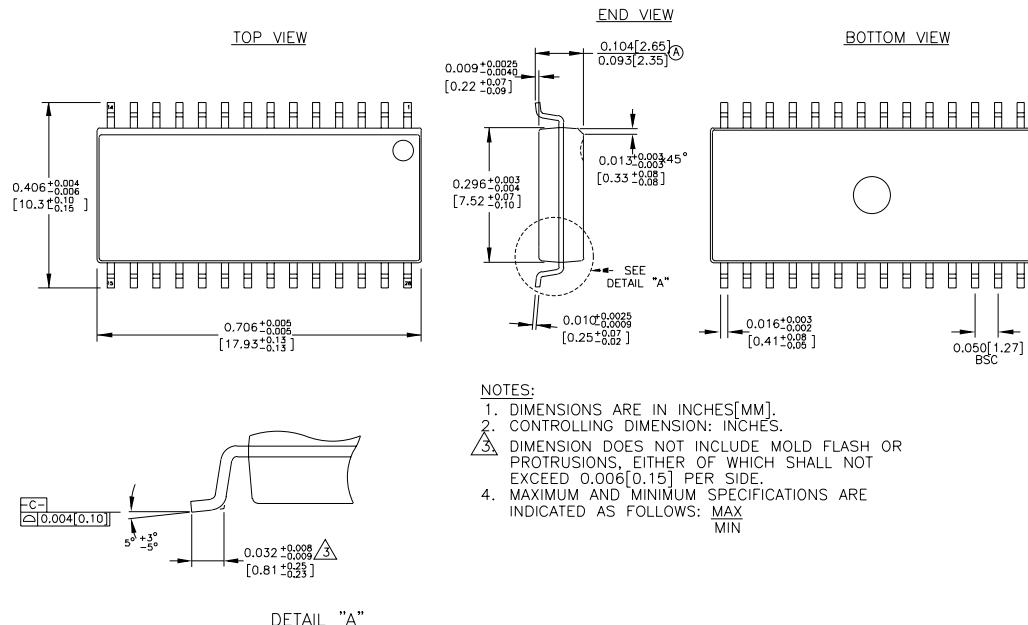
TIMING DIAGRAM



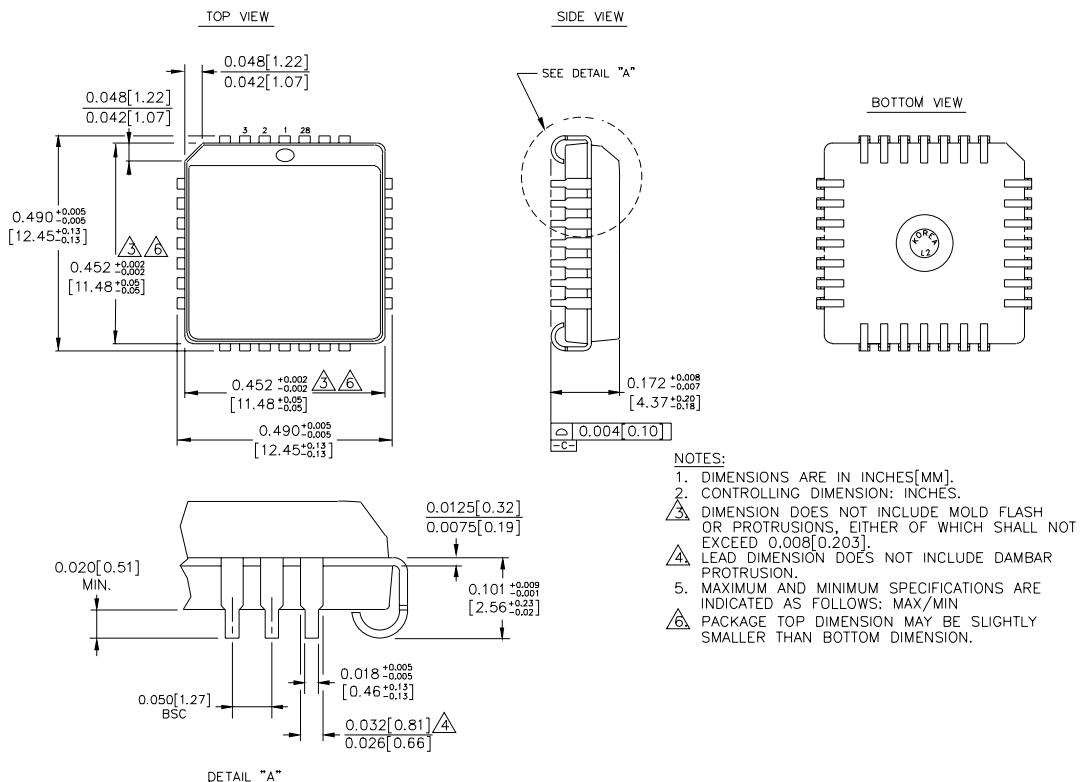
PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY89429VJC	J28-1	Commercial
SY89429VJCTR	J28-1	Commercial
SY89429VZC	Z28-1	Commercial
SY89429VZCTR	Z28-1	Commercial

28 LEAD SOIC .300" WIDE (Z28-1)



28 LEAD PLCC (J28-1)



Rev. 03

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