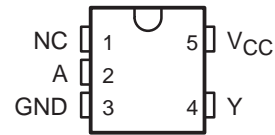


# SN74AHCT1G14 SINGLE SCHMITT-TRIGGER INVERTER GATE

SCLS322K – MARCH 1996 – REVISED JANUARY 2000

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Inputs Are TTL-Voltage Compatible**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline Transistor (DBV, DCK) Packages**

DBV OR DCK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description

The SN74AHCT1G14 contains a single inverter gate. The device performs the Boolean function  $Y = \bar{A}$ .

The device functions as an independent inverter gate, but because of the Schmitt action, gates may have different input threshold levels for positive- ( $V_{T+}$ ) and negative-going ( $V_{T-}$ ) signals.

The SN74AHCT1G14 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



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 **TEXAS  
INSTRUMENTS**

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# SN74AHCT1G14

## SINGLE SCHMITT-TRIGGER INVERTER GATE

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	347°C/W
DCK package	389°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5.5	V
$V_I$ Input voltage	0	5.5	V
$V_O$ Output voltage	0	$V_{CC}$	V
$I_{OH}$ High-level output current		–8	mA
$I_{OL}$ Low-level output current		8	mA
$T_A$ Operating free-air temperature	–40	85	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{T+}$ Positive-going input threshold voltage		4.5 V	0.9		2	0.9	2	V
		5.5 V	1.1		2	1.1	2	
$V_{T-}$ Negative-going input threshold voltage		4.5 V	0.5		1.6	0.5	1.6	V
		5.5 V	0.6		1.5	0.6	1.5	
$\Delta V_T$ Hysteresis ( $V_{T+} - V_{T-}$ )		4.5 V	0.4		1.4	0.4	1.4	V
		5.5 V	0.5		1.6	0.4	1.6	
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4	4.5		4.4		V
	$I_{OH} = -8 \text{ mA}$		3.94			3.8		
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1	V
	$I_{OL} = 8 \text{ mA}$				0.36		0.44	
$I_I$	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1		±1	μA
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μA
$C_i$	$V_I = V_{CC}$ or GND	5 V		2	10		10	pF



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**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF	4	7	7	1	8	ns
t <sub>PHL</sub>				4	7	7	1	8	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF	5.5	8	8	1	9	ns
t <sub>PHL</sub>				5.5	8	8	1	9	

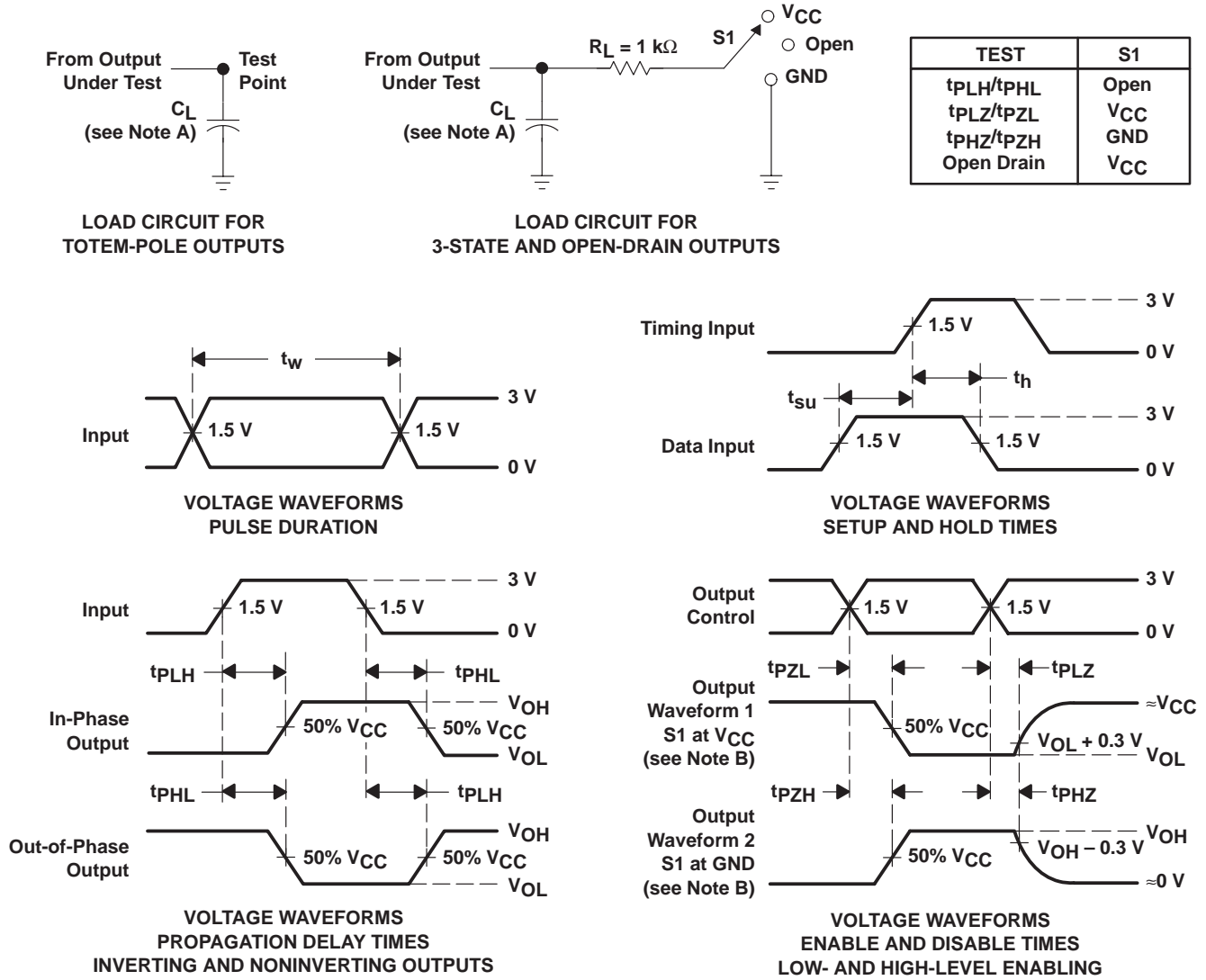
**operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	No load, f = 1 MHz	12	pF

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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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