DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT534

Octal D-type flip-flop; positive edge-trigger; 3-state; inverting

Product specification
Supersedes data of September 1993
File under Integrated Circuits, IC06

1998 Apr 10

Philips Semiconductors

Octal D-type flip-flop; positive edge-trigger; 3-state; inverting

74HC/HCT534

FEATURES

- 3-state inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- Output capability: bus driver
- I_{CC} category: MSI.

GENERAL DESCRIPTION

The 74HC/HCT534 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT534 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition. When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The “534” is functionally identical to the “374”, but has inverted outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay CP to $\overline{Q}_n$	C_L = 15 pF; V_{CC} = 5 V	12	13	ns
f_{max}	maximum clock frequency		61	40	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	19	19	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz.

   f_o = output frequency in MHz.

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

   C_L = output load capacitance in pF.

   V_{CC} = supply voltage in V.
2. For HC the condition is V_I = GND to V_{CC}; for HCT the condition is V_I = GND to V_{CC} − 1.5 V.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
74HC534	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HC534	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HCT534	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HCT534	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1

Octal D-type flip-flop; positive edge-trigger; 3-state; inverting

74HC/HCT534

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$\overline{Q}_0$ to $\overline{Q}_7$	3-state outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

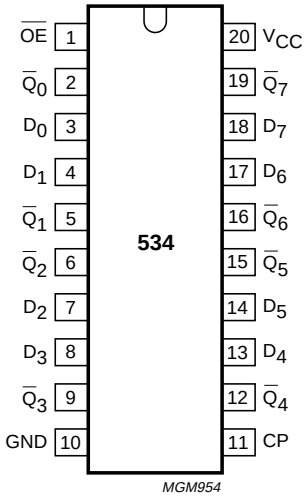


Fig.1 Pin configuration.

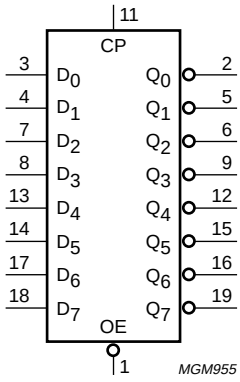


Fig.2 Logic symbol.

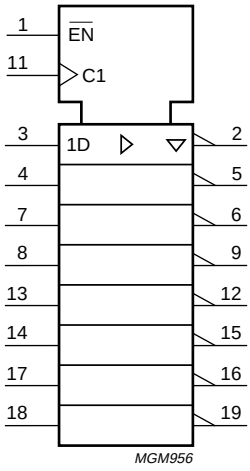


Fig.3 IEC logic symbol.

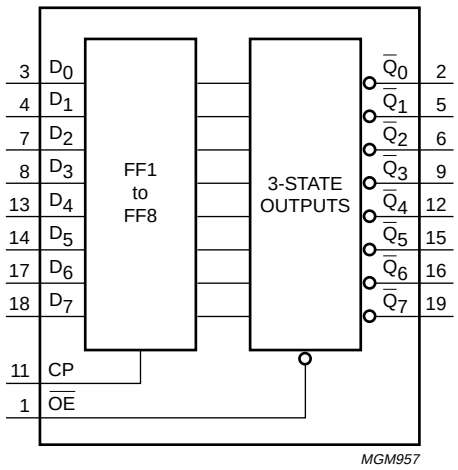


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		$\overline{Q}_0$ to $\overline{Q}_7$
load and read register	L	↑	l	L	H
	L	↑	h	H	L
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

Note

1. H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
   L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
   Z = high impedance OFF-state; ↑ = LOW-to-HIGH clock transition.

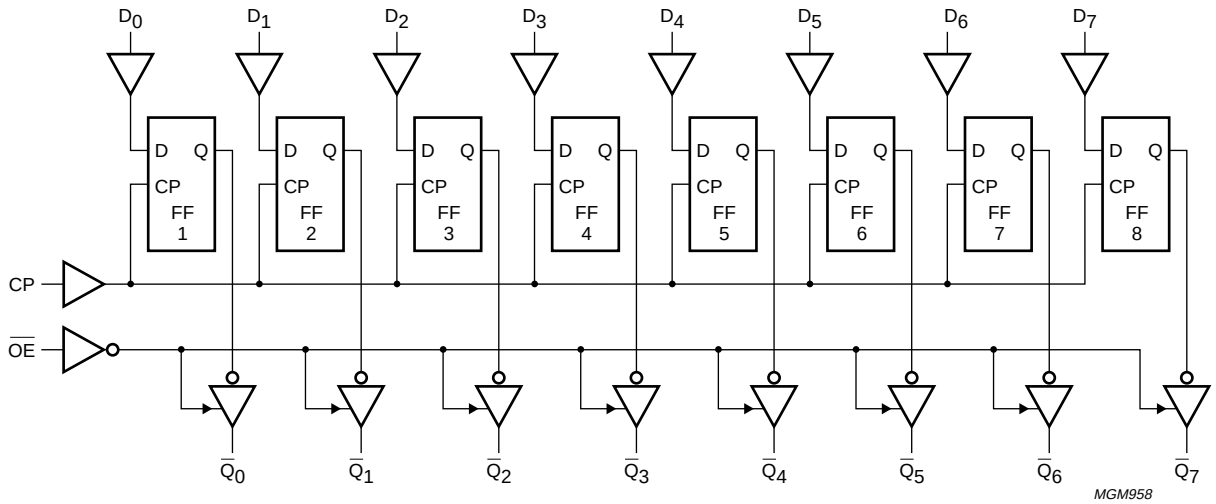


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver I_{CC} category: MSI.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nCP to n$\overline{Q}_n$		41	165		205		250	ns	2.0	Fig.6
			15	33		41		50		4.5	
			12	28		35		43		6.0	
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$		33	150		190		225	ns	2.0	Fig.7
			12	30		38		45		4.5	
			10	26		33		38		6.0	
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$		41	150		190		225	ns	2.0	Fig.7
			15	30		38		45		4.5	
			12	26		33		38		6.0	
t_{THL}/ t_{TLH}	output transition time		14	60		75		90	ns	2.0	Fig.6
			5	12		15		18		4.5	
			4	10		13		15		6.0	
t_W	clock pulse width HIGH or LOW	80	19		100		120		ns	2.0	Fig.6
		16	7		20		24			4.5	
		14	6		17		20			6.0	
t_{su}	set-up time D_n to CP	60	6		75		90		ns	2.0	Fig.8
		12	2		15		18			4.5	
		10	2		13		15			6.0	
t_h	hold time D_n to CP	5	−3		5		5		ns	2.0	Fig.8
		5	−1		5		5			4.5	
		5	−1		5		5			6.0	
f_{max}	maximum clock pulse frequency	6.0	18		4.8		4.0		MHz	2.0	Fig.6
		30	55		24		20			4.5	
		35	66		28		24			6.0	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver I_{CC} category: MSI.

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

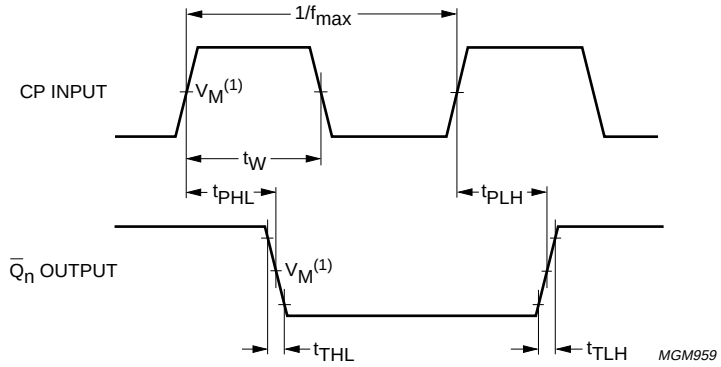
INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}$	1.25
CP	0.90
D_n	0.35

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

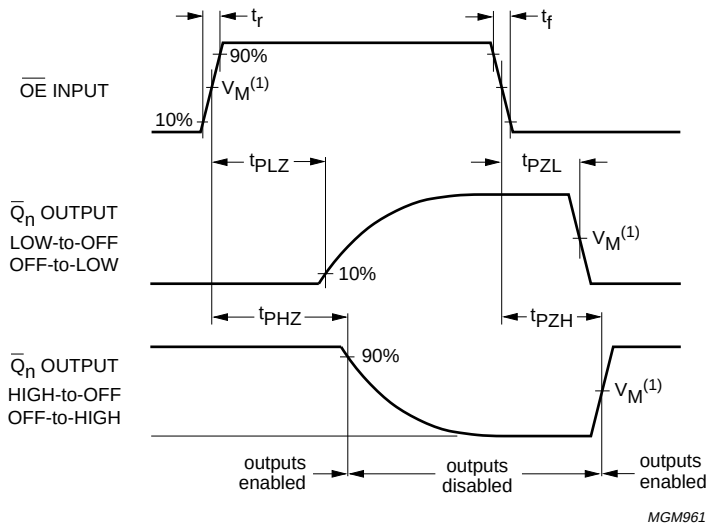
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to $\overline{Q}_n$		16	30		38		45	ns	4.5	Fig.6
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$		16	30		38		45	ns	4.5	Fig.7
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$		18	30		38		45	ns	4.5	Fig.7
t_{THL}/ t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6
t_W	clock pulse width HIGH or LOW	23	14		29		35		ns	4.5	Fig.6
t_{su}	set-up time D_n to CP	12	4		15		18		ns	4.5	Fig.8
t_h	hold time D_n to CP	5	−1		5		5		ns	4.5	Fig.8
f_{max}	maximum clock pulse frequency	22	36		18		15		MHz	4.5	Fig.6

AC WAVEFORMS



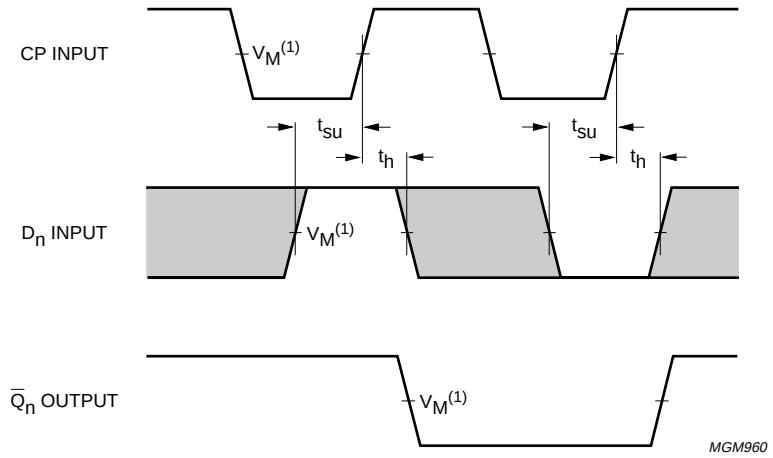
(1) HC: V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the clock (CP) to output ($\overline{Q}_n$) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.



(1) HC: V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the 3-state enable and disable times.



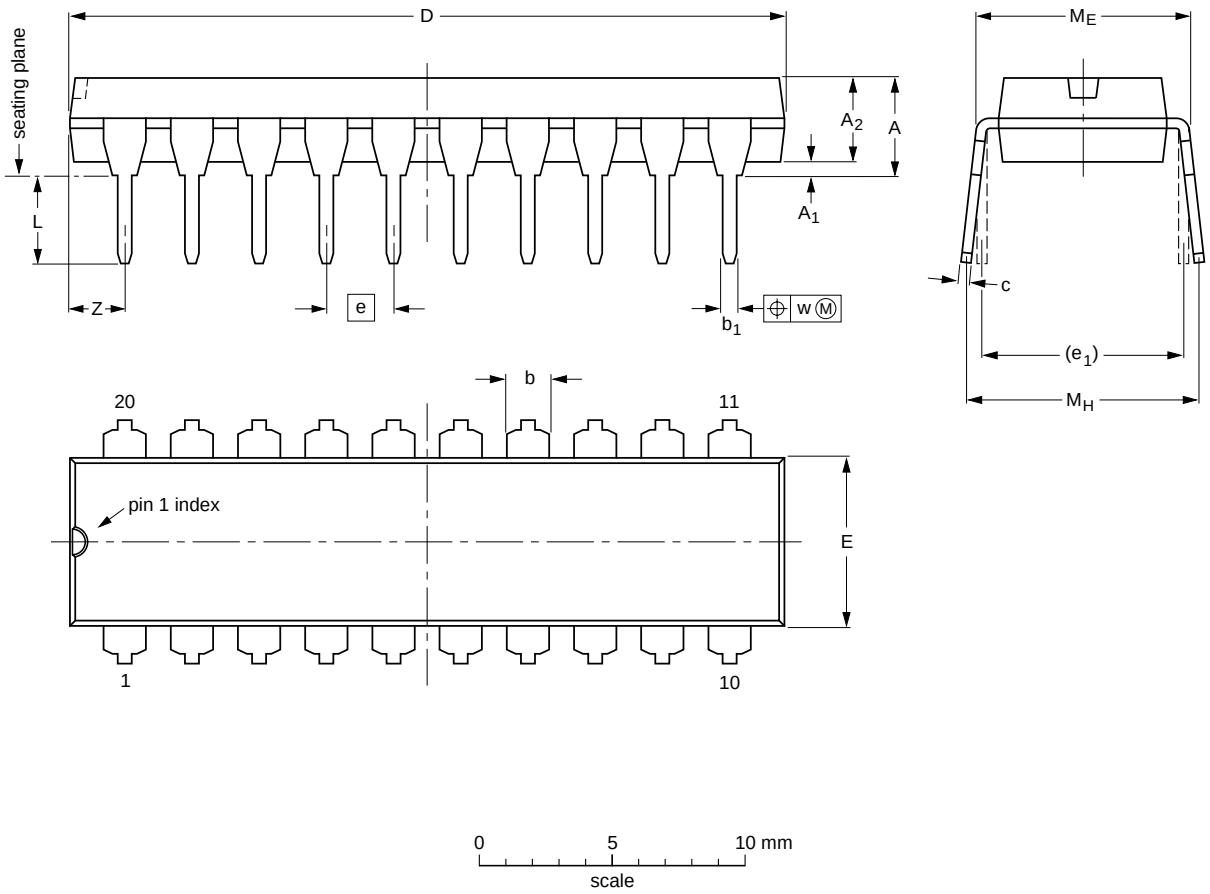
The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC: V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the data set-up and hold times for D_n input.

PACKAGE OUTLINES

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

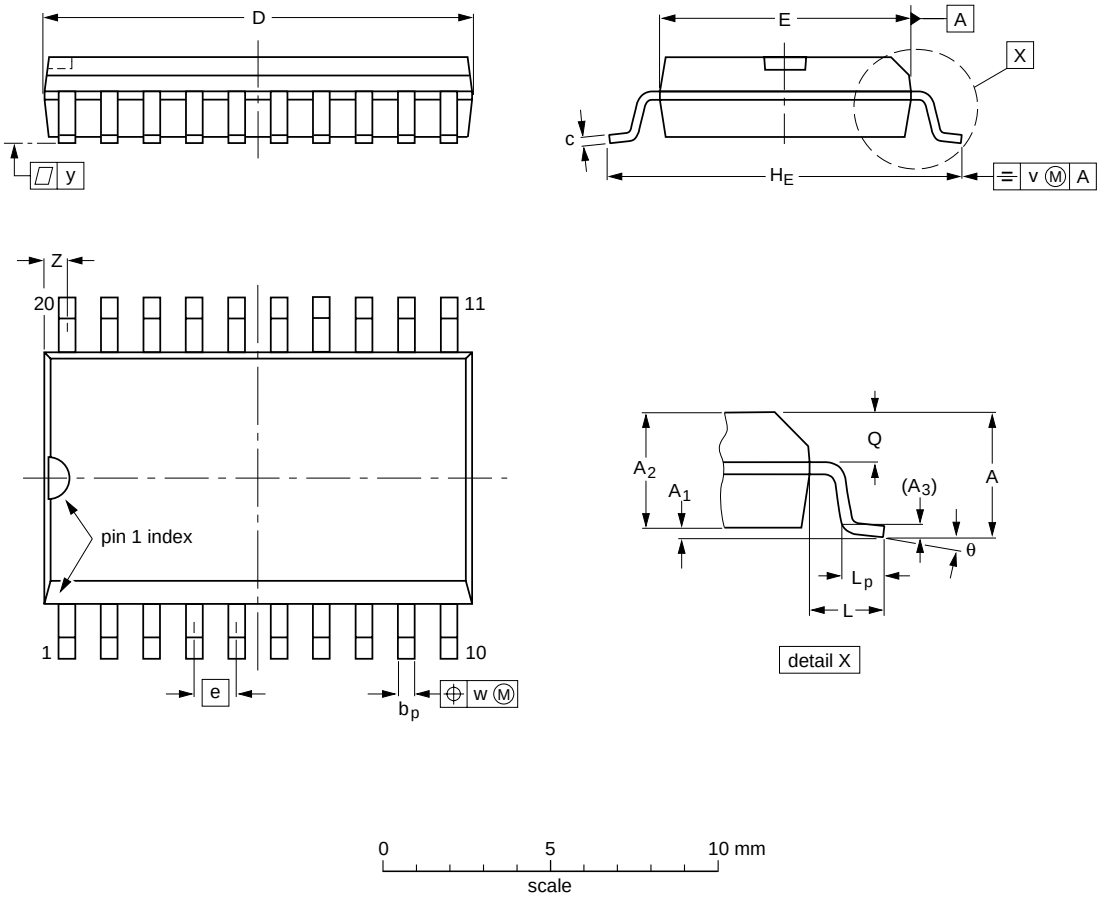
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.