
HD74HCT373/HD74HCT533

Octal D-type Transparent Latches (with 3-state outputs)/
Octal D-type Transparent Latches (with inverted 3-state outputs)

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Description

When the latch enable input is high, the Q outputs of HD74HCT373 will follow the D inputs and the Q outputs of HD74HCT533 will follow the inversion of the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals present at the other inputs and the state of the storage elements.

Features

- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation: t_{pd} (Data to Q) = 14 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 4.5$ to 5.5 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

Function Table

Output Control	Enable G	D	HD74HCT373 Q	HD74HCT533 $\bar{Q}$
L	H	H	H	L
L	H	L	L	H
L	L	X	No change	No change
H	X	X	Z	Z

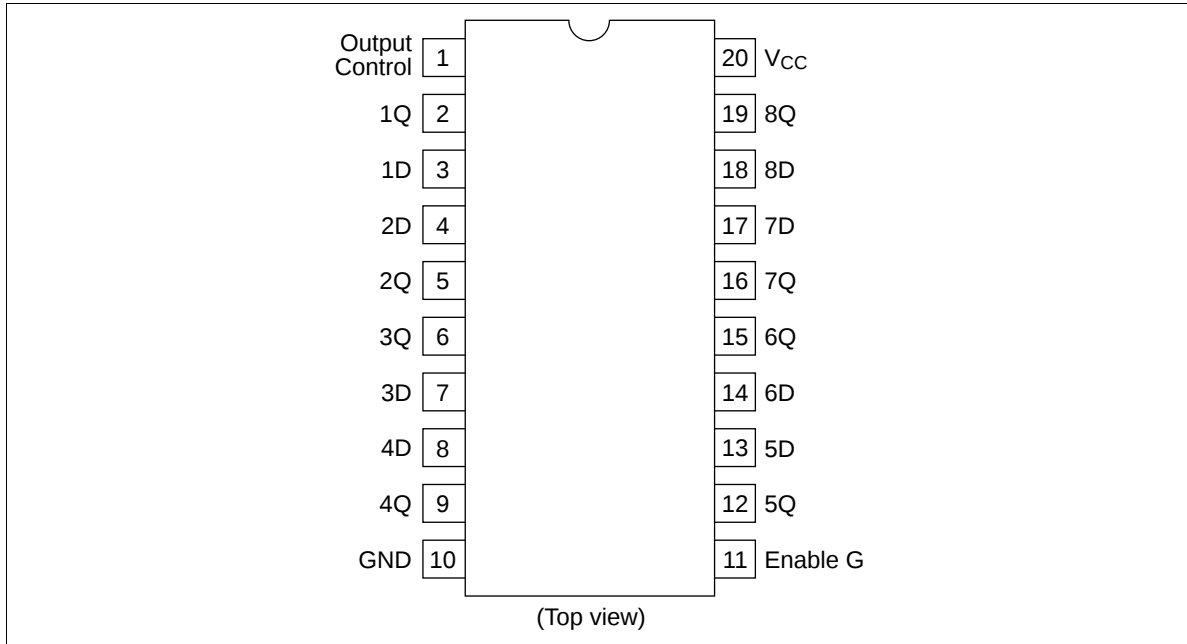
X : Irrelevant

Z : Off (high-impedance) state of a 3-state output.

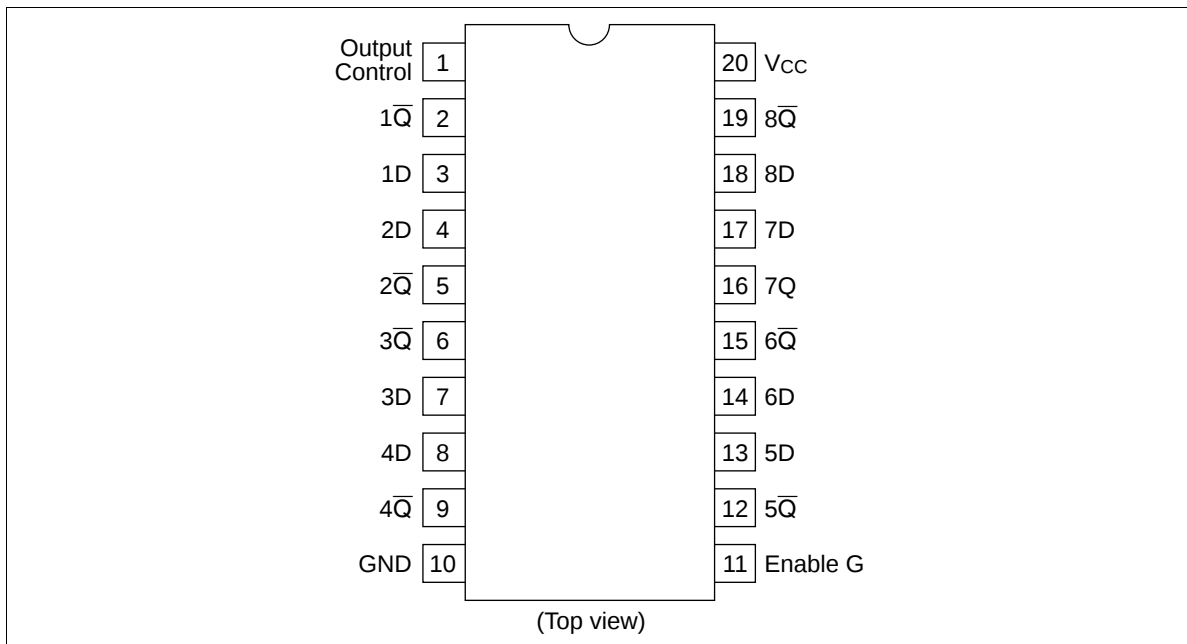
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Pin Arrangement

HD74HCT373



HD74HCT533

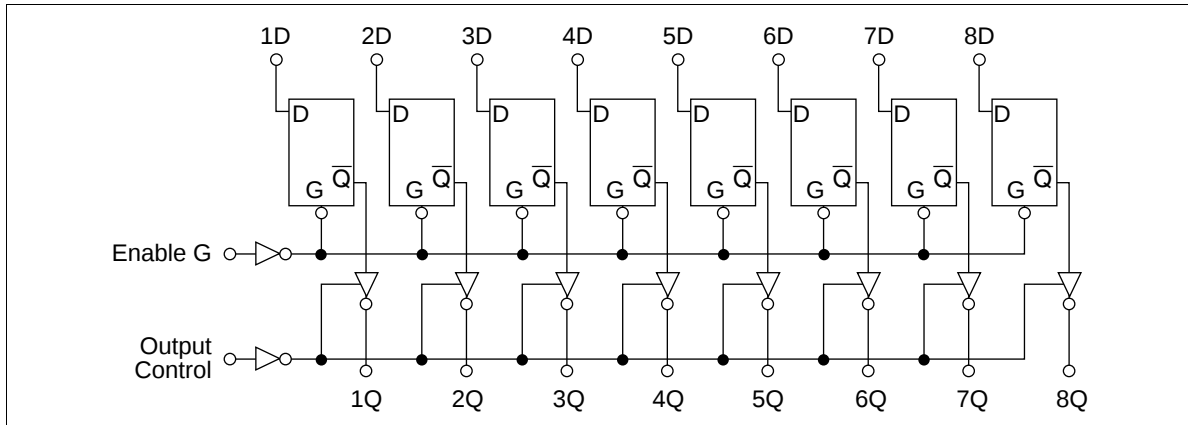


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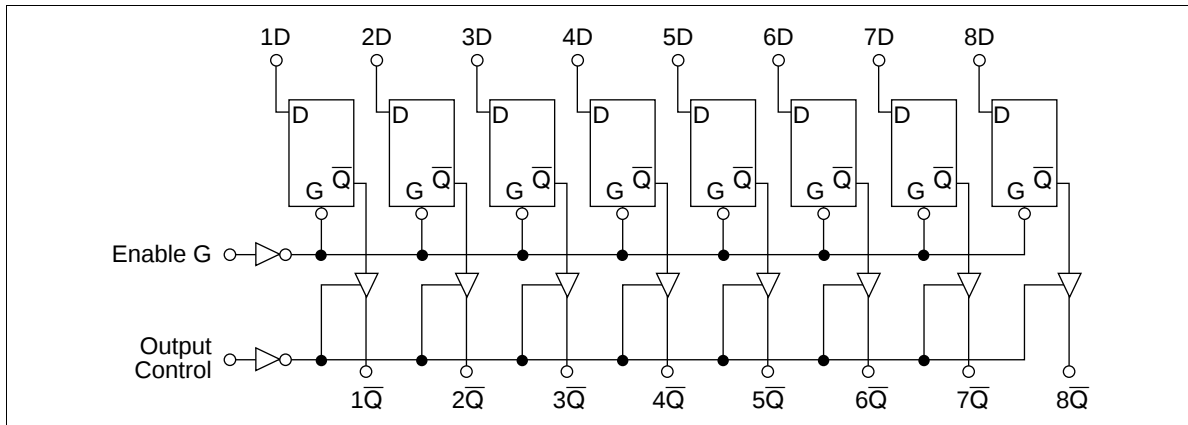
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Block Diagram

HD74HCT373



HD74HCT533



HD74HCT373/HD74HCT533

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
DC current drain per pin	I_{OUT}	± 35	mA
DC current drain per V_{CC} , GND	I_{CC} , I_{GND}	± 75	mA
DC input diode current	I_{IK}	± 20	mA
DC output diode current	I_{OK}	± 20	mA
Power dissipation per package	P_T	500	mW
Storage temperature	Tstg	-65 to +150	°C

DC Characteristics

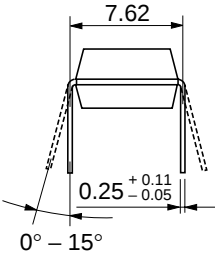
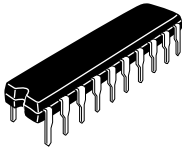
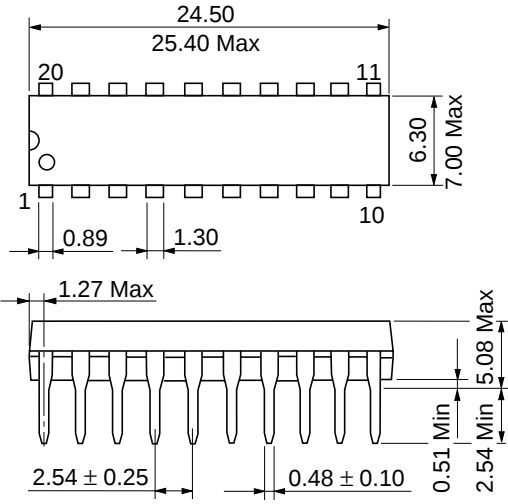
Item	Symbol	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions	
		Min	Typ	Max	Min		V _{CC} (V)	
Input voltage	V_{IH}	2.0	—	—	2.0	—	V	4.5 to 5.5
	V_{IL}	—	—	0.8	—	0.8	V	4.5 to 5.5
Output voltage	V_{OH}	4.4	—	—	4.4	—	V	4.5 Vin = V_{IH} or V_{IL} $I_{OH} = -20 \mu A$
		4.18	—	—	4.13	—		4.5 $I_{OH} = -6 mA$
	V_{OL}	—	—	0.1	—	0.1	V	4.5 Vin = V_{IH} or V_{IL} $I_{OL} = 20 \mu A$
		—	—	0.26	—	0.33		4.5 $I_{OL} = 6 mA$
Off-state output current	I_{OZ}	—	—	± 0.5	—	± 5.0	μA	5.5 Vin = V_{IH} or V_{IL} , Vout = V_{CC} or GND
Input current	I_{in}	—	—	± 0.1	—	± 1.0	μA	5.5 Vin = V_{CC} or GND
Quiescent current	I_{CC}	—	—	4.0	—	40	μA	5.5 Vin = V_{CC} or GND, Iout = 0 μA

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AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

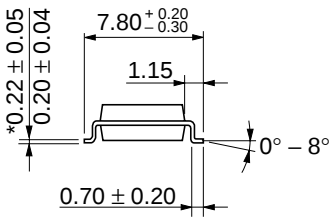
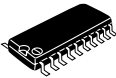
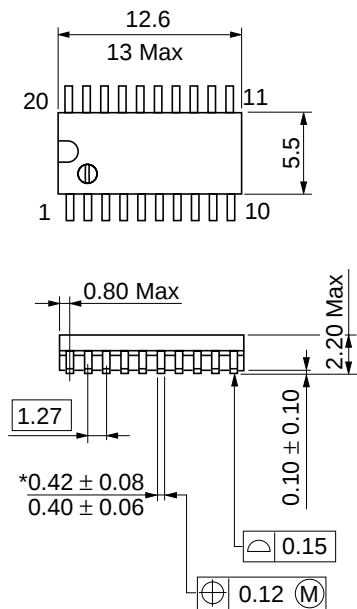
Item	Symbol	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions	
		Min	Typ	Max	Min	Max	V _{CC} (V)	
Propagation delay	t_{PLH}	—	13	30	—	38	ns	4.5
time	t_{PHL}	—	16	30	—	38		4.5
	t_{PLH}	—	14	25	—	31	ns	4.5
	t_{PHL}	—	12	25	—	31		4.5
Output enable	t_{ZL}	—	16	30	—	38	ns	4.5
time	t_{ZH}	—	15	30	—	38		4.5
Output disable	t_{LZ}	—	14	30	—	38	ns	4.5
time	t_{HZ}	—	16	30	—	38		4.5
Setup time	t_{su}	20	—	—	25	—	ns	4.5
Hold time	t_h	10	—	—	13	—	ns	4.5
Pulse width	t_w	16	—	—	20	—	ns	4.5
Output rise/fall	t_{TLH}	—	4	12	—	15	ns	4.5
time	t_{THL}	—	—	—	—	—	—	—
Input capacitance	C _{in}	—	5	10	—	10	pF	—

Unit: mm



Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g

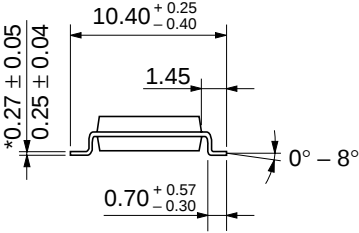
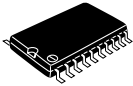
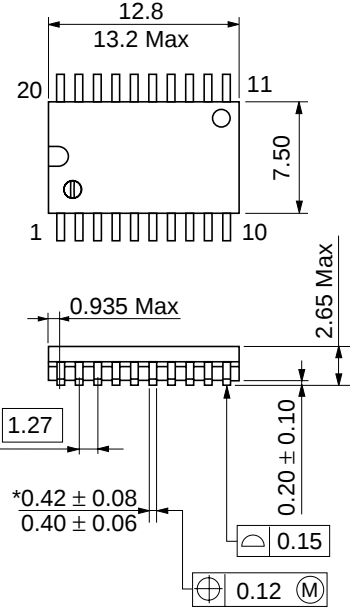
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g

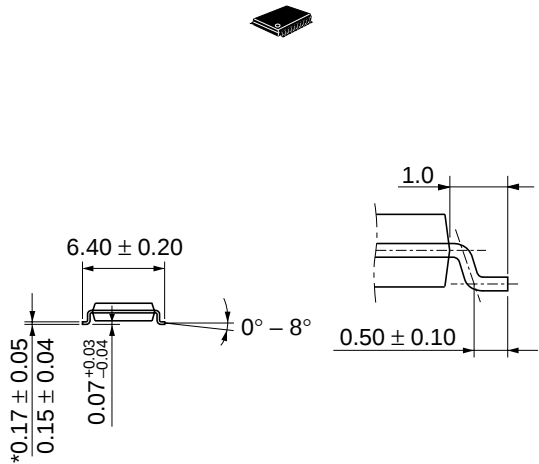
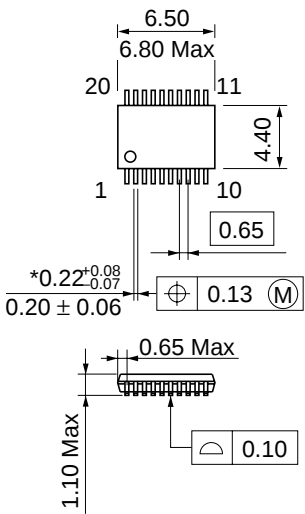
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g

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