

DATA SHEET

74AHC595; 74AHCT595

8-bit serial-in/serial or parallel-out
shift register with output latches;
3-state

Product specification
File under Integrated Circuits, IC06

2000 Mar 15

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

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FEATURES

- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V
CDM EIA/JESD22-C101 exceeds 1000 V
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- For AHC only: operates with CMOS input levels
- For AHCT only: operates with TTL input levels
- Specified from -40 to $+85$ °C and from -40 to $+125$ °C.

APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register.

DESCRIPTION

The 74AHC/AHCT595 are high-speed Si-gate CMOS devices and are pin compatible with Low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74AHC/AHCT595 is an 8-stage serial shift register with a storage register and 3-state outputs. The shift register has separate clocks.

Data is shifted on the positive-going transitions of the SH_{CP} input. The data in each register is transferred to the storage register on a positive-going transition of the ST_{CP} input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (D_S) and a serial standard output (Q_7') for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input (\overline{OE}) is LOW.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC	AHCT	
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q_7'	$C_L = 15$ pF; $V_{CC} = 5$ V	4.0	3.8	ns
	ST_{CP} to Q_n		4.2	4.0	ns
	\overline{MR} to Q_7'		4.4	4.6	ns
C_I	input capacitance		3.0	3.0	pF
f_{max}	maximum clock frequency		170	170	MHz
C_{PD}	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; notes 1, 2 and 3	180	190	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in Volts.
2. The condition is $V_I = GND$ to V_{CC} .
3. All 9 outputs switching.

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FUNCTION TABLE

See note 1.

INPUT					OUTPUT		FUNCTION
SH _{CP}	ST _{CP}	\overline{OE}	\overline{MR}	D _S	Q ₇ '	Q _n	
X	X	L	L	X	L	NC	a LOW level on \overline{MR} only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear. Parallel outputs in high impedance OFF-state.
↑	X	L	H	H	Q ₆ '	NC	logic HIGH level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q ₆ ') appears on the serial output (Q ₇ ').
X	↑	L	H	X	NC	Q _n '	contents of shift register stages (internal Q _n ') are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q ₆ '	Q _n '	contents of shift register shifted through. Previous contents of the shift register is transferred to the storage register and the parallel output stages.

Note

1. H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH transition;
↓ = HIGH-to-LOW transition;
X = don't care;
NC = no change;
Z = high impedance OFF-state.

ORDERING INFORMATION

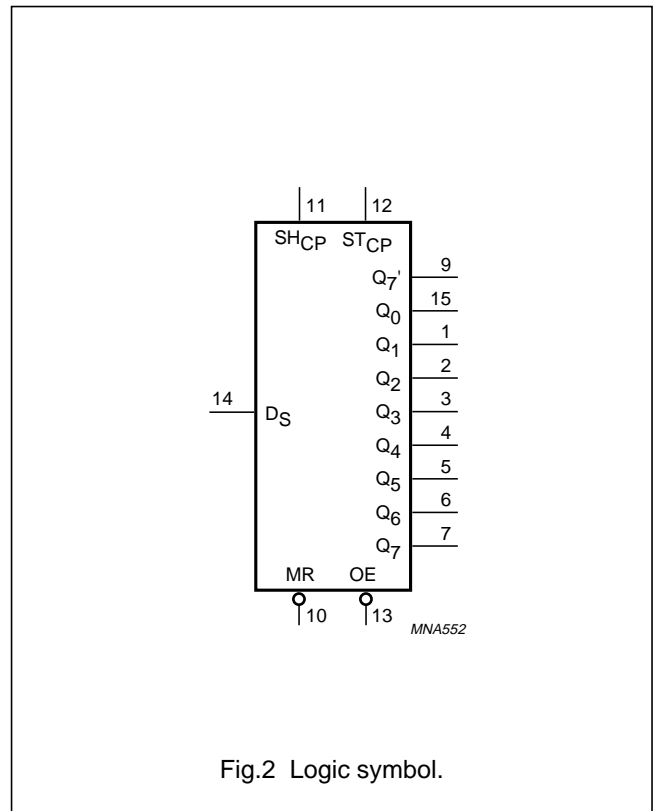
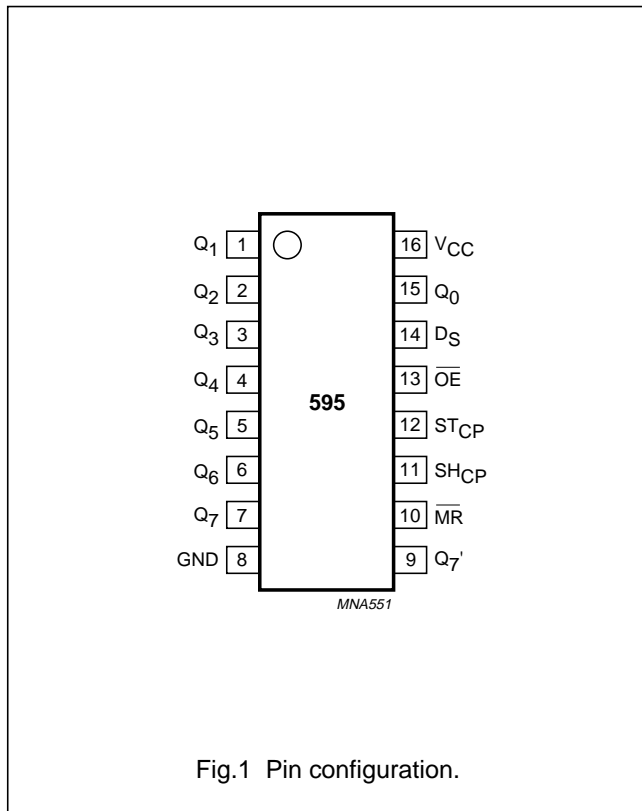
TYPE NUMBER	PACKAGES				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74AHC595D	-40 to +125 °C	16	SO	plastic	SOT109-1
74AHC595PW		16	TSSOP	plastic	SOT403-1
74AHCT595D		16	SO	plastic	SOT109-1
74AHCT595PW		16	TSSOP	plastic	SOT403-1

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PINNING

PIN	SYMBOL	DESCRIPTION
1, 2, 3, 4, 5, 6, 7 and 15	$Q_1, Q_2, Q_3, Q_4, Q_5, Q_6, Q_7$ and Q_0	parallel data output
8	GND	ground (0 V)
9	Q_7'	serial data output
10	\overline{MR}	master reset (active LOW)
11	SH_{CP}	shift register clock input
12	ST_{CP}	storage register clock input
13	\overline{OE}	output enable input (active LOW)
14	D_S	serial data input
16	V_{CC}	DC supply voltage



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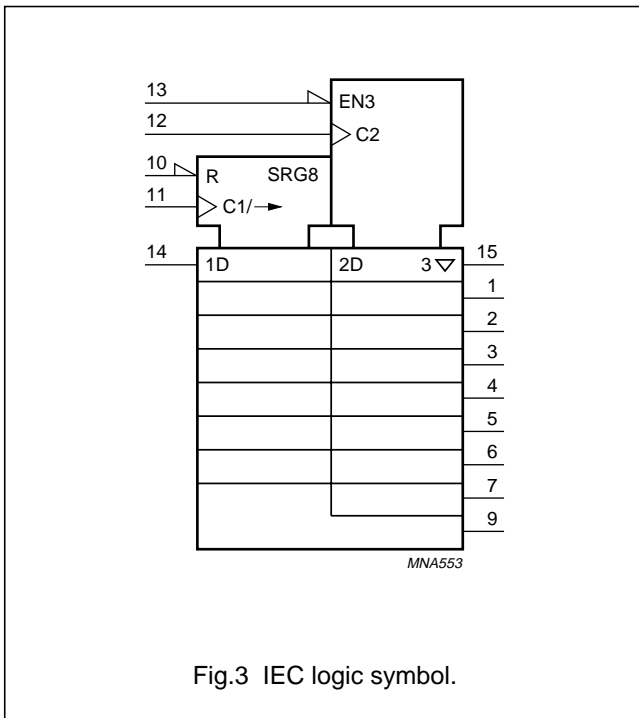


Fig.3 IEC logic symbol.

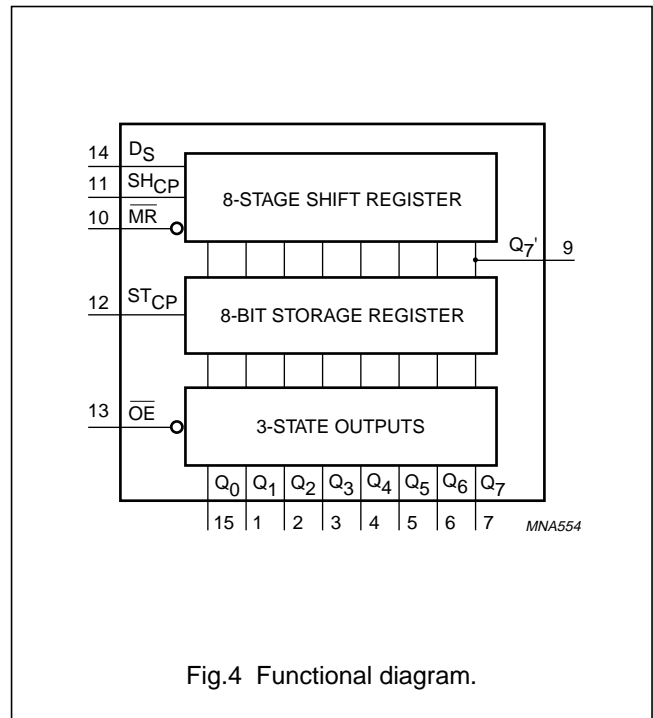


Fig.4 Functional diagram.

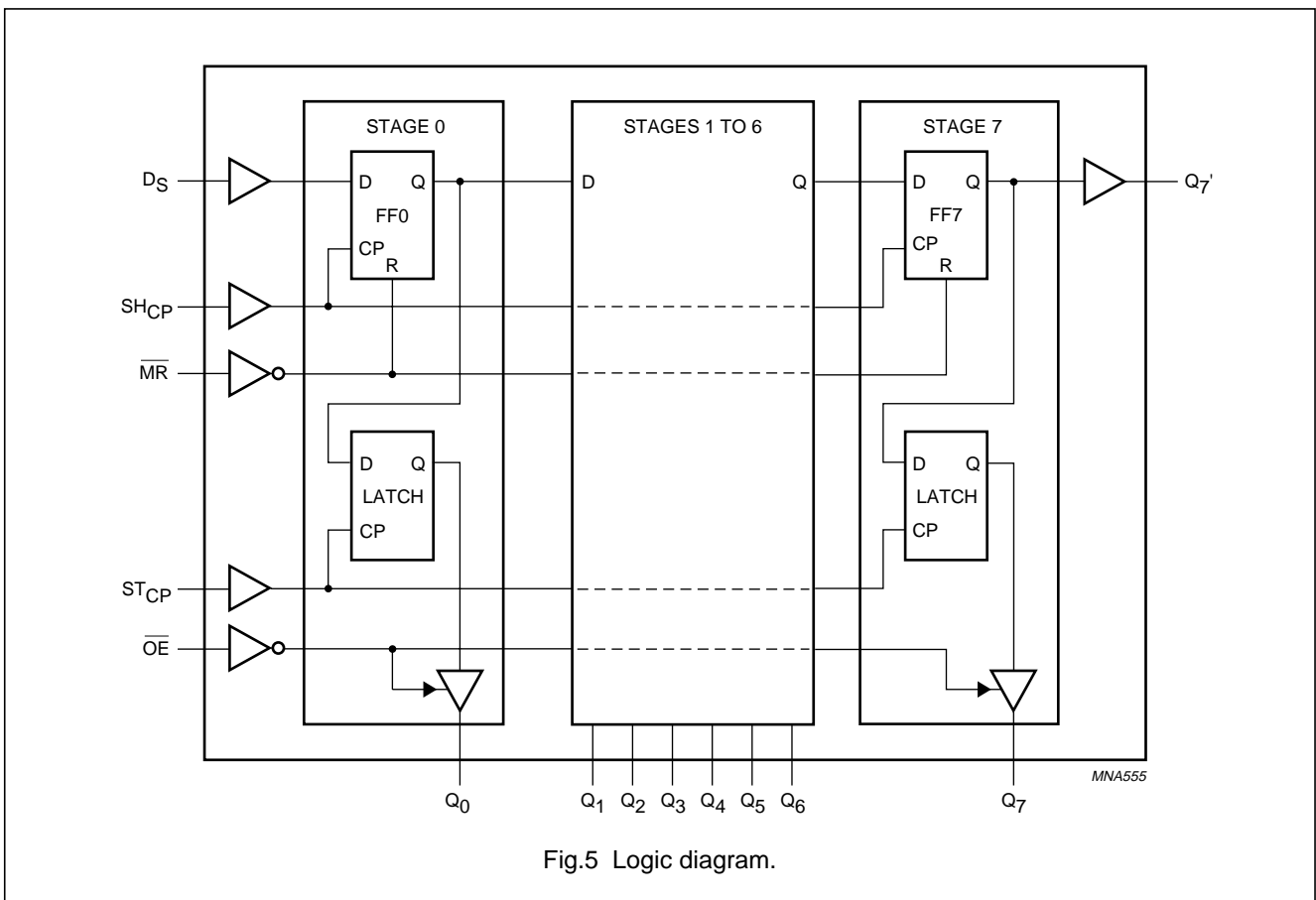
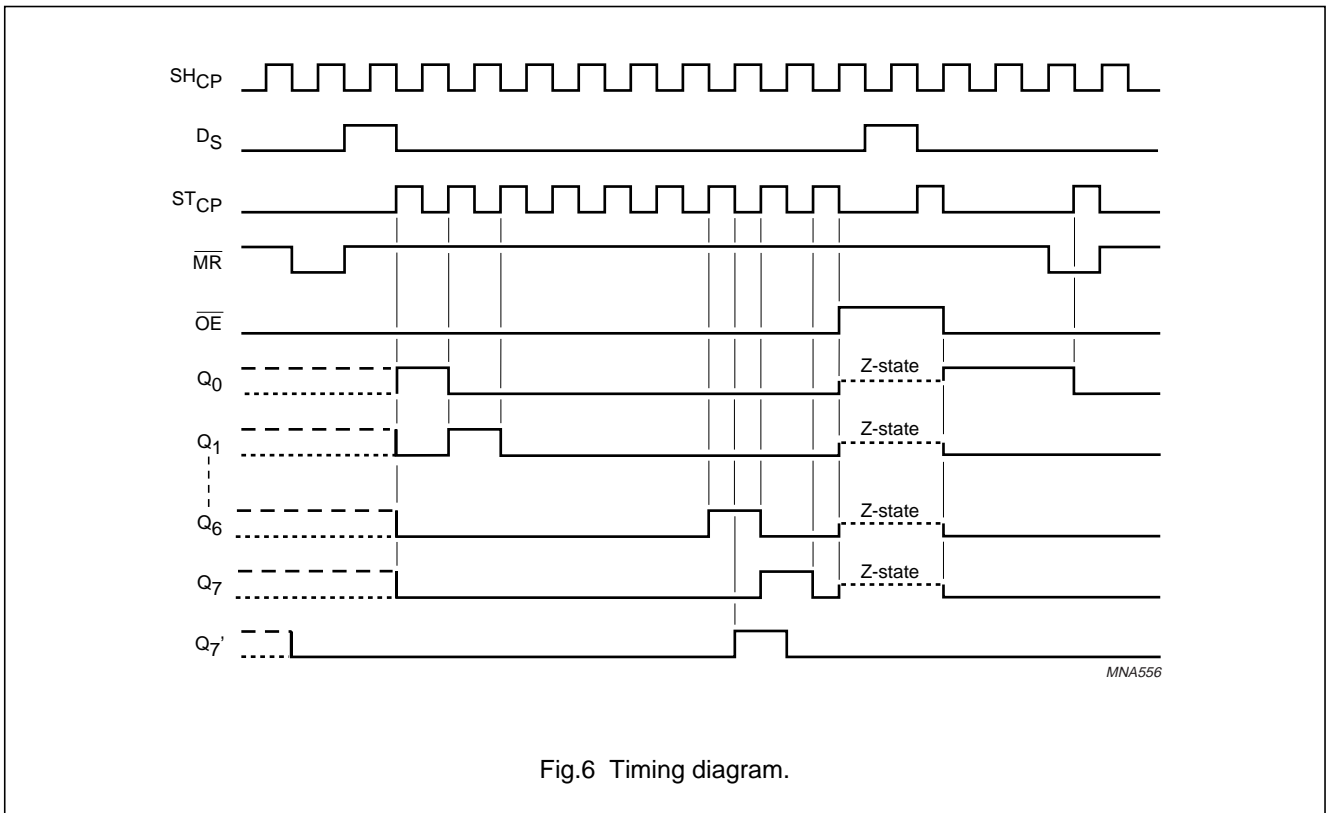


Fig.5 Logic diagram.

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

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8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC			74AHCT			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	DC supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	–	5.5	0	–	5.5	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C
			–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall ratios ($\Delta t/\Delta V$)	$V_{CC} = 3.3 \pm 0.3$ V	–	–	100	–	–	–	ns/V
		$V_{CC} = 5 \pm 0.5$ V	–	–	20	–	–	20	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_{IK}	DC input diode current	$V_I < -0.5$ V; note 1	–	–20	mA
I_{OK}	DC output clamping diode current	$-0.5 > V_O > V_{CC} + 0.5$ V; note 1	–	± 20	mA
I_O	DC output sink current	$-0.5 < V_O < V_{CC} + 0.5$ V	–	± 25	mA
I_{CC}	DC V_{CC} or GND current		–	± 75	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range: –40 to +125 °C; note 2	–	500	mW

Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO packages: above 70 °C the value of P_D derates linearly with 8 mW/K.
For TSSOP packages: above 60 °C the value of P_D derates linearly with 5.5 mW/K.

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DC CHARACTERISTICS

74AHC family

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)						UNIT	
		OTHER	V_{CC} (V)	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	1.5	–	1.5	–	V
			3.0	2.1	–	–	2.1	–	2.1	–	V
			5.5	3.85	–	–	3.85	–	3.85	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	–	0.5	–	0.5	V
			3.0	–	–	0.9	–	0.9	–	0.9	V
			5.5	–	–	1.65	–	1.65	–	1.65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $I_O = -50 \mu A$	2.0	1.9	2.0	–	1.9	–	1.9	–	V
			3.0	2.9	3.0	–	2.9	–	2.9	–	V
			4.5	4.4	4.5	–	4.4	–	4.4	–	V
		$V_I = V_{IH}$ or V_{IL} ; $I_O = -4.0$ mA	3.0	2.58	–	–	2.48	–	2.40	–	V
		$V_I = V_{IH}$ or V_{IL} ; $I_O = -8.0$ mA	4.5	3.94	–	–	3.8	–	3.70	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $I_O = 50 \mu A$	2.0	–	0	0.1	–	0.1	–	0.1	V
			3.0	–	0	0.1	–	0.1	–	0.1	V
			4.5	–	0	0.1	–	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL} ; $I_O = 4.0$ mA	3.0	–	–	0.36	–	0.44	–	0.55	V
		$V_I = V_{IH}$ or V_{IL} ; $I_O = 8.0$ mA	4.5	–	–	0.36	–	0.44	–	0.55	V
I_I	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	0.1	–	1.0	–	2.0	μA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND	5.5	–	–	± 0.25	–	± 2.5	–	± 10.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	4.0	–	40	–	80	μA
C_I	input capacitance		–	–	3	10	–	10	–	10	pF

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74AHCT family

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T _{amb} (°C)						UNIT	
		OTHER	V _{CC} (V)	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	2.0	–	2.0	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	–	0.8	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = –50 µA	4.5	4.4	4.5	–	4.4	–	4.4	–	V
		V _I = V _{IH} or V _{IL} ; I _O = –8.0 mA	4.5	3.94	–	–	3.8	–	3.70	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = 50 µA	4.5	–	0	0.1	–	0.1	–	0.1	V
		V _I = V _{IH} or V _{IL} ; I _O = 8.0 mA	4.5	–	–	0.36	–	0.44	–	0.55	V
I _I	input leakage current	V _I = V _{IH} or V _{IL}	5.5	–	–	0.1	–	1.0	–	2.0	µA
I _{oz}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND per input pin; other inputs at V _{CC} or GND; I _O = 0	5.5	–	–	±0.25	–	±2.5	–	±10.0	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	4.0	–	40	–	80	µA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} – 2.1 V other inputs at V _{CC} or GND; I _O = 0	4.5 to 5.5	–	–	1.35	–	1.5	–	1.5	mA
C _I	input capacitance		–	–	3	10	–	10	–	10	pF

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AC CHARACTERISTICS

Type 74AHC595

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)						UNIT	
		WAVEFORMS	C_L	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
$V_{CC} = 3.0$ to 3.6 V; note 1											
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q_7'	see Figs 7 and 12	15 pF	–	5.7	13.0	1.0	15.0	1.0	16.5	ns
	propagation delay ST_{CP} to Q_n	see Figs 8 and 12		–	5.9	11.9	1.0	13.5	1.0	15.0	ns
t_{PHL}	propagation delay \overline{MR} to Q_7'	see Figs 10 and 12		–	5.9	12.8	1.0	13.7	1.0	15.0	ns
t_{PZH}/t_{PZL}	3-state output enable time \overline{OE} to Q_n	see Figs 11 and 12		–	5.6	11.5	1.0	13.5	1.0	15.0	ns
t_{PHZ}/t_{PLZ}	3-state output disable time \overline{OE} to Q_n			–	5.4	11.0	1.0	13.0	1.0	14.5	ns
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q_7'	see Figs 7 and 12	50 pF	–	7.7	16.5	1.0	18.5	1.0	20.1	ns
	propagation delay ST_{CP} to Q_n	see Figs 8 and 12		–	7.7	15.4	1.0	17.0	1.0	18.5	ns
t_{PHL}	propagation delay \overline{MR} to Q_7'	see Figs 10 and 12		–	7.4	16.3	1.0	17.2	1.0	18.7	ns
t_{PZH}/t_{PZL}	3-state output enable time \overline{OE} to Q_n	see Figs 11 and 12		–	7.4	15.0	1.0	17.0	1.0	18.5	ns
t_{PHZ}/t_{PLZ}	3-state output disable time \overline{OE} to Q_n			–	8.7	15.7	1.0	16.2	1.0	17.5	ns
t_W	shift clock pulse width HIGH or LOW	see Figs 7 and 12		5.0	–	–	5.0	–	5.0	–	ns
	storage clock pulse width HIGH or LOW	see Figs 8 and 12		5.0	–	–	5.0	–	5.0	–	ns
	master reset pulse width LOW	see Figs 10 and 12		5.0	–	–	5.0	–	5.0	–	ns
t_{su}	set-up time D_S to SH_{CP}	see Figs 8 and 12		3.5	–	–	3.5	–	3.5	–	ns
	set-up time SH_{CP} to ST_{CP}	see Figs 9 and 12		8.5	–	–	8.5	–	8.5	–	ns
t_h	hold time D_S to SH_{CP}		1.5	–	–	1.5	–	1.5	–	ns	
t_{rem}	removal time \overline{MR} to SH_{CP}	see Figs 10 and 12	3.0	–	–	3.0	–	3.0	–	ns	
f_{max}	maximum clock pulse frequency SH_{CP} or ST_{CP}	see Figs 7, 8 and 12	80	125	–	60	–	40	–	MHz	

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SYMBOL	PARAMETER	TEST CONDITIONS		T _{amb} (°C)						UNIT	
		WAVEFORMS	C _L	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
V_{CC} = 4.5 to 5.5 V; note 2											
t _{PHL} /t _{PLH}	propagation delay SH _{CP} to Q ₇ '	see Figs 7 and 12	15 pF	–	4.0	8.2	1.0	9.4	1.0	10.5	ns
	propagation delay ST _{CP} to Q _n	see Figs 8 and 12		–	4.2	7.4	1.0	8.5	1.0	9.5	ns
t _{PHL}	propagation delay MR to Q ₇ '	see Figs 10 and 12		–	4.4	8.0	1.0	9.1	1.0	10.0	ns
t _{PZH} /t _{PZL}	3-state output enable time \overline{OE} to Q _n	see Figs 11 and 12		–	4.0	8.6	1.0	10.0	1.0	11.0	ns
t _{PHZ} /t _{PLZ}	3-state output disable time \overline{OE} to Q _n			–	3.8	8.0	1.0	9.5	1.0	10.5	ns
t _{PHL} /t _{PLH}	propagation delay SH _{CP} to Q ₇ '	see Figs 7 and 12		50 pF	–	5.4	10.0	1.0	11.4	1.0	12.5
	propagation delay ST _{CP} to Q _n	see Figs 8 and 12	–		5.5	9.0	1.0	10.5	1.0	11.5	ns
t _{PHL}	propagation delay MR to Q ₇ '	see Figs 10 and 12	–		5.6	10.0	1.0	11.1	1.0	12.0	ns
t _{PZH} /t _{PZL}	3-state output enable time \overline{OE} to Q _n	see Figs 11 and 12	–		5.3	10.6	1.0	12.0	1.0	13.0	ns
t _{PHZ} /t _{PLZ}	3-state output disable time \overline{OE} to Q _n		–		5.8	10.3	1.0	11.0	1.0	12.0	ns
t _W	shift clock pulse width HIGH or LOW	see Figs 7 and 12	5.0		–	–	5.0	–	5.0	–	ns
	storage clock pulse width HIGH or LOW	see Figs 8 and 12	5.0	–	–	5.0	–	5.0	–	ns	
	master reset pulse width LOW	see Figs 10 and 12	5.0	–	–	5.0	–	5.0	–	ns	
t _{su}	set-up time D _S to SH _{CP}	see Figs 8 and 12	3.0	–	–	3.0	–	3.0	–	ns	
	set-up time SH _{CP} to ST _{CP}	see Figs 9 and 12	5.0	–	–	5.0	–	5.0	–	ns	
t _h	hold time D _S to SH _{CP}	see Figs 10 and 12	2.0	–	–	2.0	–	2.0	–	ns	
t _{rem}	removal time MR to SH _{CP}		2.5	–	–	2.5	–	2.5	–	ns	
f _{max}	maximum clock pulse frequency SH _{CP} or ST _{CP}	see Figs 7, 8 and 12	130	170	–	110	–	90	–	MHz	

Notes

1. Typical values at V_{CC} = 3.3 V.
2. Typical values at V_{CC} = 5.0 V.

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Type 74AHCT595GND = 0 V; $t_r = t_f \leq 3.0$ ns.

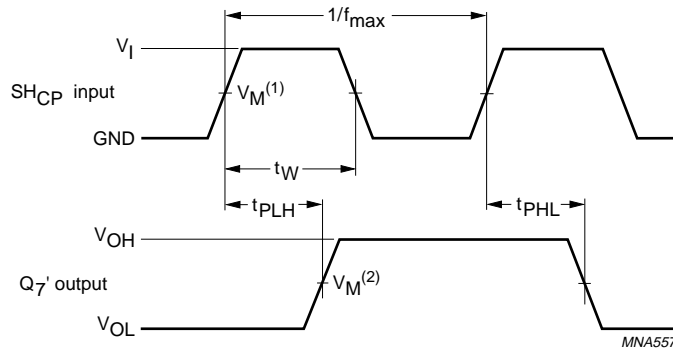
SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)						UNIT	
		WAVEFORMS	C_L	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
$V_{CC} = 4.5$ to 5.5 V; note 1											
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q_7'	see Figs 7 and 12	15 pF	–	3.8	8.2	1.0	9.0	1.0	10.0	ns
	propagation delay ST_{CP} to Q_n	see Figs 8 and 12		–	4.0	7.4	1.0	8.5	1.0	9.5	ns
t_{PHL}	propagation delay \overline{MR} to Q_7'	see Figs 10 and 12		–	4.6	8.2	1.0	9.5	1.0	10.5	ns
t_{PZH}/t_{PZL}	3-state output enable time \overline{OE} to Q_n	see Figs 11 and 12		–	4.8	9.0	1.0	11.0	1.0	12.0	ns
t_{PHZ}/t_{PLZ}	3-state output disable time \overline{OE} to Q_n			–	3.6	6.9	1.0	8.0	1.0	9.0	ns
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q_7'	see Figs 7 and 12	50 pF	–	5.2	10.0	1.0	11.0	1.0	12.0	ns
	propagation delay ST_{CP} to Q_n	see Figs 8 and 12		–	5.3	9.0	1.0	10.5	1.0	11.5	ns
t_{PHL}	propagation delay \overline{MR} to Q_7'	see Figs 10 and 12		–	5.8	10.5	1.0	11.5	1.0	12.5	ns
t_{PZH}/t_{PZL}	3-state output enable time \overline{OE} to Q_n	see Figs 11 and 12		–	6.2	11.6	1.0	13.0	1.0	14.5	ns
t_{PHZ}/t_{PLZ}	3-state output disable time \overline{OE} to Q_n			–	5.8	10.3	1.0	11.0	1.0	12.0	ns
t_W	shift clock pulse width HIGH or LOW	see Figs 7 and 12		5.0	–	–	5.0	–	5.0	–	ns
	storage clock pulse width HIGH or LOW	see Figs 8 and 12		5.0	–	–	5.0	–	5.0	–	ns
	master reset pulse width LOW	see Figs 10 and 12		5.0	–	–	5.0	–	5.0	–	ns
t_{su}	set-up time SH_{CP} to ST_{CP}	see Figs 8 and 12		5.0	–	–	5.0	–	5.0	–	ns
	set-up time D_S to SH_{CP}	see Figs 9 and 12		3.0	–	–	3.0	–	3.0	–	ns
t_h	hold time D_S to SH_{CP}		2.0	–	–	2.0	–	2.0	–	ns	
t_{rem}	removal time \overline{MR} to SH_{CP}	see Figs 10 and 12	3.0	–	–	3.0	–	3.0	–	ns	
f_{max}	maximum clock pulse frequency SH_{CP} or ST_{CP}	see Figs 7, 8 and 12	130	170	–	110	–	90	–	MHz	

Note1. Typical values at $V_{CC} = 5.0$ V.

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

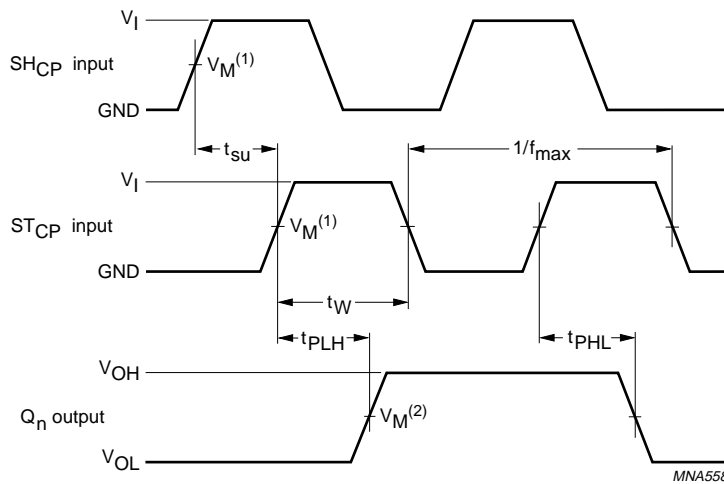
74AHC595; 74AHCT595

AC WAVEFORMS



FAMILY	VI INPUT REQUIREMENTS	VM(1) INPUT	VM(2) OUTPUT
AHC	GND to VCC	50% VCC	50% VCC
AHCT	GND to 3.0 V	1.5 V	50% VCC

Fig.7 The clock (SHCP) to output (Q7') propagation delays, the shift clock pulse width (tW) and maximum shift clock frequency (fmax).

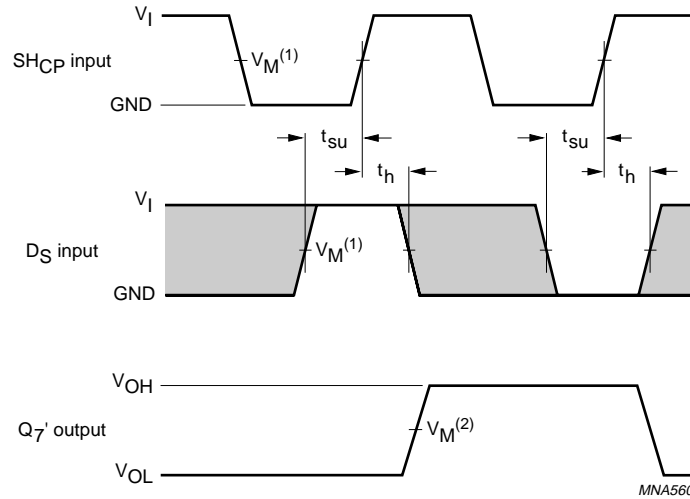


FAMILY	VI INPUT REQUIREMENTS	VM(1) INPUT	VM(2) OUTPUT
AHC	GND to VCC	50% VCC	50% VCC
AHCT	GND to 3.0 V	1.5 V	50% VCC

Fig.8 The storage clock (STCP) to output (Qn) propagation delays, the storage clock pulse width (tW) and the shift clock to storage clock set-up time (tsu).

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

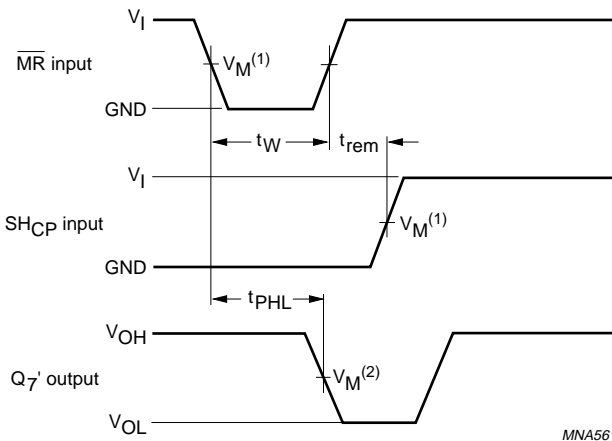
74AHC595; 74AHCT595



FAMILY	V _I INPUT REQUIREMENTS	V _M ⁽¹⁾ INPUT	V _M ⁽²⁾ OUTPUT
AHC	GND to V _{CC}	50% V _{CC}	50% V _{CC}
AHCT	GND to 3.0 V	1.5 V	50% V _{CC}

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.9 The data set-up (t_{su}) and hold (t_h) times for the D_S input.

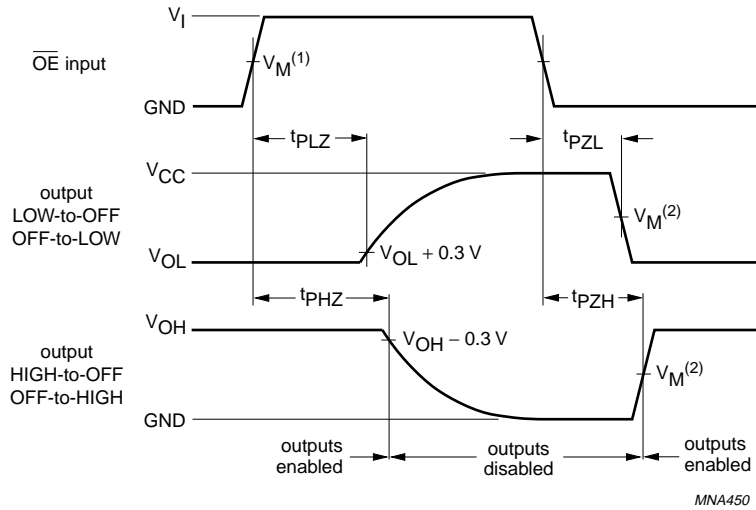


FAMILY	V _I INPUT REQUIREMENTS	V _M ⁽¹⁾ INPUT	V _M ⁽²⁾ OUTPUT
AHC	GND to V _{CC}	50% V _{CC}	50% V _{CC}
AHCT	GND to 3.0 V	1.5 V	50% V _{CC}

Fig.10 The master reset (\overline{MR}) pulse width, the master reset to output (Q_7) propagation delays and the master reset to shift clock (SHCP) removal time (t_{rem}).

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

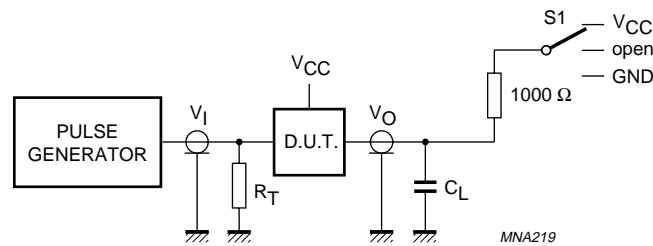
74AHC595; 74AHCT595



MNA450

FAMILY	V _I INPUT REQUIREMENTS	V _M ⁽¹⁾ INPUT	V _M ⁽²⁾ OUTPUT
AHC	GND to V _{CC}	50% V _{CC}	50% V _{CC}
AHCT	GND to 3.0 V	1.5 V	50% V _{CC}

Fig.11 3-state enable and disable times.



MNA219

TEST	S1
t _{PLH} /t _{PHL}	open
t _{PLZ} /t _{PZL}	V _{CC}
t _{PHZ} /t _{PZH}	GND

Definitions for test circuit.

C_L = load capacitance including jig and probe capacitance (See Chapter "AC characteristics").
 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.12 Load circuitry for switching times.

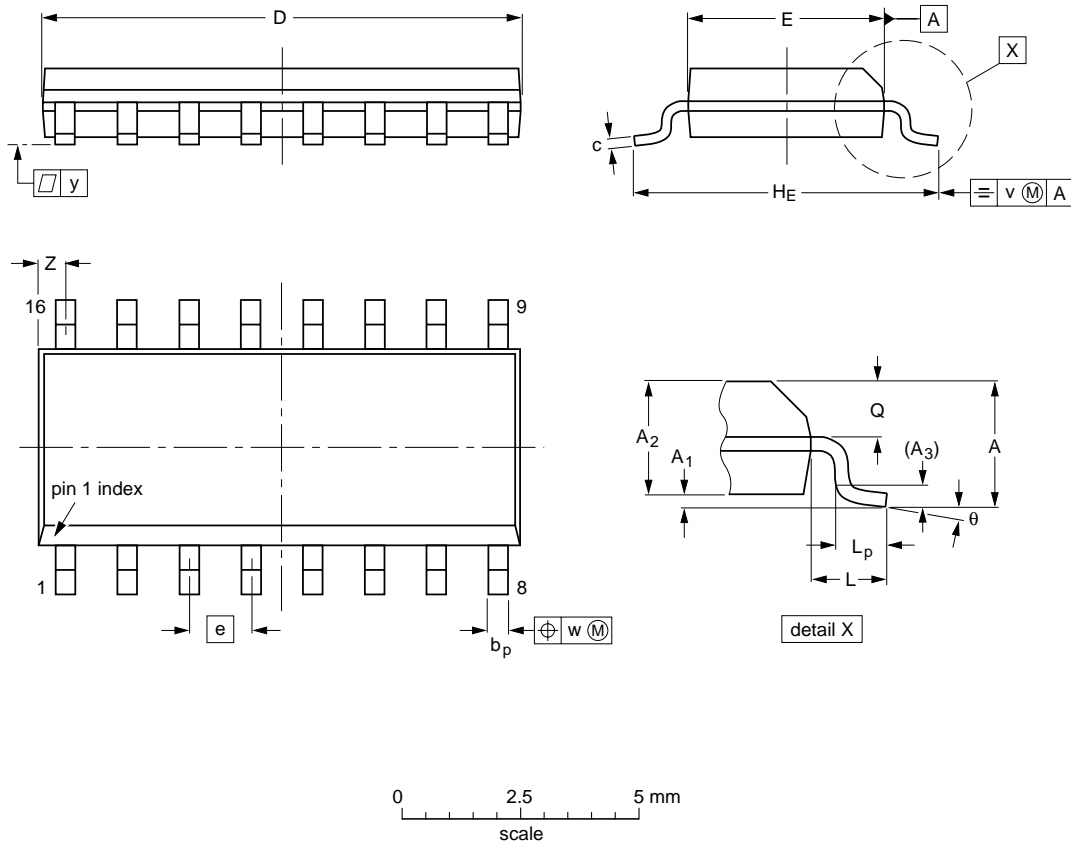
8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74AHC595; 74AHCT595

PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

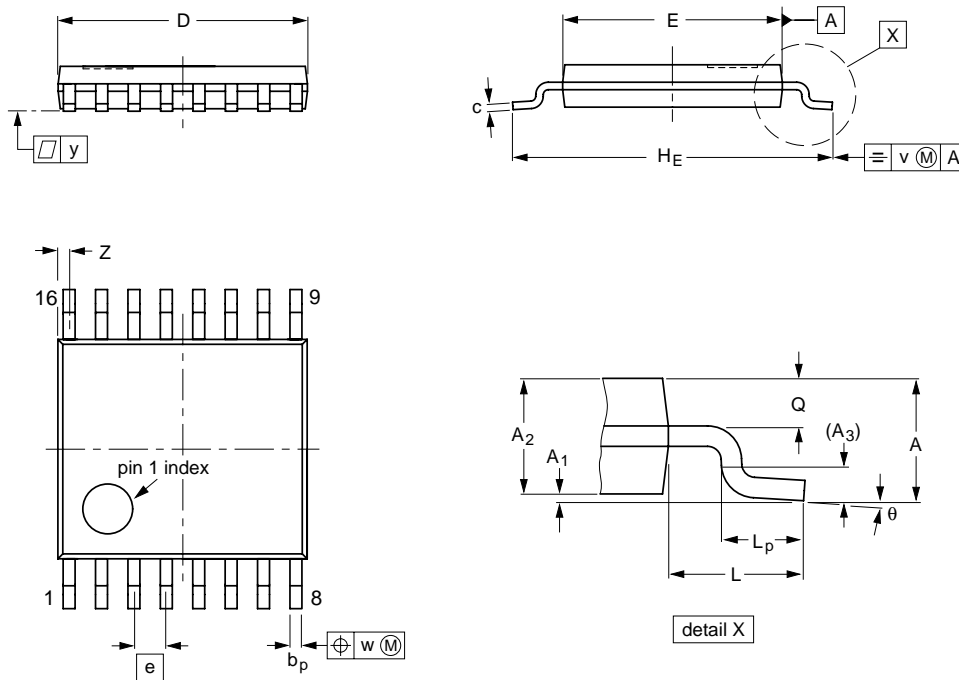
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT109-1	076E07	MS-012			97-05-22 99-12-27

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74AHC595; 74AHCT595

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				-95-04-04 99-12-27

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74AHC595; 74AHCT595

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74AHC595; 74AHCT595

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
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Product specification	This data sheet contains final product specifications.
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Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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Printed in The Netherlands

613507/01/pp20

Date of release: 2000 Mar 15

Document order number: 9397 750 06822

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