

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

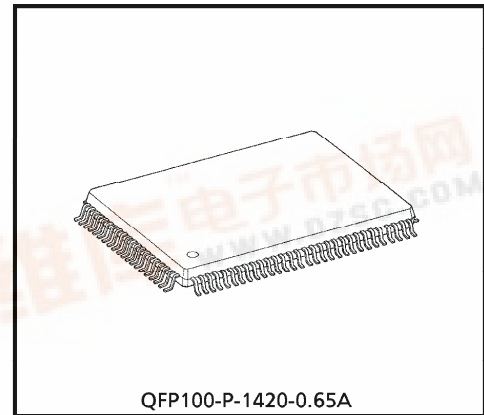
# T6B07

## COLUMN DRIVER FOR A DOT MATRIX LCD

The T6B07 is an 80-channel-output column driver for an STN dot matrix LCD. The T6B07 features 28-V LCD drive voltage and a 10-MHz maximum operating frequency. The T6B07 is able to drive LCD panels with a duty ratio of up to 1/240. It is recommended for use with the T6B08.

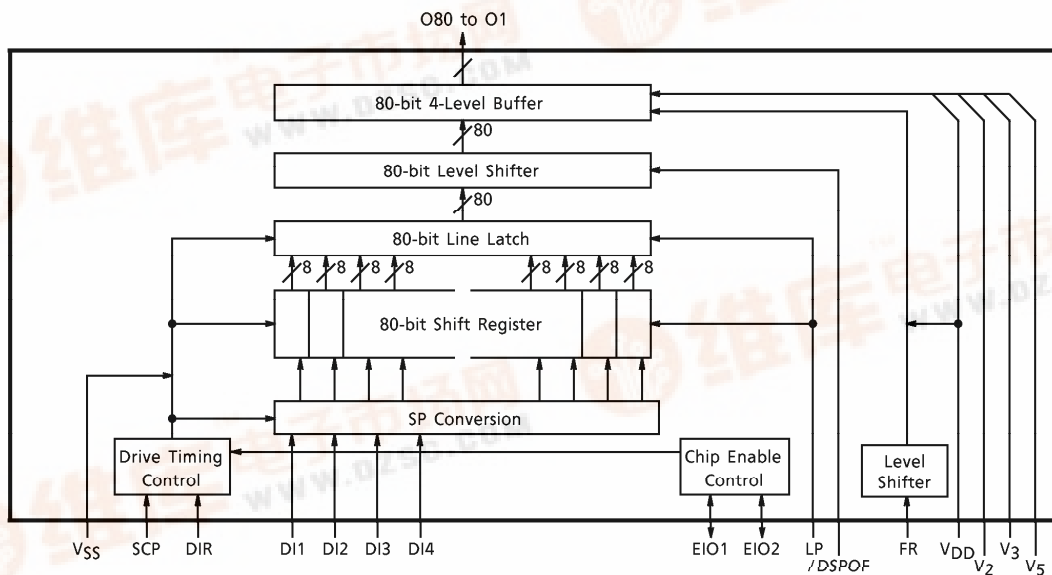
### FEATURES

- Display duty application : to 1/240
- LCD drive signal : 80
- Data transfer : 1, 2, 4-bit bidirectional
- Operating frequency : 10MHz
- LCD drive voltage : 11 to 28V (max 30V)
- Operating voltage : 3.0 to 5.5V
- Operating temperature : -20 to 75°C
- LCD drive output resistance : 2.2kΩ (max) (12.8V, 1/9 bias)
- Display-off function : When /DSPOF is L, all LCD drive outputs (O1 to O80) remain at the V<sub>DD</sub> level.
- Low power consumption : Cascade connections and auto enable transfer functions are available.



Weight : 1.60g (typ.)

### BLOCK DIAGRAM



961001EBA2

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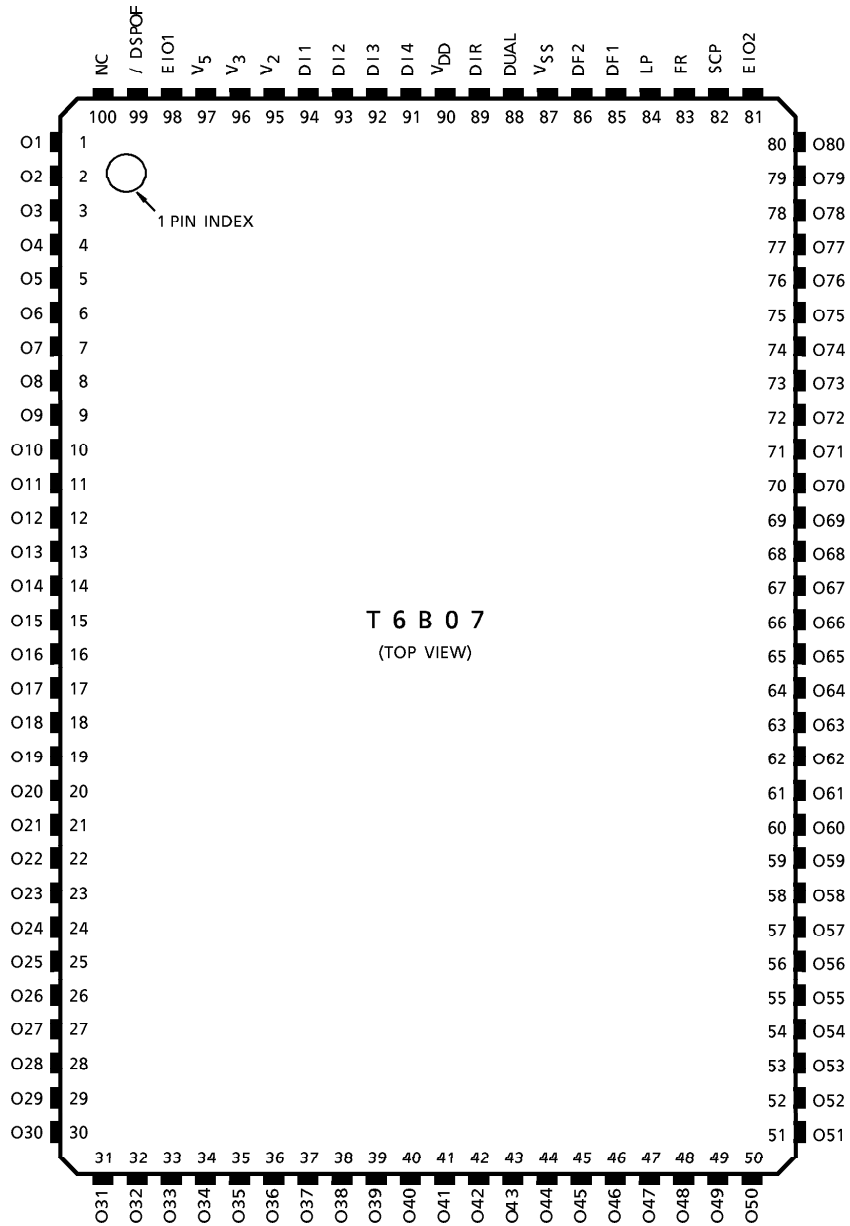
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PIN ASSIGNMENT



**PIN FUNCTIONS**

PIN NAME	I/O	FUNCTIONS	LEVEL																			
O1 to O80	Output	Output for LCD drive signal	V <sub>DD</sub> to V <sub>5</sub>																			
DI1 to DI4	Input	Input for shift data																				
SCP	Input	(Shift Clock Pulse) Input for shift clock pulse	V <sub>DD</sub> to V <sub>SS</sub>																			
FR	Input	(Frame) Input for frame signal																				
LP	Input	(Latch Pulse) Input for shift clock pulse Display data is latched on the rising edge of LP.																				
DUAL	Input	(Dual Mode) Terminal for dual input mode or single input mode select																				
DIR	Input	(Direction) Input for data flow direction select																				
DF1, DF2	Input	(Data Format) Input for selection data format (1-bit, 2-bit, 4-bit)																				
EIO1, EIO2	I/O	Input/output for ENABLE signal <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>DUAL</th> <th>DIR</th> <th>EIO2</th> <th>EIO1</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>OUT</td> <td>IN</td> </tr> <tr> <td>L</td> <td>H</td> <td>IN</td> <td>OUT</td> </tr> <tr> <td>H</td> <td>L</td> <td>OUT</td> <td>IN</td> </tr> <tr> <td>H</td> <td>H</td> <td>OUT</td> <td>IN</td> </tr> </tbody> </table>		DUAL	DIR	EIO2	EIO1	L	L	OUT	IN	L	H	IN	OUT	H	L	OUT	IN	H	H	OUT
DUAL	DIR	EIO2	EIO1																			
L	L	OUT	IN																			
L	H	IN	OUT																			
H	L	OUT	IN																			
H	H	OUT	IN																			
/DSPOF	Input	(Display Off) /DSPOF=L : Display-off mode, (O1 to O80) remain at the V <sub>DD</sub> level. /DSPOF=H : Display-on mode, (O1 to O80) are operational.																				
V <sub>DD</sub>	—	Power supply for internal logic (5V)	—																			
V <sub>SS</sub>	—	Power supply for internal logic (0V)																				
V <sub>2</sub>	—	Power supply for LCD drive circuit																				
V <sub>3</sub>	—	Power supply for LCD drive circuit																				
V <sub>5</sub>	—	Power supply for LCD drive circuit																				

**RELATION BETWEEN FR, DATA INPUT AND OUTPUT LEVEL**

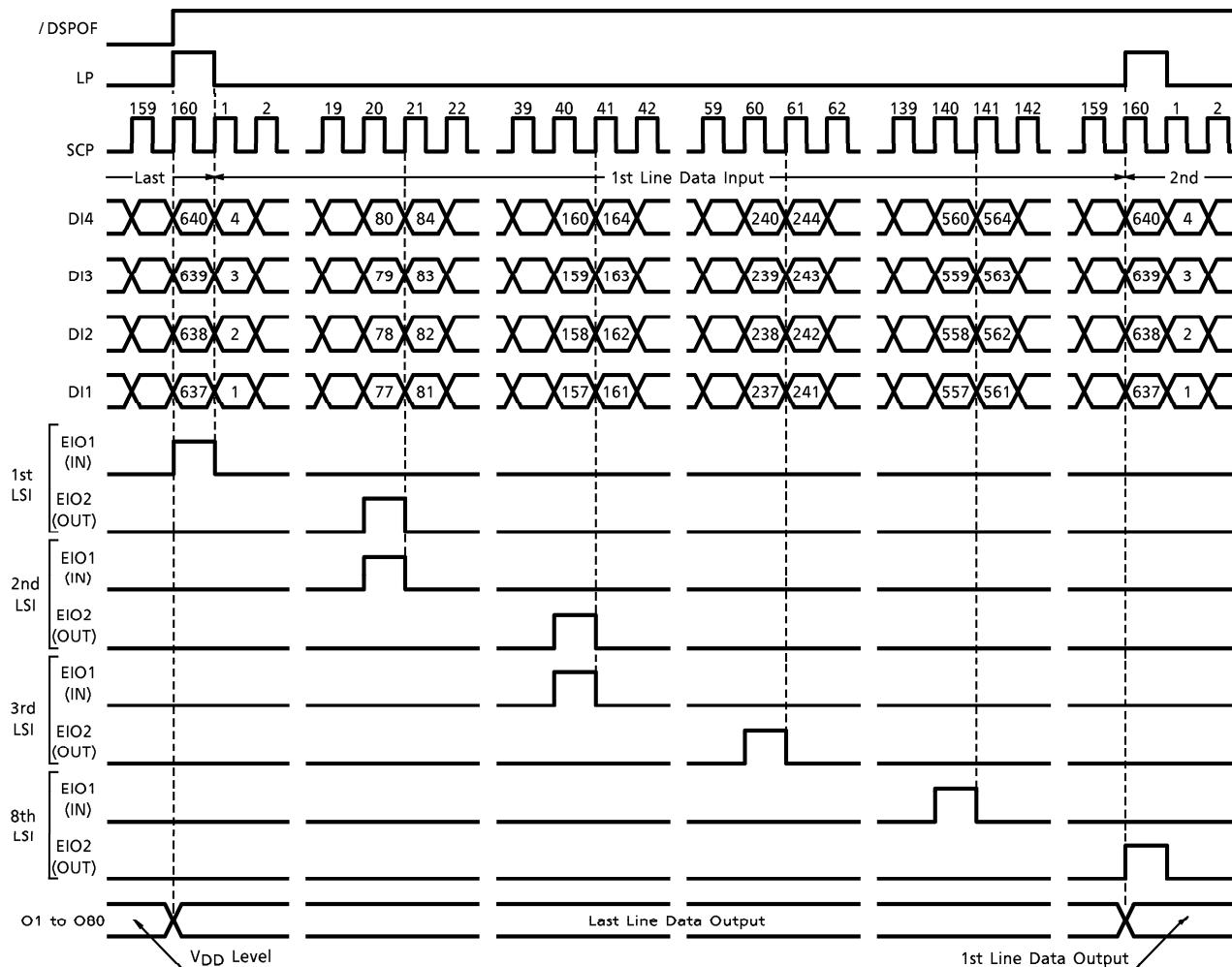
FR	DATA INPUT (DIO1, DIO2)	/DSPOF	OUTPUT LEVEL
L	L	H	V <sub>2</sub>
L	H	H	V <sub>DD</sub>
H	L	H	V <sub>3</sub>
H	H	H	V <sub>5</sub>
*	*	L	V <sub>DD</sub>

\*Don't care



**TIMING DIAGRAM**

DIR = L, DUAL = L, DF2 = H



**ABSOLUTE MAXIMUM RATINGS**

(Ensure that the following conditions are maintained,  $V_{DD} \geq V_2 \geq V_3 \geq V_5$ ,  $V_{SS} = 0V$ )

ITEM	SYMBOL	PIN NAME	RATING	UNIT
Supply Voltage 1	$V_{DD}$	$V_{DD}$	-0.3 to 7.0	V
Supply Voltage 2	$V_2$	$V_2$	$V_{DD} - 30.0$ to $V_{DD} + 0.3$	V
	$V_3$	$V_3$		
	$V_5$	$V_5$		
Input Voltage	$V_{IN}$	(*1)	-0.3 to $V_{DD} + 0.3$	V
Operating Temperature	$T_{opr}$	—	-20 to 75	°C
Storage Temperature	$T_{stg}$	—	-55 to 125	°C

(\*1) SCP, FR, LP, DIR, DF1, DF2, DUAL, DI1 to DI4, /DSPOF

**ELECTRICAL CHARACTERISTICS**

**DC CHARACTERISTICS**

TEST CONDITIONS (1) (Unless otherwise noted,  $V_{SS} = 0V$ ,  $V_{DD} = 4.5$  to  $5.5V$ ,  $V_5 = (V_{DD} - 28)$  to  $(V_{DD} - 11)V$ ,  $T_a = -20$  to  $75^\circ C$ )

ITEM	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	PIN NAME
Supply Voltage 1	—	—	—	4.5	5.0	5.5	V	$V_{DD}$
Supply Voltage 2	$V_5$	—	—	$V_{DD} - 28$	—	$V_{DD} - 11$	V	$V_5$
Input Voltage	H Level	$V_{IH}$	—	$V_{DD} - 0.8$	—	$V_{DD}$	V	SCP, FR, LP, DIR, DUAL, DF1, DF2, DI1 to DI4, /DSPOF
	L Level	$V_{IL}$	—	0	—	0.8		
Output Voltage	H Level	$V_{OH}$	$I_{OH} = -0.5mA$	$V_{DD} - 0.5$	—	—	V	EIO1, EIO2
	L Level	$V_{OL}$	$I_{OL} = 0.5mA$	—	—	0.5		
Output Resistance	H Level	$R_{OH}$	$V_{OUT} = V_{DD} - 0.5V$ (*2)	—	1.2	2.2	k $\Omega$	O1 to O80
	M Level	$R_{OM}$	$V_{OUT} = V_2 \pm 0.5V$ (*2)	—	1.2	2.2		
		$R_{OM}$	$V_{OUT} = V_3 \pm 0.5V$ (*2)	—	1.2	2.2		
	L Level	$R_{OL}$	$V_{OUT} = V_5 + 0.5V$ (*2)	—	1.2	2.2		
Current Consumption (*3)	$I_{SS}$	—	$V_{DD} = 5.5V$ $V_5 = -22.5V$ $f_{FR} = 35Hz$ $f_{SCP} = 2.5MHz$ $V_{IH} = 5.5V, V_{IL} = 0V$ Input Data: every bit inverted	—	400	700	$\mu A$	$V_{SS}$
Current Consumption (*4)	$I_{SS}$	—	As mentioned above	—	100	200	$\mu A$	$V_{SS}$

(\*2)  $V_{DD} = 3.0V$ ,  $V_5 = -7.8V$ ,  $V_2 = V_{DD} - 2/9(V_{DD} - V_5)$ ,  $V_3 = V_{DD} - 7/9(V_{DD} - V_5)$

(\*3) Internal data receiver operating

(\*4) Internal data receiver sleeping

TEST CONDITIONS (2) (Unless otherwise noted,  $V_{SS} = 0V$ ,  $V_{DD} = 3.0$  to  $5.5V$ ,  $V_5 = (V_{DD} - 28)$  to  $(V_{DD} - 11)V$ ,  $T_a = -20$  to  $75^\circ C$ )

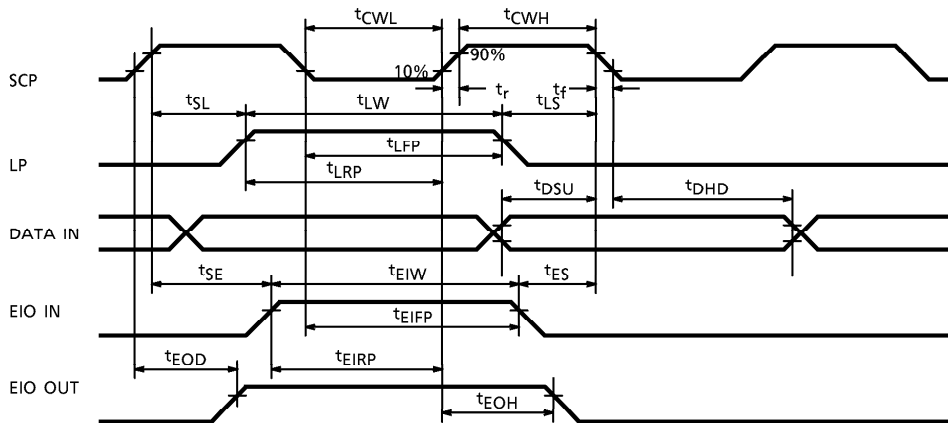
ITEM	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	PIN NAME
Supply Voltage 1	—	—	—	3.0	3.3	5.5	V	$V_{DD}$
Supply Voltage 2	$V_5$	—	—	$V_{DD} - 28$	—	$V_{DD} - 11$	V	$V_5$
Input Voltage	H Level	$V_{IH}$	—	$V_{DD} - 0.6$	—	$V_{DD}$	V	SCP, FR, LP, DIR, DUAL, DF1, DF2, DI1 to DI4, /DSPOF
	L Level	$V_{IL}$	—	0	—	0.6		
Output Voltage	H Level	$V_{OH}$	$I_{OH} = -0.5mA$	$V_{DD} - 0.5$	—	—	V	EIO1, EIO2
	L Level	$V_{OL}$	$I_{OL} = 0.5mA$	—	—	0.5		
Output Resistance	H Level	$R_{OH}$	—	$V_{OUT} = V_{DD} - 0.5V$ (*5)	—	1.2	k $\Omega$	O1 to O80
	M Level	$R_{OM}$	—	$V_{OUT} = V_2 \pm 0.5V$ (*5)	—	1.2		
		$R_{OM}$	—	$V_{OUT} = V_3 \pm 0.5V$ (*5)	—	1.2		
	L Level	$R_{OL}$	—	$V_{OUT} = V_5 + 0.5V$ (*5)	—	1.2		
Current Consumption (*6)	$I_{SS}$	—	$V_{DD} = 5.5V$ $V_5 = -2.5V$ $f_{FR} = 35Hz$ $f_{SCP} = 2.5MHz$ $V_{IH} = 5.5V$ , $V_{IL} = 0V$ Input Data: every bit inverted	—	400	700	$\mu A$	$V_{SS}$
Current Consumption (*7)	$I_{SS}$	—	As mentioned above	—	100	200	$\mu A$	$V_{SS}$

(\*5)  $V_{DD} = 3.0V$ ,  $V_5 = -9.8V$ ,  $V_2 = V_{DD} - 2/9(V_{DD} - V_5)$ ,  $V_3 = V_{DD} - 7/9(V_{DD} - V_5)$

(\*6) Internal data receiver operating

(\*7) Internal data receiver sleeping

AC CHARACTERISTICS



TEST CONDITIONS (1)

( $V_{SS} = 0V$ ,  $V_{DD} = 4.5$  to  $5.5V$ ,  $V_0 = V_{DD}$ ,  $V_5 = (V_{DD} - 28)$  to  $(V_{DD} - 11)V$ ,  $T_a = -20$  to  $75^\circ C$ )

ITEM	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Operating Frequency	$t_{SCP}$	—	—	10.0	MHz
SCP Pulse Width	$t_{CWH}$	—	40	—	ns
	$t_{CWL}$	—	40	—	
Data Set-up Time	$t_{DSU}$	—	15	—	
Data Hold Time	$t_{DHD}$	—	5	—	
SCP Rise / Fall Time	$t_r, t_f$	—	—	(*9)	
LP Set-up Time	$t_{LRP}$	—	5	—	
LP Hold Time	$t_{LFP}$	—	15	—	
LP Pulse Width	$t_{LW}$	—	15	—	
SCP-Rise-to-LP-Rise Time	$t_{SL}$	—	10	—	
LP-Fall-to-SCP-Fall Time	$t_{LS}$	—	17	—	
EIO IN Set-up Time	$t_{EIRP}$	—	5	—	
EIO IN Hold Time	$t_{EIFP}$	—	15	—	
EIO IN Pulse Width	$t_{EIW}$	—	15	—	
SCP-Rise-to-EIO-Rise Time	$t_{SE}$	(*8)	0	—	
EIO-Fall-to-SCP-Fall Time	$t_{ES}$	(*8)	20	—	
EIO OUT Data Delay Time	$t_{EOD}$	—	—	55	
EIO OUT Hold Time	$t_{EOH}$	—	—	30	

(\*8)  $C_L = 10pF$

(\*9)  $t_r, t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$  or  $t_r, t_f \leq 50ns$



TEST CONDITIONS (2)

( $V_{SS} = 0V$ ,  $V_{DD} = 3.0$  to  $5.5V$ ,  $V_0 = V_{DD}$ ,  $V_5 = (V_{DD} - 28)$  to  $(V_{DD} - 11)V$ ,  $T_a = -20$  to  $75^\circ C$ )

ITEM	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Operating Frequency	$t_{SCP}$	—	—	6.5	MHz
SCP Pulse Width	$t_{CWH}$	—	50	—	ns
	$t_{CWL}$	—	50	—	
Data Set-up Time	$t_{DSU}$	—	30	—	
Data Hold Time	$t_{DHD}$	—	10	—	
SCP Rise / Fall Time	$t_r, t_f$	—	—	(*11)	
LP Set-up Time	$t_{LRP}$	—	8	—	
LP Hold Time	$t_{LFP}$	—	30	—	
LP Pulse Width	$t_{LW}$	—	30	—	
SCP-Rise-to-LP-Rise Time	$t_{SL}$	—	20	—	
LP-Fall-to-SCP-Fall Time	$t_{LS}$	—	40	—	
EIO IN Set-up Time	$t_{EIRP}$	—	10	—	
EIO IN Hold Time	$t_{EIFP}$	—	30	—	
EIO IN Pulse Width	$t_{EIW}$	—	30	—	
SCP-Rise-to-EIO-Rise Time	$t_{SE}$	(*10)	0	—	
EIO-Fall-to-SCP-Fall Time	$t_{ES}$	(*10)	33	—	
EIO OUT Data Delay Time	$t_{EOD}$	—	—	80	
EIO OUT Hold Time	$t_{EOH}$	—	—	43	

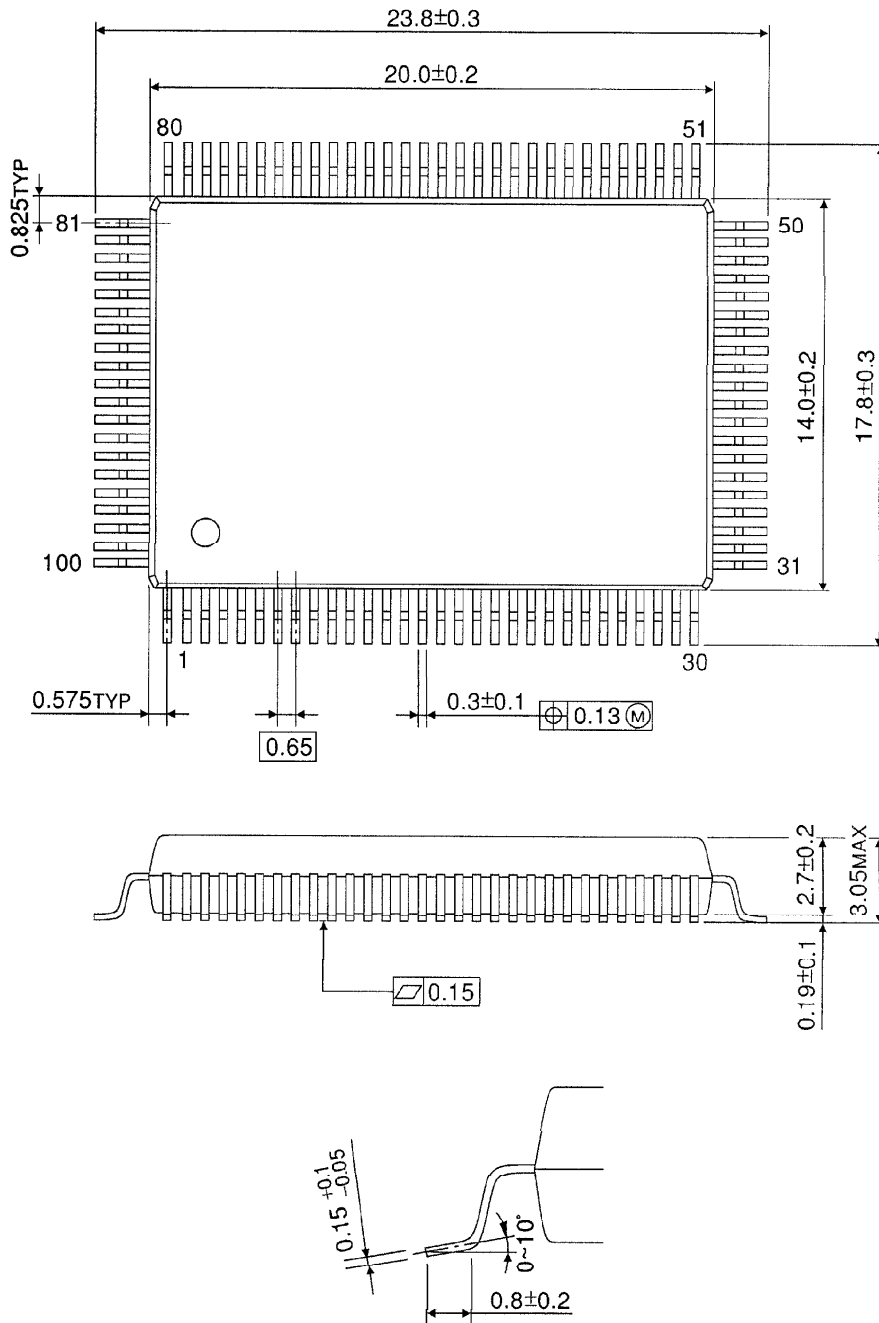
(\*10)  $C_L = 10pF$

(\*11)  $t_r, t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$  or  $t_r, t_f \leq 50ns$

(Note) Insert the bypass capacitor ( $0.1\mu F$ ) between  $V_{DD}$  and  $V_{SS}$  to decrease power supply noise. Place the bypass capacitor as close to the LSI as possible.

OUTLINE DRAWING  
QFP100-P-1420-0.65A

Unit : mm



Weight : 1.60g (Typ.)