

TOSHIBA

T6B66B

TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T 6 B 6 6 B

ROW DRIVER LSI FOR DOT MATRIX LCD

The TOSHIBA T6B66B is a row (common) driver LSI for a small- or medium-scale dot matrix LCD.

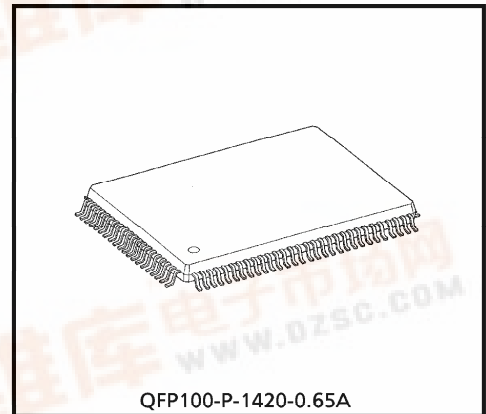
The T6B66B generates timing signals for the display using an on-chip oscillator and also controls the T6B65A column (segment) LCD driver.

Four duty options are available: 1/17, 1/33, 1/49 and 1/65.

It has 65 low-impedance row-driver outputs.

It has internal resistors to divide the bias voltage, a power supply Op-Amp DC-DC converter and a contrast control circuit.

It is easy to construct a low-power LCD system consisting of a T6B66B and a T6B65A column (segment) LCD driver.



QFP100-P-1420-0.65A

Weight : 1.6 g (typ.)

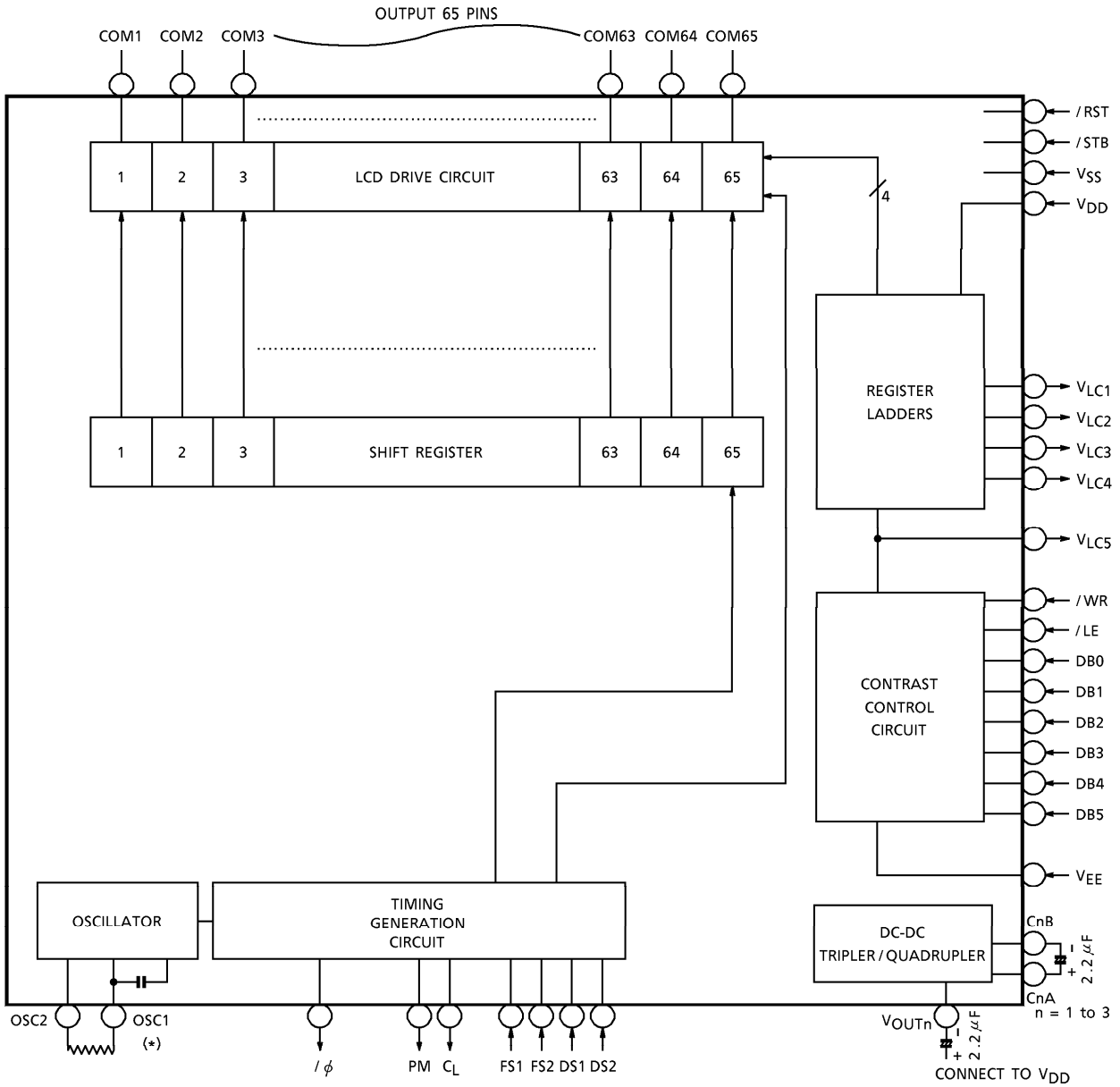
FEATURES

- Timing signal for LCD generated
- 65 low-impedance LCD driver outputs
- On-chip oscillator with external resistor and internal capacitor
- Duty : 1/17, 1/33, 1/49, 1/65
- Low power consumption
- Logic power supply : 2.7 to 5.5 V
- LCD power supply : $V_{DD} - 4.0$ to $V_{DD} - 16.0$ V
- CMOS Si-Gate process
- 100-pin flat plastic package

980910EBA1

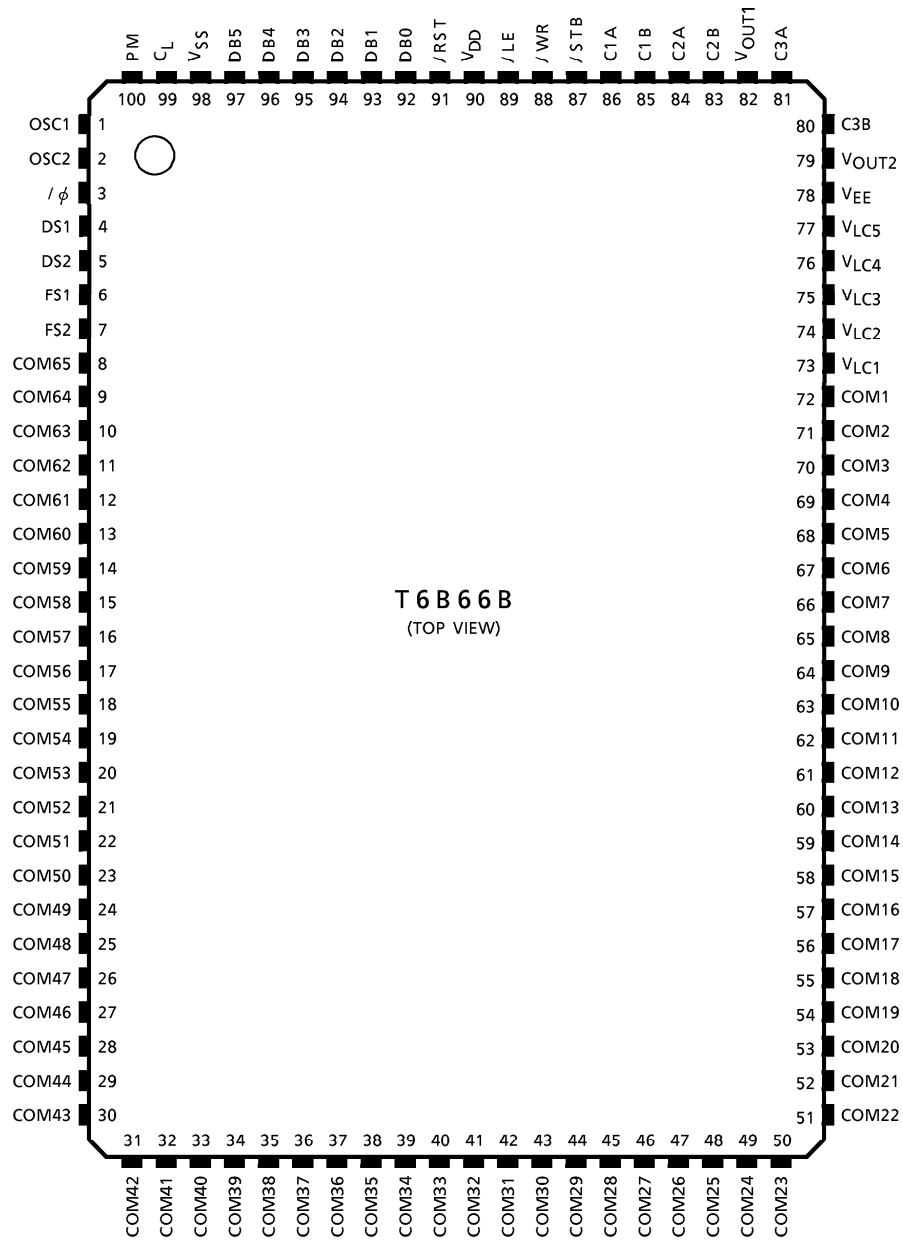
- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

BLOCK DIAGRAM



(*) : When external clock operation is used, the clock should be input to OSC1.

PIN ASSIGNMENT



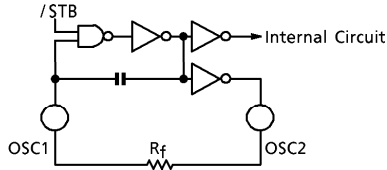
PIN FUNCTIONS

PIN NAME	PIN No.	I/O	FUNCTIONS																									
COM1 to COM65	8 to 72	Output	Row driver outputs																									
CL	99	Output	Shift clock pulse																									
PM	100	Output	Pre-Frame signal																									
/φ	3	Output	Clock signal																									
/LE	89	Input	Latch Enable signal																									
/WR	88	Input	Write Enable signal																									
DB0 to DB5	92 to 97	Input	Data bus																									
DS1, DS2	4, 5	Input	Display duty select																									
			<table border="1"> <thead> <tr> <th>DISPLAY DUTY</th> <th>1/17</th> <th>1/33</th> <th>1/49</th> <th>1/65</th> </tr> </thead> <tbody> <tr> <td>DS1</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>DS2</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	DISPLAY DUTY	1/17	1/33	1/49	1/65	DS1	0	1	0	1	DS2	0	0	1	1										
			DISPLAY DUTY	1/17	1/33	1/49	1/65																					
DS1	0	1	0	1																								
DS2	0	0	1	1																								
FS1, FS2	6, 7	Input	Frequency select																									
			<table border="1"> <thead> <tr> <th>FS1</th> <th>FS2</th> <th>f_{OSC} (kHz)</th> <th>f_{PM} (Hz)</th> <th>f_{/φ} (kHz)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>26.88</td> <td>35</td> <td>13.44</td> </tr> <tr> <td>1</td> <td>0</td> <td>53.76</td> <td>35</td> <td>26.88</td> </tr> <tr> <td>0</td> <td>1</td> <td>215.0</td> <td>35</td> <td>107.5</td> </tr> <tr> <td>1</td> <td>1</td> <td>430.1</td> <td>35</td> <td>215.0</td> </tr> </tbody> </table>	FS1	FS2	f _{OSC} (kHz)	f _{PM} (Hz)	f _{/φ} (kHz)	0	0	26.88	35	13.44	1	0	53.76	35	26.88	0	1	215.0	35	107.5	1	1	430.1	35	215.0
			FS1	FS2	f _{OSC} (kHz)	f _{PM} (Hz)	f _{/φ} (kHz)																					
			0	0	26.88	35	13.44																					
			1	0	53.76	35	26.88																					
0	1	215.0	35	107.5																								
1	1	430.1	35	215.0																								
/STB	87	Input	Standby pin : when /STB = L, all clocks stop.																									
/RST	91	Input	Reset signal pin : When /RST = L, registers are cleared.																									
OSC1, OSC2	1, 2	Input	When using the internal clock oscillator, connect a resistor or ceramic oscillator between OSC1 and OSC2. When using an external clock, connect the clock to OSC1 and leave OSC2 open.																									
VOUT1	82	Output	DC-DC output pin																									
VOUT2	79	Output	DC-DC output pin																									
CnA to CnB	83 to 86	—	Connect using a capacitor for DC-DC converter (n = 1 to 3)																									
VDD, VSS	90, 98	—	Power supply																									
VLC1 to VLC5	73 to 77	—	Power supply for LCD drive																									
VEE	78	—	Power supply for LCD drive																									

FUNCTION OF EACH BLOCK

- Oscillator

The T6B66B has an on-chip oscillator with one external resistor.



R_f	f_{osc}	FS1	FS2
51 k Ω	430 kHz	H	H
110 k Ω	215 kHz	L	H
460 k Ω	54 kHz	H	L
1100 k Ω	27 kHz	L	L

(Note) : The resistance values are typical values. The oscillation frequency depends on how the device is mounted. It is necessary to adjust the oscillation frequency to a target value.

Relationship between oscillation frequency and R_f

- Timing generation circuit

This circuit divides the signals from the oscillator and generates display timing signals (CL, PM) and the operating clock ($/\phi$) signal.

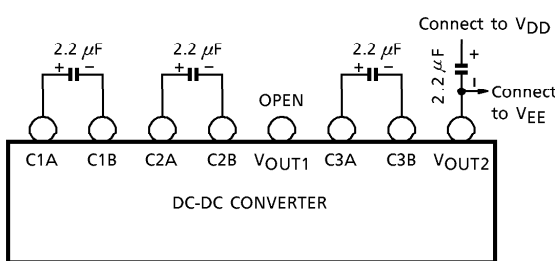
- Shift register

65-bit shift register

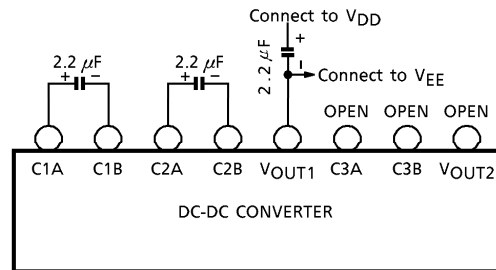
- DC-DC converter (tripler and quadrupler)

The T6B66B has an on-chip DC-DC tripler and quadrupler. When $/STB = L$, V_{OUT1} and $V_{OUT2} = V_{DD}$.

A 2.2 to 10 μF capacitor is recommended for this DC-DC Converter.



Quadrupler mode

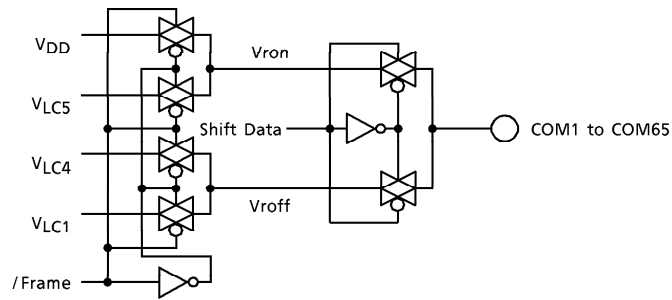


Tripler mode

When not using the DC-DC converter, leave the C_nA , C_nB and V_{OUTn} pins open and connect an external V_{EE} supply.

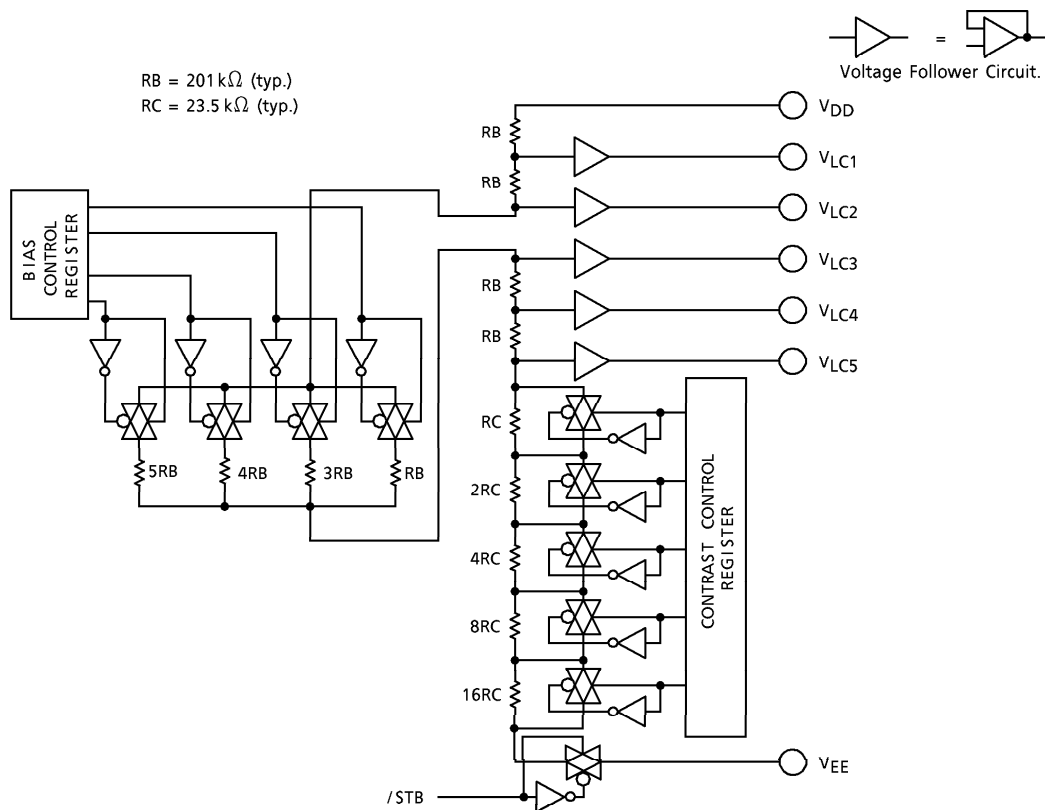
• Row driver circuit and LCD voltage generation circuit

The row driver circuit consists of 65 driver circuits. The combination of the data from the shift register and the Frame signal selects one of the four LCD levels. Details of the voltage generation circuit and the row driver circuit are shown in the diagram as below.



• Resistor ladder, contrast control circuit

The T6B66B has an on-chip resistor with an op-amp, bias selector and a contrast control circuit. The contrast control circuit allows 32 levels of contrast adjustment by software. The bias selector uses software to select the bias : 1/5, 1/7, 1/8 or 1/9. Details of the resistor ladder and the contrast control circuit are shown in the diagram below.



COMMAND DETAILS

CODE						FUNCTION
DB5	DB4	DB3	DB2	DB1	DB0	
1	CONTRAST (0 to 31)					Set Contrast
0	1	1	*	*	*	Test Mode Select
0	1	0	1	1/0	1/0	Op-Amp Control OP1
0	1	0	0	*	1/0	Op-Amp ON/OFF
0	0	0	1	R ₁	R ₂	Bias Control
0	0	0	0	1	1/0	Display ON/OFF

* : INVALID

- Set contrast

DB5	DB4	DB3	DB2	DB1	DB0
1	D	D	D	D	D

Range : 20H to 3FH

This command sets the contrast for the LCD. The T6B66B has 32 levels of contrast. (20H (bright)← →3FH (dark))

- Test mode select

DB5	DB4	DB3	DB2	DB1	DB0
0	1	1	*	*	*

* : INVALID

This command selects the test mode. Do not use this command.

- Op-Amp control 1 (OP1)

DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1/0	1/0

Range : 14H to 17H

This command sets the power supply level for the op-amp.

This command selects one of four levels. The command 14H selects the lowest level and 17H the maximum level.

(Notes) : When L is input to /RST, the power supply level is the minimum level.

● Op-amp ON/OFF

DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	*	1/0

Op-amp ON (0) / OFF (1)

* : INVALID

Range : 10H to 11H

This command sets the op-amp ON/OFF.

When using an external op-amp, the command 11H is used.

● Bias control

DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1/0	1/0

SET UP	BIAS
04H	1/5
05H	1/7
06H	1/8
07H	1/9

Range : 04H to 07H

This command sets the bias for the LCD power supply.

● Display ON/OFF

DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1/0

Display ON (1) / OFF (0)

Range : 02H to 03H

This command controls the display ON/OFF setting.

When the display is OFF, all the common output waveforms return to the V_{DD} level.

(Note) : When L is input to /RST, Display is set to OFF.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

ITEM	SYMBOL	RATING	UNIT
Supply Voltage (1)	V_{DD} (Note 1)	-0.3 to 7.0	V
Supply Voltage (2)	$V_{EE1, 2}$ (Note 3)	$V_{DD} - 18.0$ to $V_{DD} + 0.3$	V
Input Voltage	V_{in} (Note 1, 2)	-0.3 to $V_{DD} + 0.3$	V
Operating Temperature	T_{opr}	-20 to 75	°C
Storage Temperature	T_{stg}	-55 to 125	°C

(Note 1) : Referenced to V_{SS}

(Note 2) : Applies to data bus and I/O pins

(Note 3) : Ensure that the following condition is always maintained.

$$V_{DD} \geq V_{EE1}, V_{EE2}$$

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

TEST CONDITIONS (1)

(Unless otherwise noted, $V_{SS} = 0\text{ V}$, $V_{DD} = 3.0 \pm 10\%$, $V_{DD} - V_{EE} = 16\text{ V}$, $T_a = -20$ to 75°C)

ITEM	SYMBOL	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	PIN NAME
Operating Supply (1)	V_{DD}	—	—	2.7	—	3.3	V	V_{DD}
Operating Supply (2)	V_{EE}	—	—	$V_{DD} - 16.0$	—	$V_{DD} - 4.0$	V	V_{EE}
Input Voltage	H Level	V_{IH}	—	0.8 V_{DD}	—	V_{DD}	V	DS1, DS2 DB0 to DB5, /LE, /WR, /STB, /RST, FS1, FS2
	L Level	V_{IL}	—	0	—	0.2 V_{DD}	V	
Output Voltage	H Level	V_{OH}	$I_{OH} = -400\ \mu\text{A}$	$V_{DD} - 0.4$	—	—	V	C_L , PM, I_ϕ
	L Level	V_{OL}	$I_{OL} = 400\ \mu\text{A}$	—	—	0.4	V	
Row Driver Output Resistance	R_{row}	—	$V_{DD} - V_{LC5} = 16.0\text{ V}$ Load current $= \pm 100\ \mu\text{A}$	—	—	1.5	$\text{k}\Omega$	COM1 to COM65
Input Leakage	I_{IL}	—	$V_{in} = V_{DD}$ to V_{SS}	-1	—	1	μA	DB0 to DB5, /LE, /WR, /STB, /RST, FS1, FS2, DS1, DS2
Operating Frequency	f_ϕ	—	—	10	—	250	kHz	I_ϕ
External Clock Frequency	f_{ex}	—	—	20	—	500	kHz	OSC1
External Clock Duty	f_{duty}	—	—	45	50	55	%	OSC1
External Clock Rise / Fall Time	t_r / t_f	—	—	—	—	50	ns	OSC1
Current Consumption (1)	I_{SS}	1	(Note 1)	—	-200	-300	μA	V_{SS}
Current Consumption (2)	I_{EE}	2	(Note 2)	—	-60	-80	μA	V_{EE}
Current Consumption (3)	I_{DD}	3	(Note 3)	—	430	550	μA	V_{DD}
Current Consumption (4)	I_{STB}	4	(Note 4)	-1	—	1	μA	V_{DD}

(Note 1) : Logic current : $V_{EE} = V_{DD} - 16\text{ V}$, 1/65 duty, $R_f = 47\ \text{k}\Omega$, no load, op-amp minimum power supply level

(Note 2) : LCD driver current : $V_{EE} = V_{DD} - 16\text{ V}$, 1/9 bias, $R_f = 47\ \text{k}\Omega$, no load, op-amp minimum power supply level

(Note 3) : All currents : $V_{DD} = 3.0\text{ V}$, $V_{OUT2} = V_{EE}$ (quadrupler mode), 1/65 duty, 1/9 bias, $R_f = 47\ \text{k}\Omega$, no load, op-amp minimum power supply level

(Note 4) : Standby current : $V_{DD} = 3.0\text{ V} \pm 10\%$, $V_{OUT} = V_{EE}$, $T_a = 25^\circ\text{C}$, /STB = L, no load

TEST CONDITIONS (2)

(Unless otherwise noted, $V_{SS} = 0\text{ V}$, $V_{DD} = 5.0 \pm 10\%$, $V_{DD} - V_{EE} = 16\text{ V}$, $T_a = -20$ to 75°C)

ITEM	SYMBOL	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	PIN NAME
Operating Supply (1)	V_{DD}	—	—	4.5	—	5.5	V	V_{DD}
Operating Supply (2)	V_{EE}	—	—	$V_{DD} - 16.0$	—	$V_{DD} - 4.0$	V	V_{EE}
Input Voltage	H Level	V_{IH}	—	$0.7 V_{DD}$	—	V_{DD}	V	DS1, DS2 DB0 to DB5, /LE, /WR, /STB, /RST, FS1, FS2
	L Level	V_{IL}	—	0	—	$0.3 V_{DD}$	V	
Output Voltage	H Level	V_{OH}	—	$I_{OH} = -400\ \mu\text{A}$	—	—	V	C_L , PM, / ϕ
	L Level	V_{OL}	—	$I_{OL} = 400\ \mu\text{A}$	—	0.4	V	
Row Driver Output Resistance	R_{row}	—	$V_{DD} - V_{LC5} = 16.0\text{ V}$ Load current $= \pm 100\ \mu\text{A}$	—	—	1.5	$\text{k}\Omega$	COM1 to COM65
Input Leakage	I_{IL}	—	$V_{in} = V_{DD}$ to V_{SS}	-1	—	1	μA	DB0 to DB5, /LE, /WR, /STB, /RST, FS1, FS2, DS1, DS2
Operating Frequency	f_{ϕ}	—	—	10	—	250	kHz	/ ϕ
External Clock Frequency	f_{ex}	—	—	20	—	500	kHz	OSC1
External Clock Duty	f_{duty}	—	—	45	50	55	%	OSC1
External Clock Rise / Fall Time	t_r / t_f	—	—	—	—	50	ns	OSC1
Current Consumption (1)	I_{SS}	1	(Note 5)	—	-490	-680	μA	V_{SS}
Current Consumption (2)	I_{EE}	2	(Note 6)	—	-60	-80	μA	V_{EE}
Current Consumption (3)	I_{DD}	3	(Note 7)	—	680	900	μA	V_{DD}
Current Consumption (4)	I_{STB}	4	(Note 8)	-1	—	1	μA	V_{DD}

(Note 5) : Logic current : $V_{EE} = V_{DD} - 16\text{ V}$, 1/65 duty, $R_f = 47\ \text{k}\Omega$, no load, op-amp minimum power supply level

(Note 6) : LCD driver current : $V_{EE} = V_{DD} - 16\text{ V}$, 1/9 bias, $R_f = 47\ \text{k}\Omega$, no load, op-amp minimum power supply level

(Note 7) : All currents : $V_{DD} = 5.0\text{ V}$, $V_{OUT1} = V_{EE}$ (tripler mode), 1/65 duty, 1/9 bias, $R_f = 47\ \text{k}\Omega$, no load, op-amp minimum power supply level

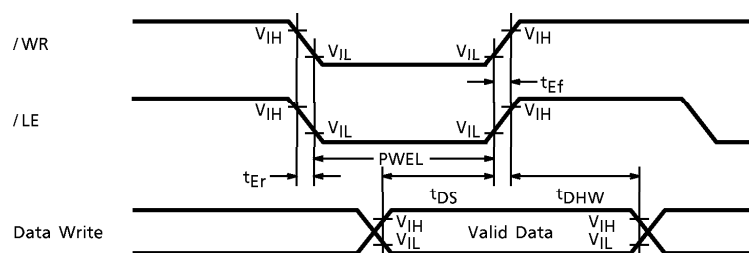
(Note 8) : Standby current : $V_{DD} = 5.0\text{ V}$, $V_{OUT} = V_{EE}$, $T_a = 25^\circ\text{C}$, /STB = L, no load

ITEM	SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	PIN NAME
Output Voltage (Tripler Mode)	VO1	5	(Note 9)	-9.47	-9.57	—	V	V _{OUT1}
Output Voltage (Quadrupler Mode)	VO2	6	(Note 10)	-8.07	-8.22	—	V	V _{OUT2}

(Note 9) : $V_{DD} = 5.0\text{ V}$, $I_{Load} = 500\ \mu\text{A}$, $V_{EE} = -10.0\text{ V}$ (external voltage)
 $C_{nA} - C_{nB} = 2.2\ \mu\text{F}$, $V_{DD} - V_{OUT1} = 2.2\ \mu\text{F}$, $R_f = 47\ \text{k}\Omega$, $T_a = 25^\circ\text{C}$

(Note 10) : $V_{DD} = 3.0\text{ V}$, $I_{Load} = 500\ \mu\text{A}$, $V_{EE} = -9.0\text{ V}$ (external voltage)
 $C_{nA} - C_{nB} = 2.2\ \mu\text{F}$, $V_{DD} - V_{OUT2} = 2.2\ \mu\text{F}$, $R_f = 47\ \text{k}\Omega$, $T_a = 25^\circ\text{C}$

AC CHARACTERISTICS



TEST CONDITIONS (1) ($V_{SS} = 0\text{ V}$, $V_{DD} = 3.0\text{ V} \pm 10\%$, $V_{DD} - V_{EE} = 16\text{ V}$, $T_a = -20\text{ to }75^\circ\text{C}$)

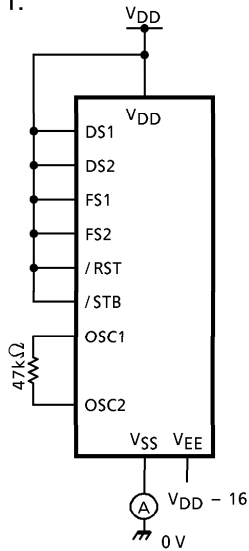
ITEM	SYMBOL	MIN	MAX	UNIT
Enable Rise / Fall Time	t_{Er} , t_{Ef}	—	25	ns
Enable Pulse Width	PWEL	60	—	ns
Data Set-up Time	t_{DS}	60	—	ns
Data Hold Time	t_{DHW}	10	—	ns

TEST CONDITIONS (2) ($V_{SS} = 0\text{ V}$, $V_{DD} = 5.0\text{ V} \pm 10\%$, $V_{DD} - V_{EE} = 16\text{ V}$, $T_a = -20\text{ to }75^\circ\text{C}$)

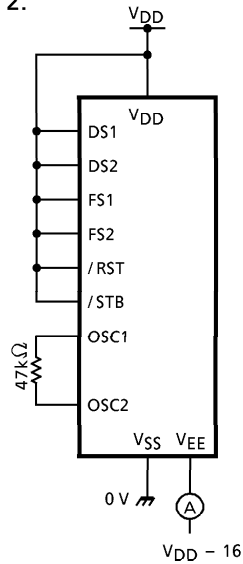
ITEM	SYMBOL	MIN	MAX	UNIT
Enable Rise / Fall Time	t_{Er} , t_{Ef}	—	20	ns
Enable Pulse Width	PWEL	60	—	ns
Data Set-up Time	t_{DS}	60	—	ns
Data Hold Time	t_{DHW}	10	—	ns

TEST CIRCUIT

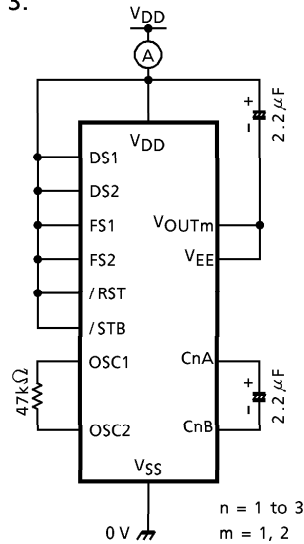
1.



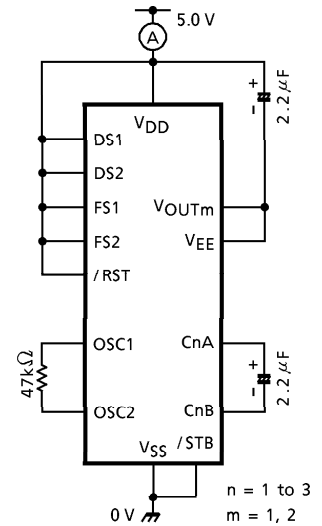
2.



3.

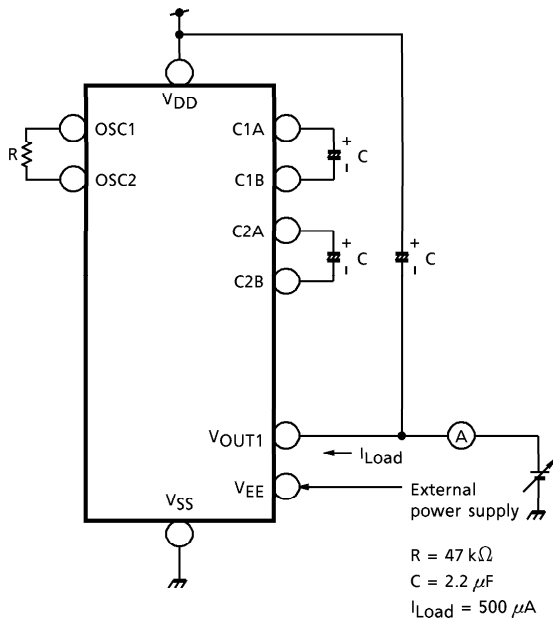


4.

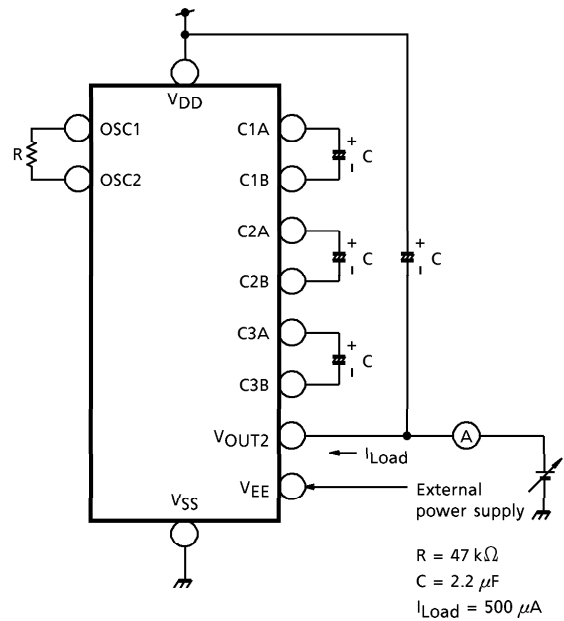


(*) : /LE, /WR, DB to DB5 connected to V_{DD}

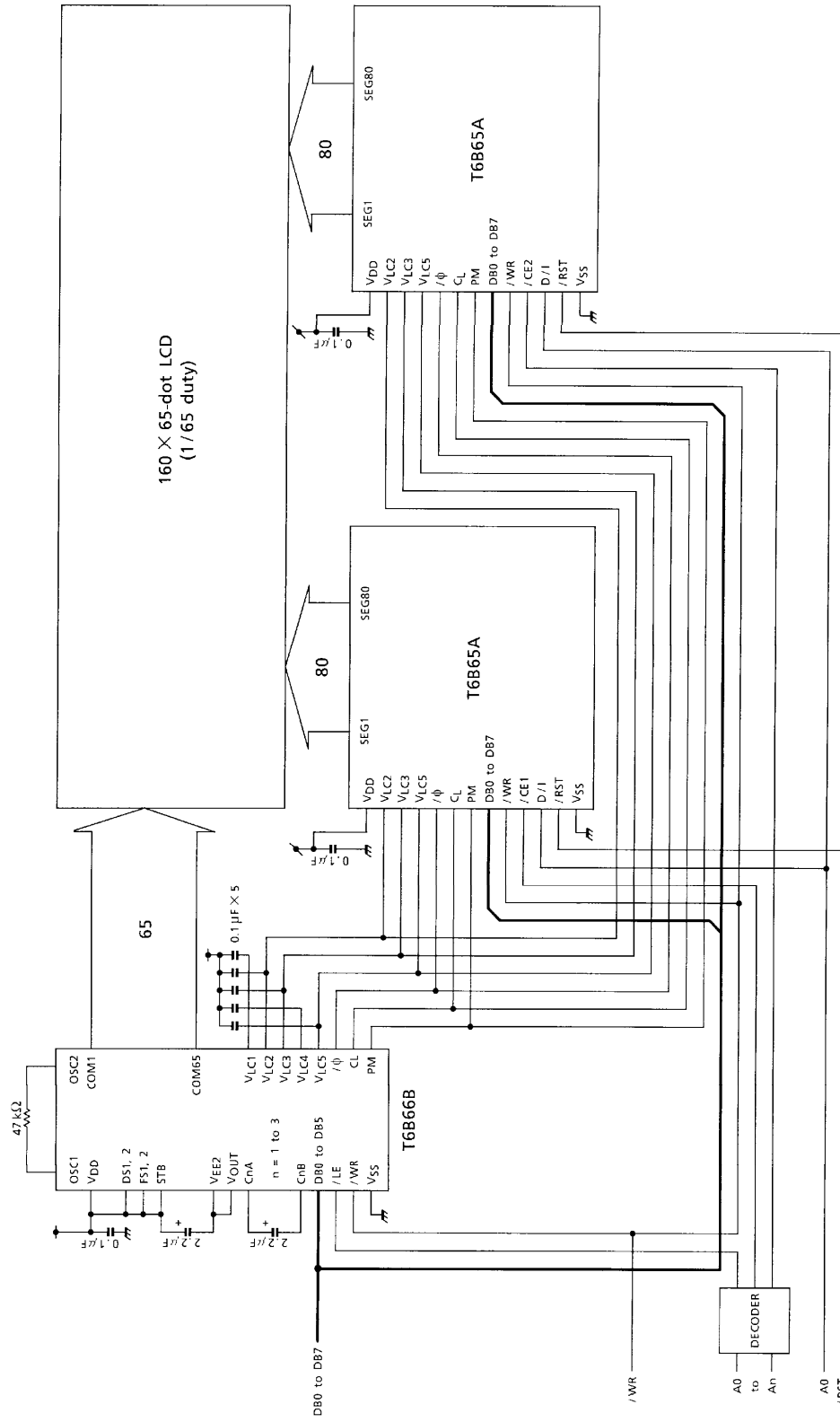
5. Tripler mode



6. Quadrupler mode

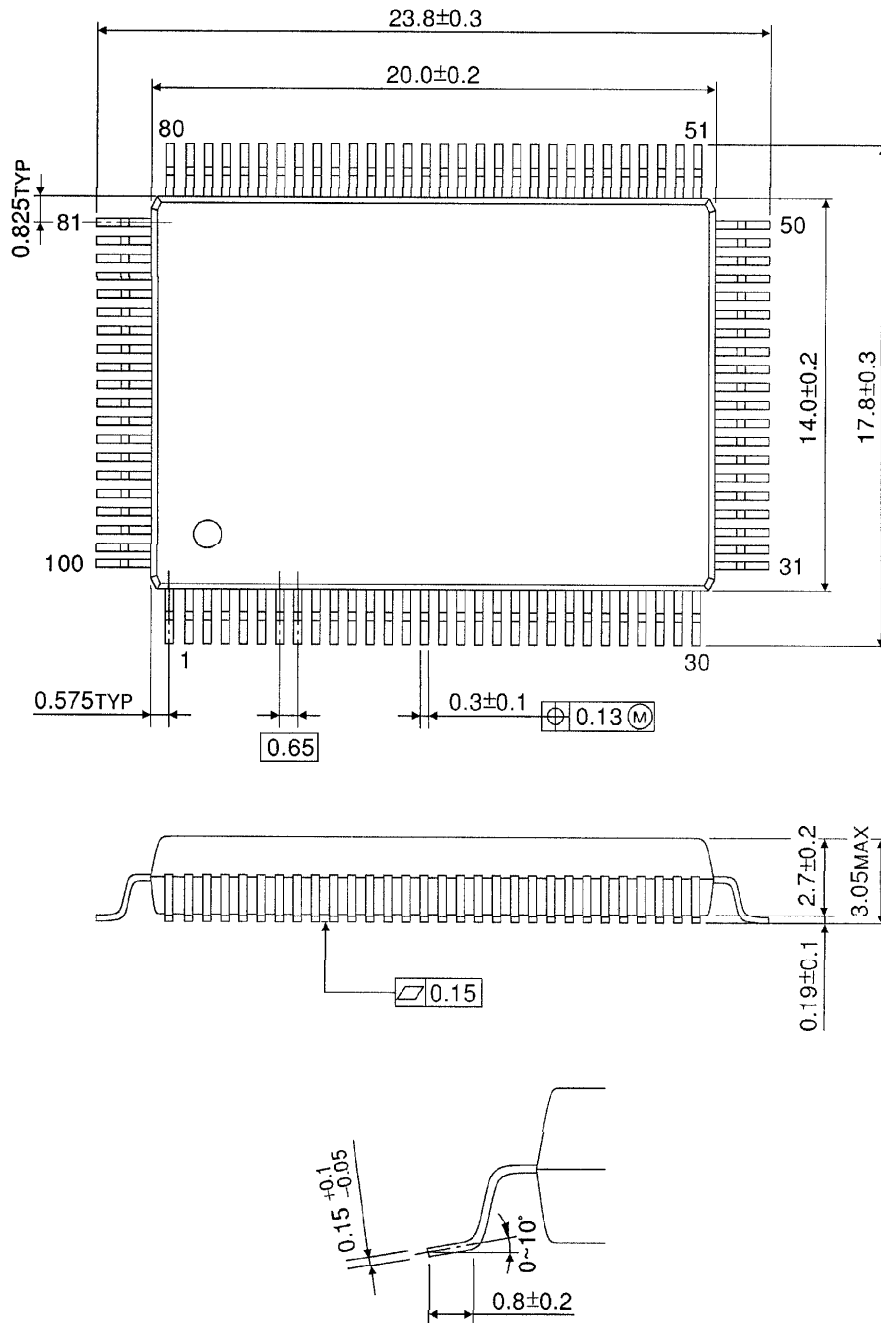


APPLICATION CIRCUIT (1)



OUTLINE DRAWING
QFP100-P-1420-0.65A

Unit : mm



Weight : 1.6 g (typ.)