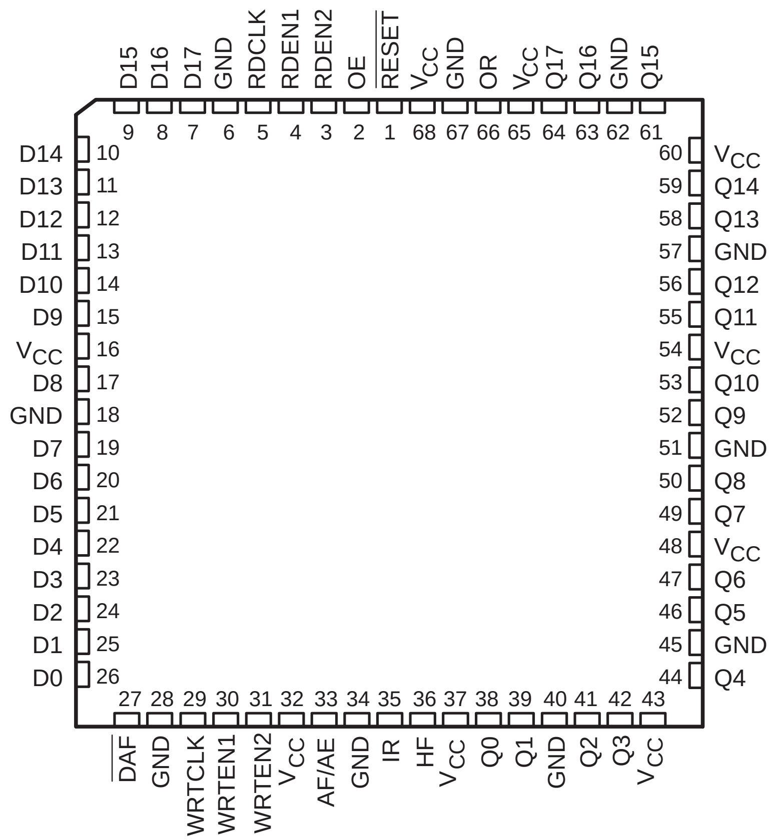
- **Member of the Texas Instruments Widebus™ Family**
- **Independent Asynchronous Inputs and Outputs**
- **Read and Write Operations Can Be Synchronized to Independent System Clocks**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Pin-to-Pin Compatible With SN74ACT7882, SN74ACT7884, and SN74ACT7811**
- **Input-Ready, Output-Ready, and Half-Full Flags**
- **Cascadable in Word Width and/or Word Depth**
- **Fast Access Times of 13 ns With a 50-pF Load**
- **High Output Drive for Direct Bus Interface**
- **Released as DSCC SMD (Standard Microcircuit Drawing) 5962-9562701QYA and 5962-9562701NXD**
- **Package Options Include 68-Pin Ceramic Quad Flat (HV) and 80-Pin Plastic Quad Flat (PN) Packages**

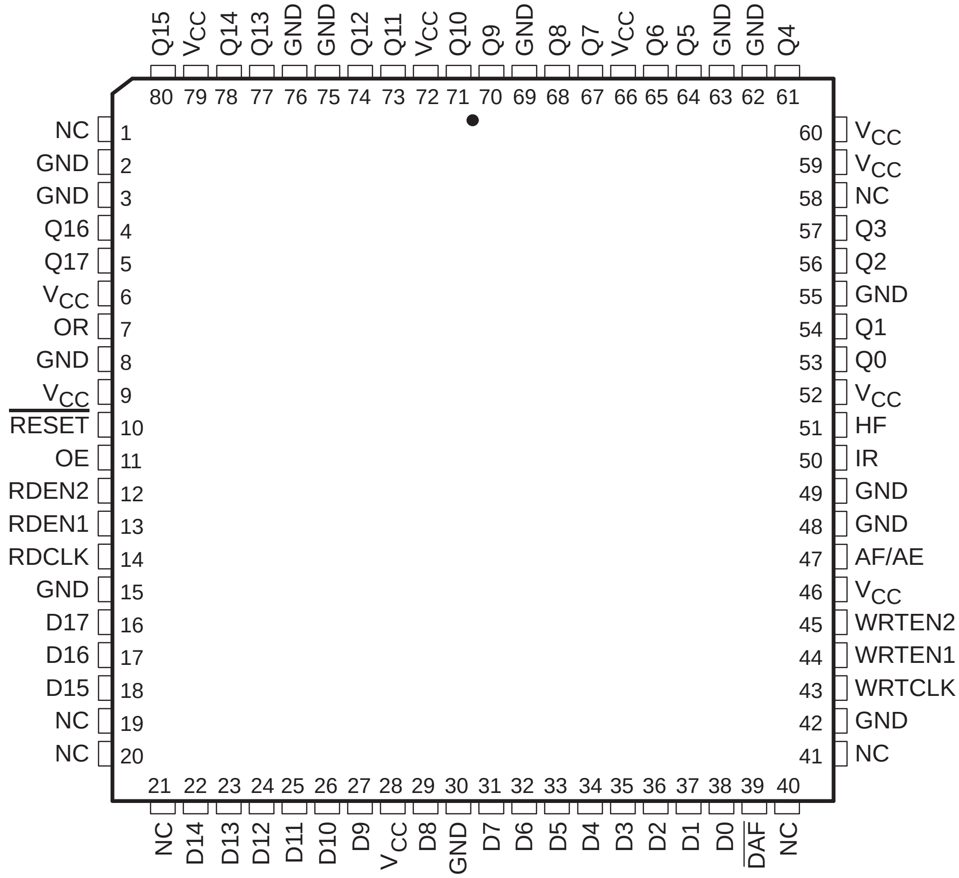
HV PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments Incorporated.

PN PACKAGE
(TOP VIEW)



NC – No internal connection

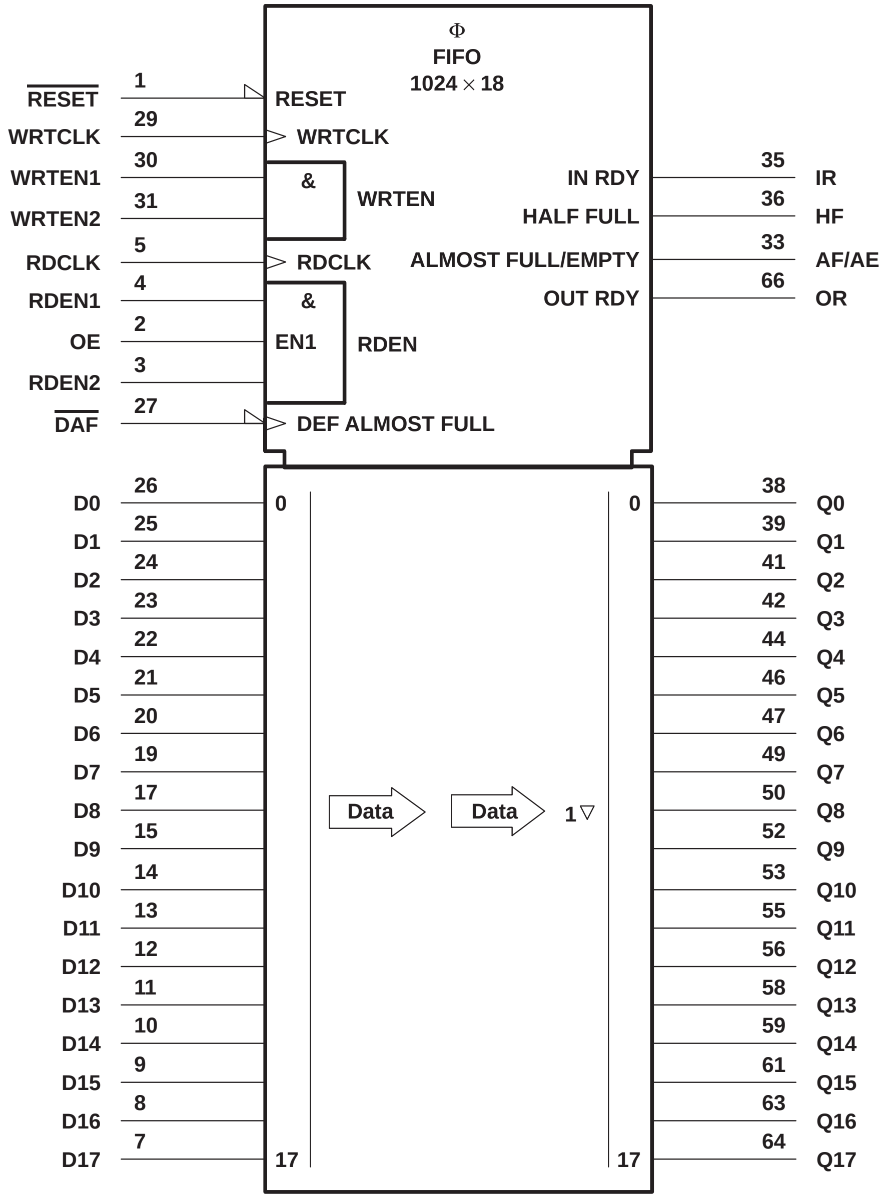
description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN54ACT7881 is organized as 1024 × 18 bits and processes data with rates up to 50 MHz and access times of 13 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is accomplished easily in both word width and word depth.

The SN54ACT7881 has normal input-bus to output-bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent reads and writes to their respective system clocks.

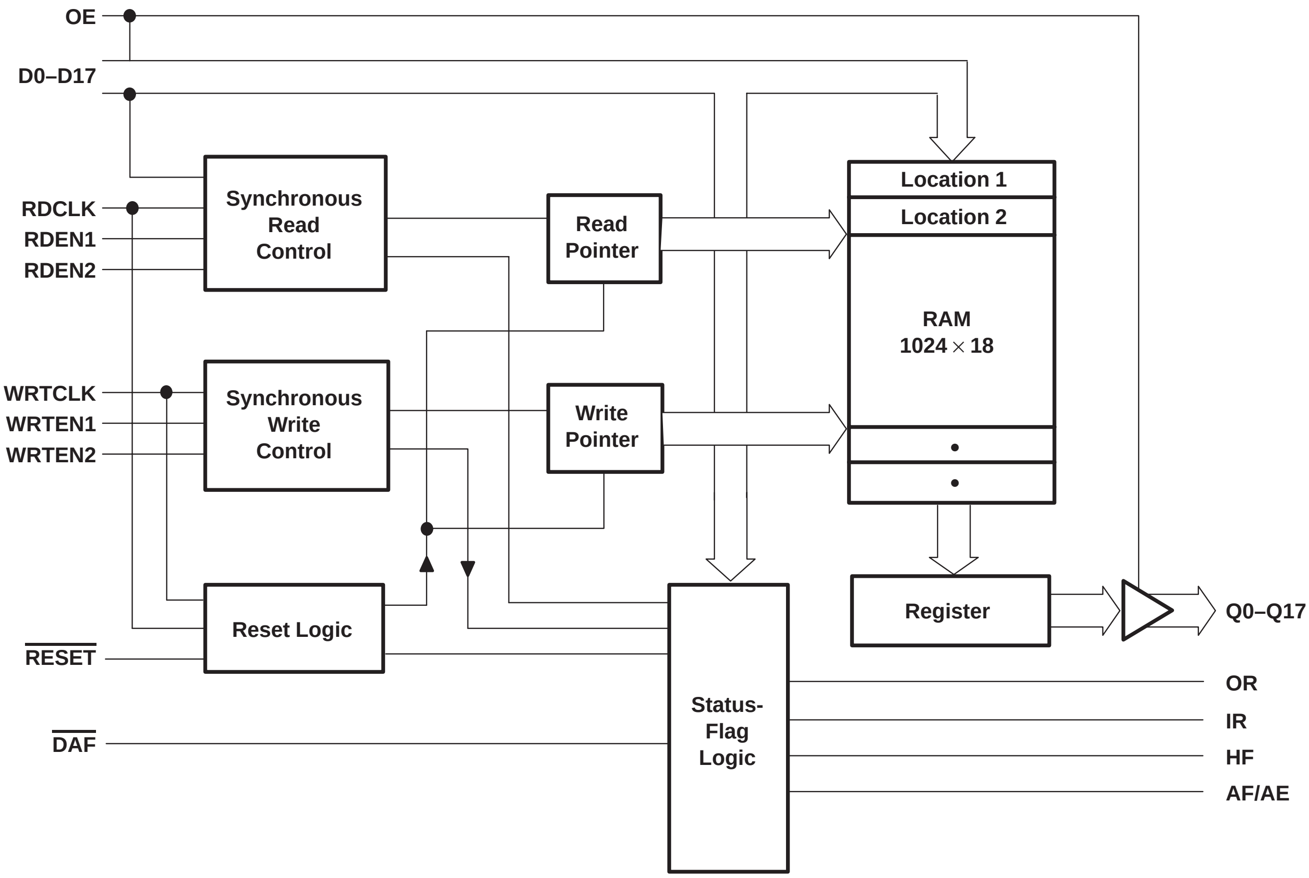
The SN54ACT7881 is characterized for operation over the full military temperature range of –55°C to 125°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the HV package.

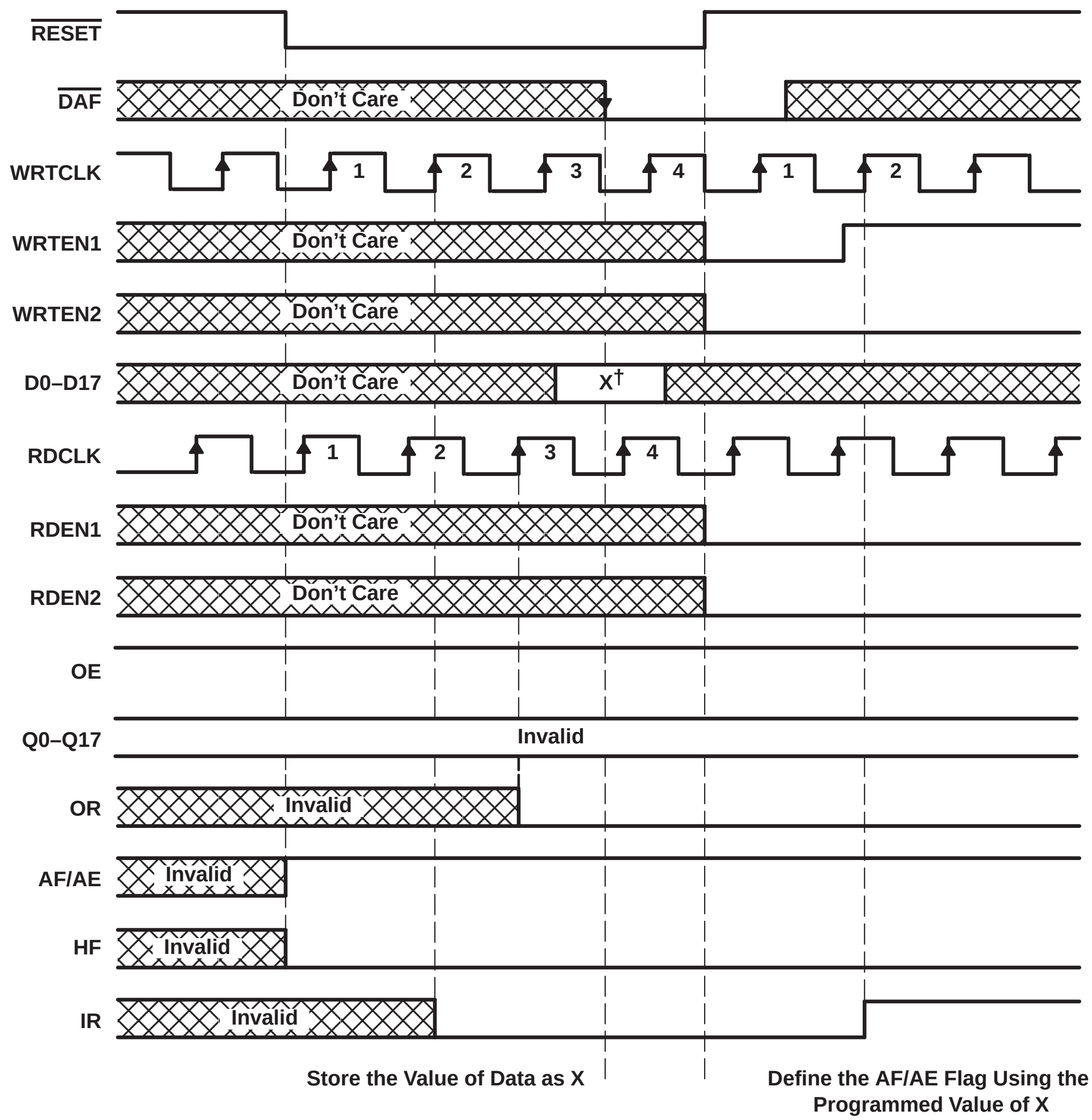
functional block diagram



Terminal Functions

TERMINAL† NAME	TERMINAL† NO.	I/O	DESCRIPTION
AF/AE	47	O	Almost-full/almost-empty flag. The AF/AE boundary is defined by the AF/AE offset value (X). This value can be programmed during reset, or the default value of 256 can be used. AF/AE is high when the FIFO contains (X + 1) or fewer words or (1025 – X) or more words. AF/AE is low when the FIFO contains between (X + 2) and (1024 – X) words. Programming procedure for AF/AE – The AF/AE flag is programmed during each reset cycle. The AF/AE offset value (X) is either a user-defined value or the default of X = 256. Instructions to program AF/AE using both methods are as follows: **User-defined X** Step 1: Take $\overline{\text{DAF}}$ from high to low. Step 2: If $\overline{\text{RESET}}$ is not already low, take $\overline{\text{RESET}}$ low. Step 3: With $\overline{\text{DAF}}$ held low, take $\overline{\text{RESET}}$ high. This defines the AF/AE using X. Step 4: To retain the current offset for the next reset, keep $\overline{\text{DAF}}$ low. **Default X** To redefine AF/AE using the default value of X = 256, hold $\overline{\text{DAF}}$ high during the reset cycle.
$\overline{\text{DAF}}$	39	I	Define-almost-full. The high-to-low transition of $\overline{\text{DAF}}$ stores the binary value of data inputs as the AF/AE offset value (X). With $\overline{\text{DAF}}$ held low, a low pulse on $\overline{\text{RESET}}$ defines the AF/AE flag using X.
D0–D17	18–16, 27–22, 29, 38–31	I	Data inputs for 18-bit-wide data to be stored in the memory. A high-to-low transition of $\overline{\text{DAF}}$ captures data for the AF/AE offset (X) from D8–D0.
HF	51	O	Half-full flag. HF is high when the FIFO contains 512 or more words and is low when the number of words in memory is less than half the depth of the FIFO.
IR	50	O	Input-ready flag. IR is high when the FIFO is not full and low when the device is full. During reset, IR is driven low on the rising edge of the second WRTCLK pulse. IR is then driven high on the rising edge of the second WRTCLK pulse after $\overline{\text{RESET}}$ goes high. After the FIFO is filled and IR is driven low, IR is driven high on the second WRTCLK pulse after the first valid read.
OE	11	I	Output enable. The Q0–Q17 outputs are in the high-impedance state when OE is low. OE must be high before the rising edge of RDCLK to read a word from memory.
OR	7	O	Output-ready flag. OR is high when the FIFO is not empty and low when the FIFO is empty. During reset, OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.
Q0–Q17	4, 5, 53, 54, 56, 57, 61, 64, 65, 67, 68, 70, 71, 73, 74, 77, 78, 80,	O	Data outputs. The first data word to be loaded into the FIFO is moved to Q0–Q17 on the rising edge of the third RDCLK pulse to occur after the first valid write. RDEN1 and RDEN2 do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, OE, and OR are high.
RDCLK	14	I	Read clock. Data is read out of memory on the low-to-high transition of RDCLK if OR, OE, RDEN1, and RDEN2 are high. RDCLK is a free-running clock and functions as the synchronizing clock for all data transfers out of the FIFO. OR also is driven synchronously with respect to RDCLK.
RDEN1 RDEN2	13 12	I	Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to read a word out of memory. RDEN1 and RDEN2 are not used to read the first word stored in memory.
$\overline{\text{RESET}}$	10	I	Reset. A reset is accomplished by taking $\overline{\text{RESET}}$ low and generating a minimum of four RDCLK and WRTCLK cycles. This ensures that the internal read and write pointers are reset and that OR, HF, and IR are low, and AF/AE is high. The FIFO must be reset upon power up. With $\overline{\text{DAF}}$ at a low level, a low pulse on $\overline{\text{RESET}}$ defines AF/AE using the AF/AE offset value (X), where X is the value previously stored. With $\overline{\text{DAF}}$ at a high level, a low-level pulse on $\overline{\text{RESET}}$ defines the AF/AE flag using the default value of X = 256.
WRTCLK	29	I	Write clock. Data is written into memory on a low-to-high transition of WRTCLK if IR, WRTEN1, and WRTEN2 are high. WRTCLK is a free-running clock and functions as the synchronizing clock for all data transfers into the FIFO. IR also is driven synchronously with respect to WRTCLK.
WRTEN1 WRTEN2	30 31	I	Write enable. WRTEN1 and WRTEN2 must be high before a rising edge on WRTCLK for a word to be written into memory. WRTEN1 and WRTEN2 do not affect the storage of the AF/AE offset value (X).

† Terminals listed are for the PN package.



† X is the binary value on D8–D0.

Figure 1. Reset Cycle: Define AF/AE Flag Using a Programmed Value of X

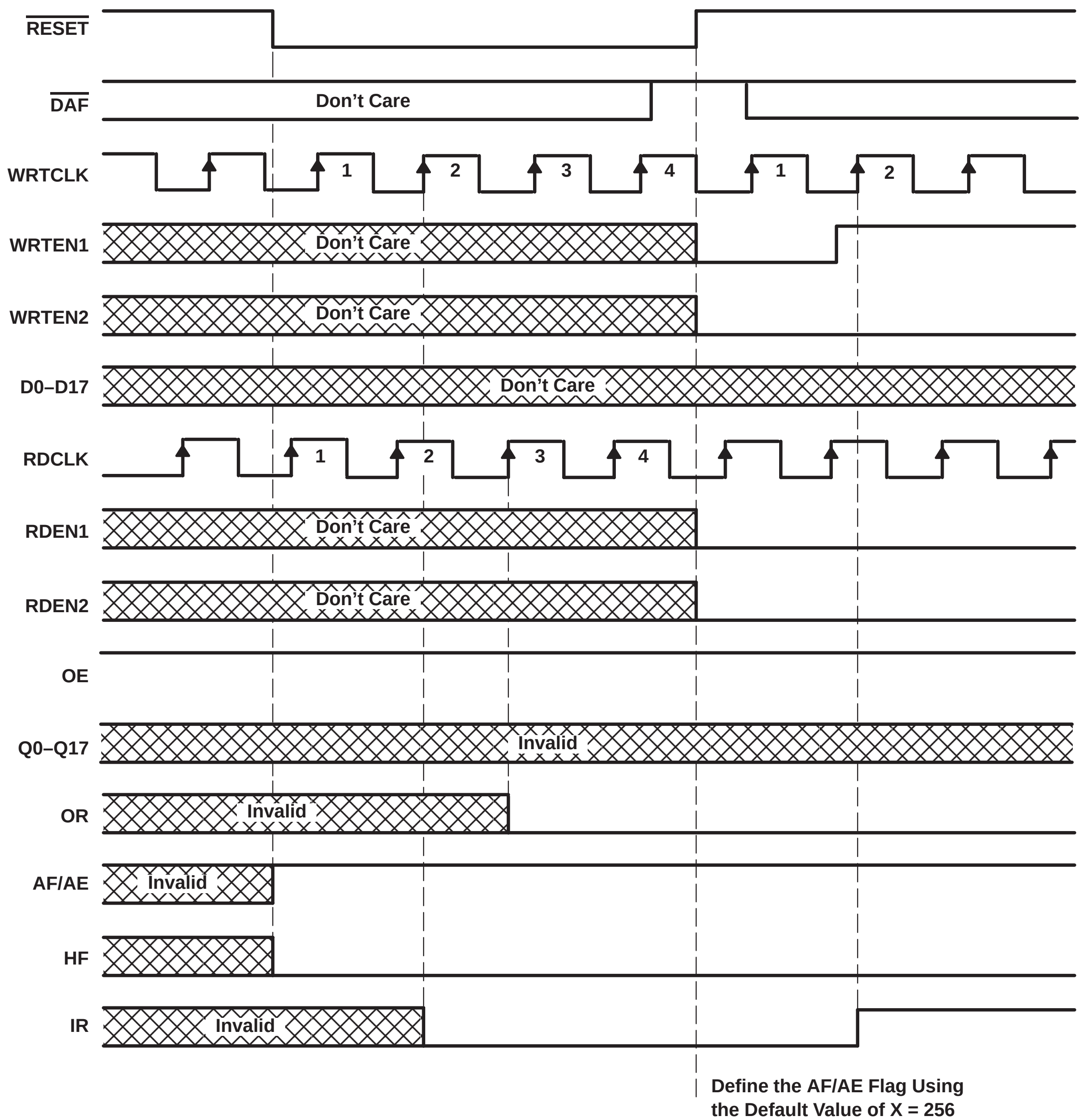
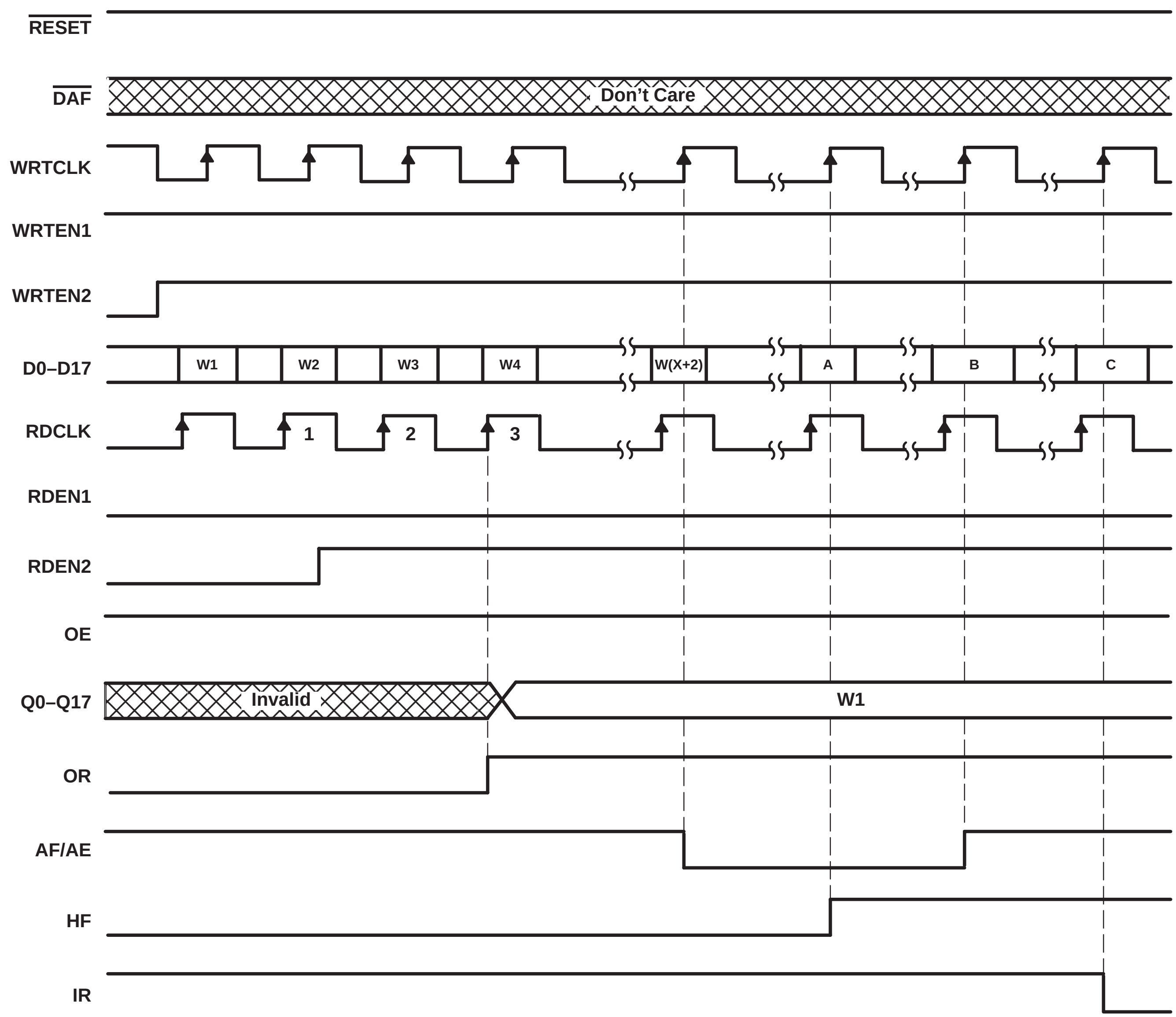


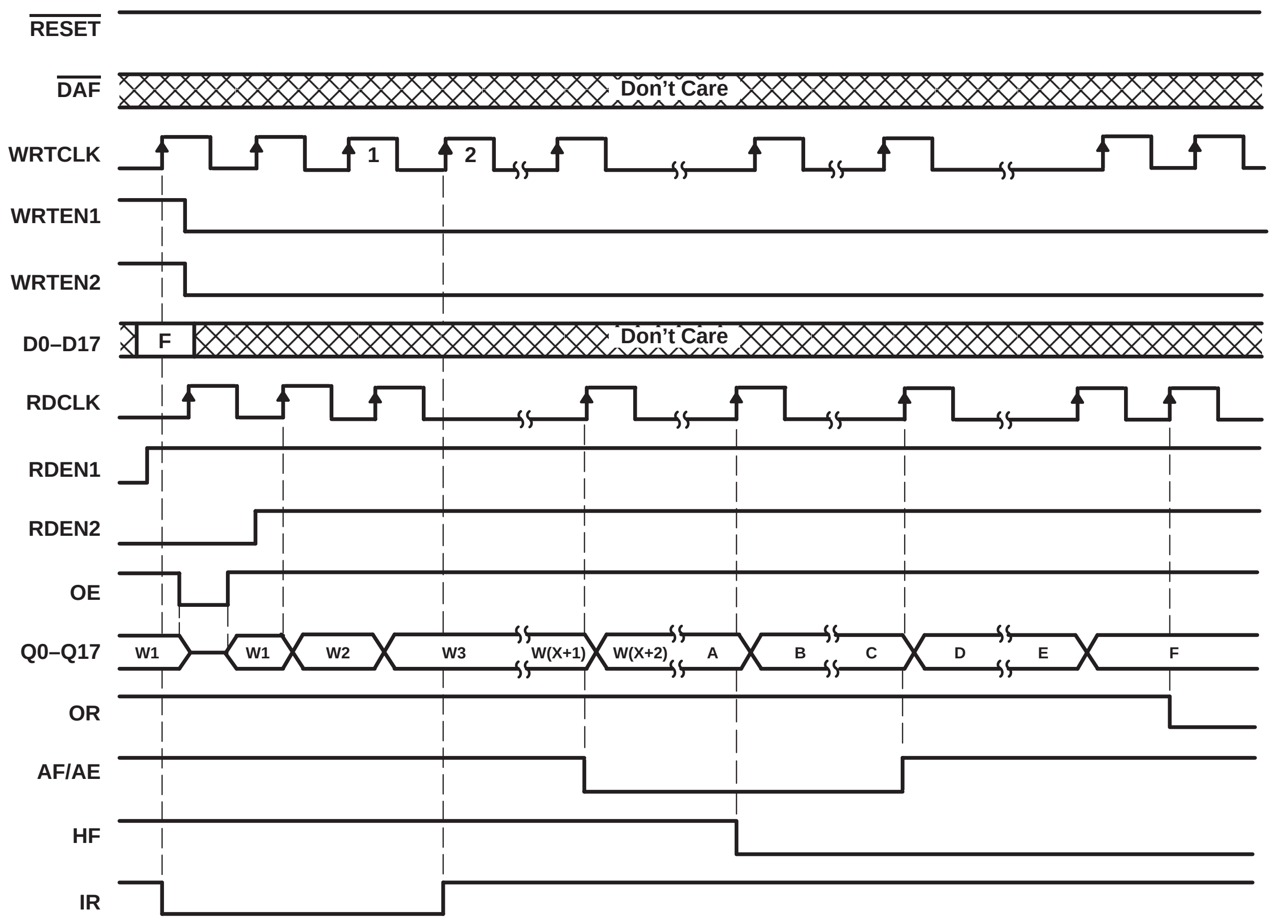
Figure 2. Reset Cycle: Define AF/AE Flag Using the Default Value of X = 256



DATA-WORD NUMBERS FOR FLAG TRANSITIONS

TRANSITION WORD		
A	**B**	**C**
W513	W(1025 – X)	W1025

Figure 3. Write Cycle



DATA-WORD NUMBERS FOR FLAG TRANSITIONS

TRANSITION WORD					
A	**B**	**C**	**D**	**E**	**F**
W513	W514	W(1024 – X)	W(1025 – X)	W1024	W1025

Figure 4. Read Cycle

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input voltage range, V_I . . . . –0.5 V to 7 V
Voltage range applied to a disabled 3-state output . . . . –0.5 V to 5.5 V
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		16	mA
T_A	Operating free-air temperature	–55	125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –8 mA	2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 16 mA			0.5	V
I_I	V_{CC} = 5.5 V,	$V_I = V_{CC}$ or 0			±5	µA
I_{OZ}	V_{CC} = 5.5 V,	$V_O = V_{CC}$ or 0			±5	µA
I_{CC}§	$V_I = V_{CC}$ – 0.2 V or 0				400	µA
	One input at 3.4 V,	Other inputs at V_{CC} or GND			1.2	mA
C_i	V_I = 0,	f = 1 MHz		4		pF
C_o	V_O = 0,	f = 1 MHz		8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ I_{CC} is tested with outputs open.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 4)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			50	MHz
t_w	Pulse duration	WRTCLK high	7		ns
		WRTCLK low	7.5		
		RDCLK high	7		
		RDCLK low	7		
		$\overline{\text{DAF}}$ high	7		
t_{su}	Setup time	D0–D17 before WRTCLK↑	5		ns
		WRTEN1, WRTEN2 high before WRTCLK↑	5		
		OE, RDEN1, RDEN2 high before RDCLK↑	5		
		Reset: $\overline{\text{RESET}}$ low before first WRTCLK↑ and RDCLK↑†	6*		
		Define AF/AE: D0–D8 before $\overline{\text{DAF}}$↓	5		
		Define AF/AE: $\overline{\text{DAF}}$↓ before $\overline{\text{RESET}}$↑	6		
		Define AF/AE (default): $\overline{\text{DAF}}$ high before $\overline{\text{RESET}}$↑	5		
t_h	Hold time	D0–D17 after WRTCLK↑	0		ns
		WRTEN1, WRTEN2 high after WRTCLK↑	0		
		OE, RDEN1, RDEN2 high after RDCLK↑	0.5		
		Reset: $\overline{\text{RESET}}$ low after fourth WRTCLK↑ and RDCLK↑†	0*		
		Define AF/AE: D0–D8 after $\overline{\text{DAF}}$↓	1		
		Define AF/AE: $\overline{\text{DAF}}$ low after $\overline{\text{RESET}}$↑	0		
		Define AF/AE (default): $\overline{\text{DAF}}$ high after $\overline{\text{RESET}}$↑	0		

* On products compliant to MIL-PRF-38535, this parameter is not production tested .
† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 5)

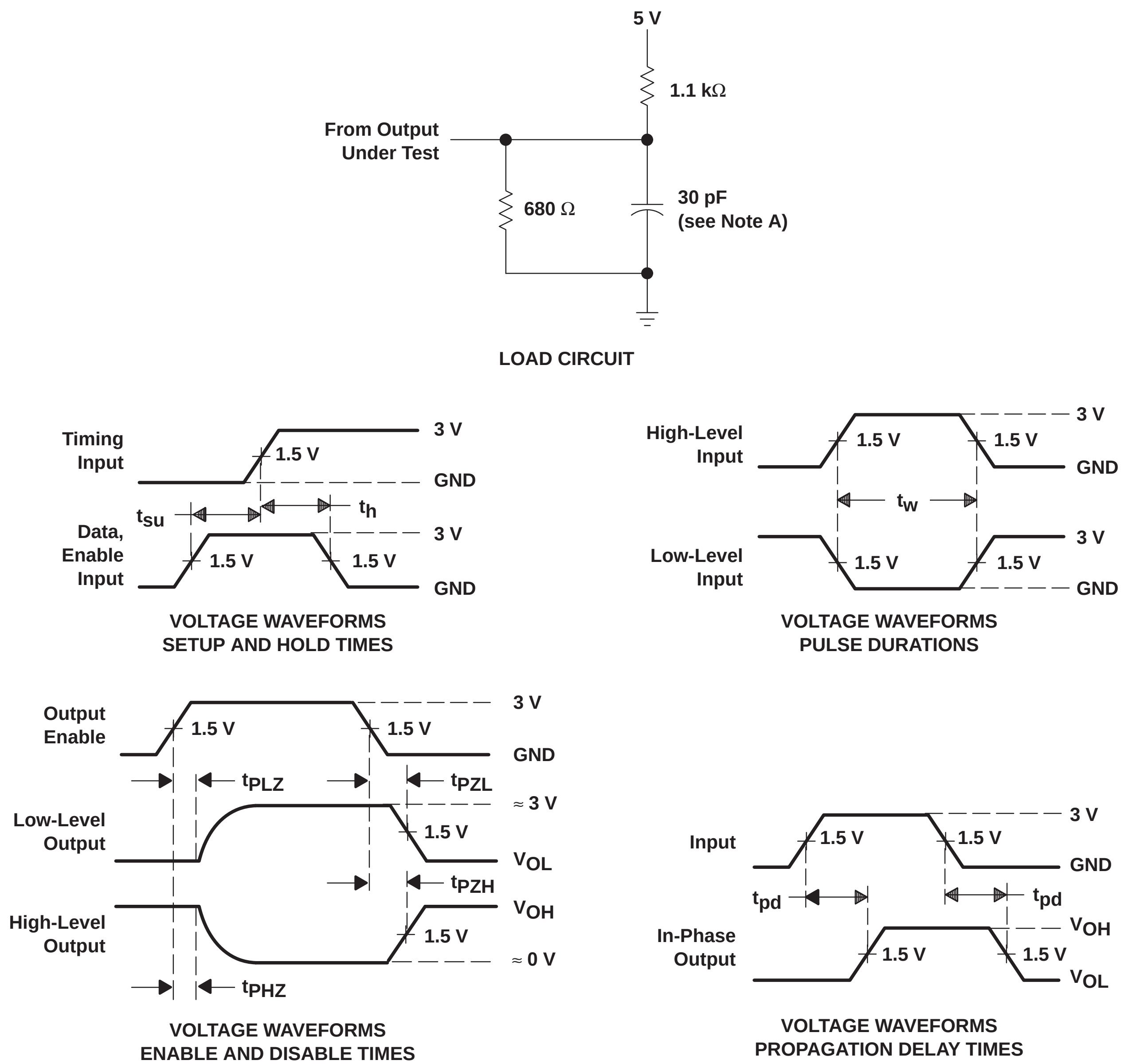
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}	WRTCLK or RDCLK		50		MHz
t_{pd}	RDCLK↑	Any Q	3	13	ns
t_{pd}‡	RDCLK↑	Any Q			ns
t_{pd}	WRTCLK↑	IR	2	9.5	ns
	RDCLK↑	OR	2	9.5	
	WRTCLK↑	AF/AE	6	19	
	RDCLK↑		6	19	
t_{PLH}	WRTCLK↑	HF	6	17	ns
t_{PHL}	RDCLK↑	HF	6	17	ns
t_{PLH}	$\overline{\text{RESET}}$↓	AF/AE	3	17	ns
t_{PHL}	$\overline{\text{RESET}}$↓	HF	3	19	ns
t_{en}	OE	Any Q	2	11	ns
t_{dis}	OE	Any Q	2	14	ns

‡ This parameter is measured with C_L = 30 pF (see Figure 5).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per 1K bits	C_L = 50 pF, f = 5 MHz	65	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Includes probe and jig capacitance
B. t_{PZL} and t_{PZH} are the same as t_{en}.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

Figure 5. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

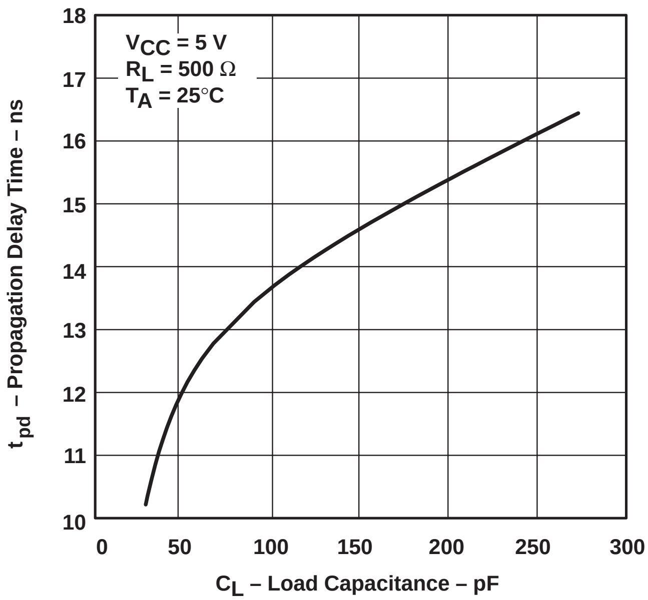


Figure 6

POWER-DISSIPATION CAPACITANCE
vs
SUPPLY VOLTAGE

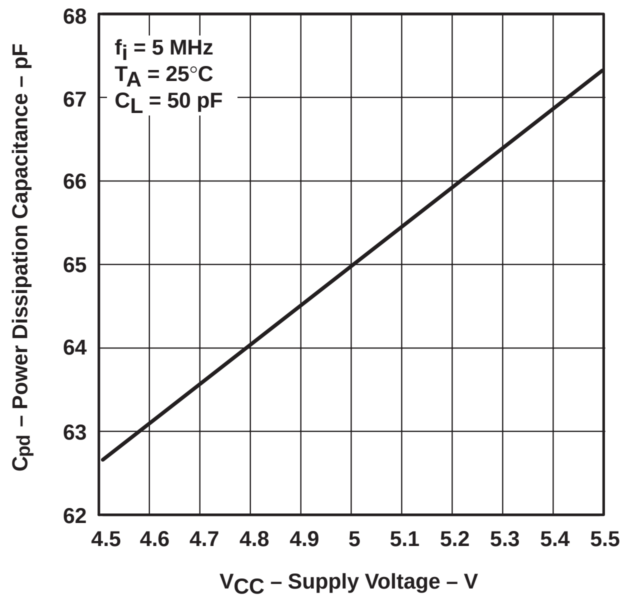


Figure 7

APPLICATION INFORMATION

expanding the SN54ACT7881

The SN54ACT7881 is expandable in both word width and word depth. Word-depth expansion is accomplished by connecting the devices in series such that data flows through each device in the chain. Figure 9 shows two SN54ACT7881 devices configured for word-depth expansion. The common clock between the devices can be tied to either the write clock (WRTCLK) of the first device or the read clock (RDCLK) of the last device. The output-ready flag (OR) of the previous device and the input-ready flag (IR) of the next device maintain data flow to the last device in the chain whenever space is available.

Figure 10 shows two SN54ACT7881 devices in word-width expansion. Word-width expansion is accomplished by simply connecting all common control signals between the devices and creating composite input-ready (IR) and output-ready (OR) signals. The almost-full/almost-empty flag (AF/AE) and half-full flag (HF) can be sampled from any one device. Word-depth expansion and word-width expansion can be used together.

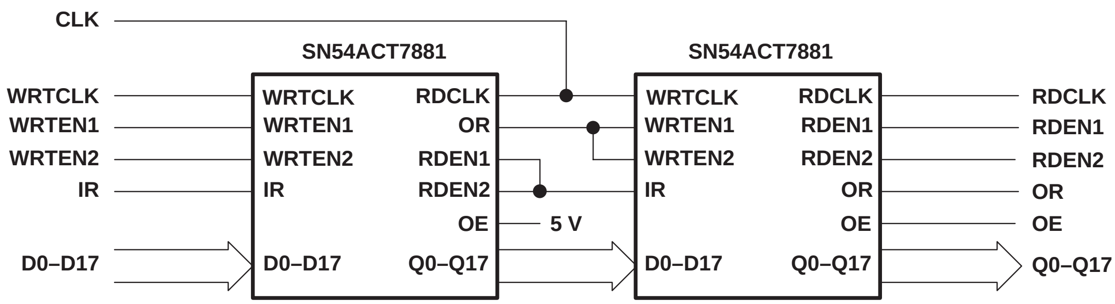


Figure 8. Word-Depth Expansion: 2048/4096/8192 Words × 18 Bits, N = 2

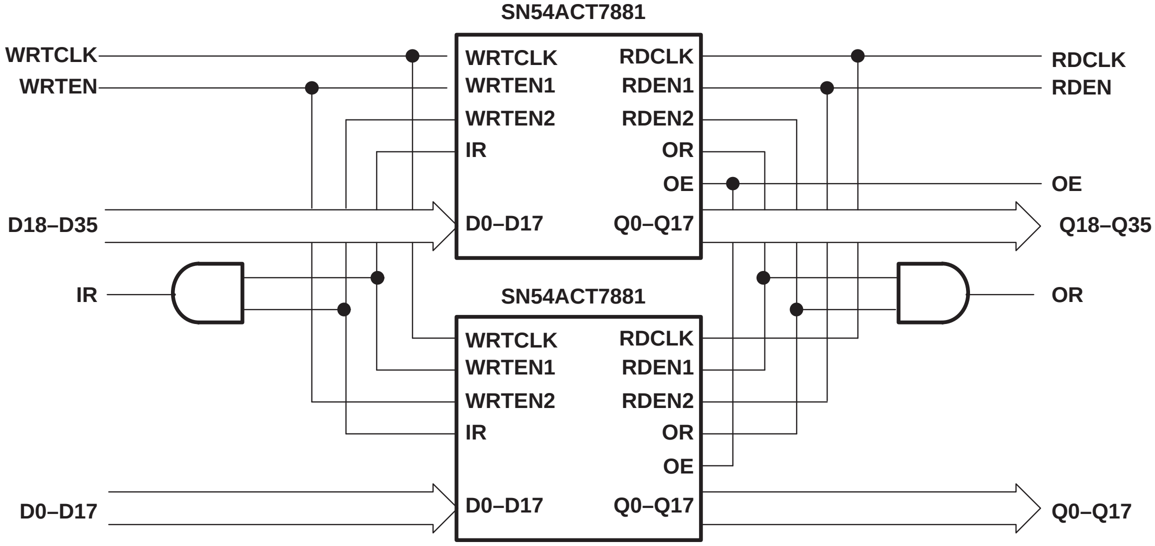


Figure 9. Word-Width Expansion: 1024 Words × 36 Bits

IMPORTANT NOTICE