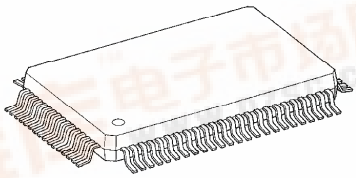
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T7932

COLUMN DRIVER LSI FOR A DOT MATRIX GRAPHIC LCD

The T7932 is a column (segment) driver for a small- or medium-scale dot matrix graphic LCD. The T7932 realizes a low power LCD system using the CMOS Si-Gate process. The T7932 stores 4-bit / 8-bit display data transferred from a microprocessor. The built-in display RAM image corresponds to the LCD screen and the data is converted to an LCD drive signal. The T7932 can be combined with a T7933 to construct an LCD system. An MPU can drive the T7932 directly.



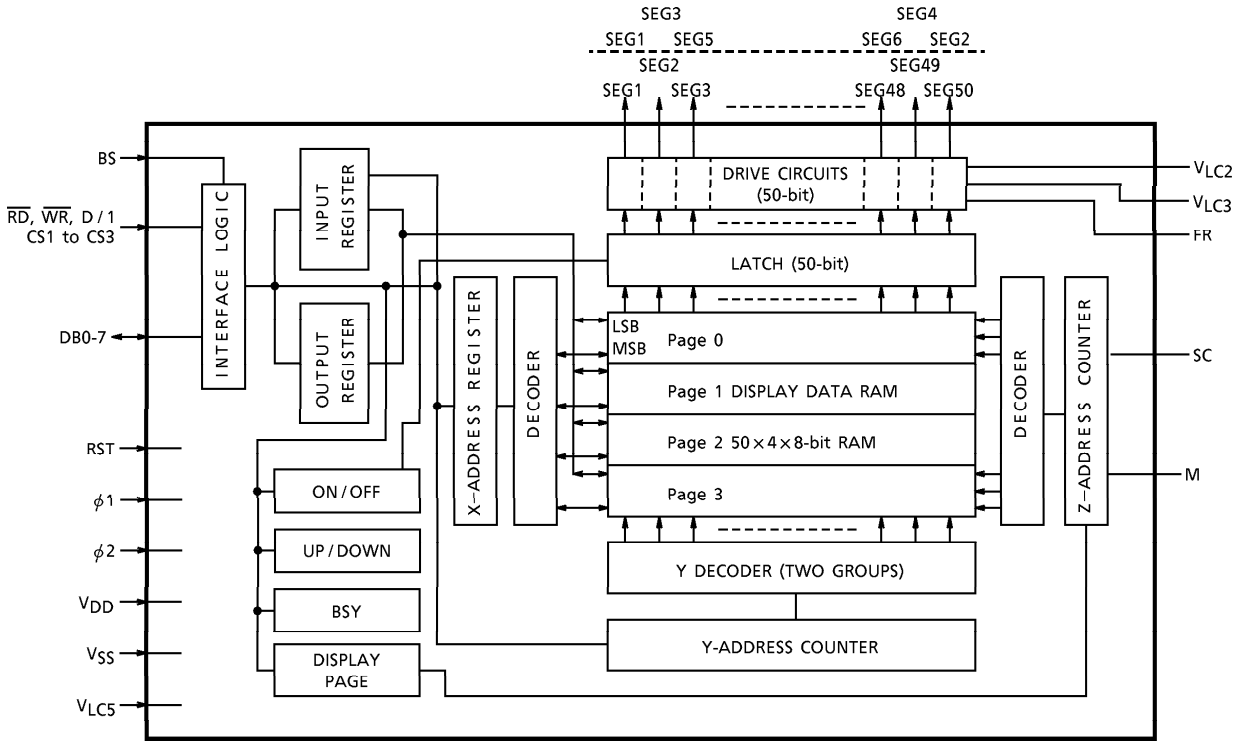
QFP80-P-1420-0.80A

Weight: 1.5g (typ.)

FEATURES

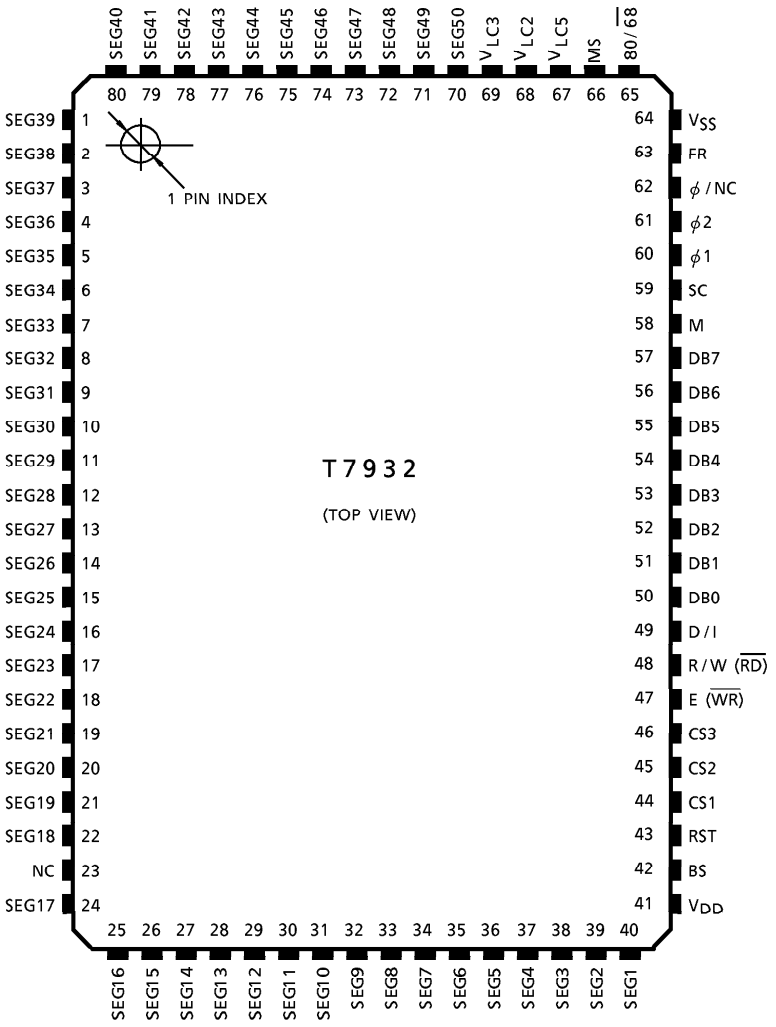
- Dot matrix graphic LCD column driver with display RAM.
- Interface : with 80-series MPU and 68-series MPU (4-bit / 8-bit)
- Selectable column output pin arrangement
  (Optional mode : odd / even separate mode)
- Relation of RAM data ↔ Display
  ① RAM bit data 1…ON
  ② RAM bit data 0…OFF
- Display RAM capacity : 50 × 8 × 4 = 1600 bits
- LCD drive output : 50
- Duty : Can be controlled by external input signal.
- Various functions
  Display Data Read / Write, Display ON / OFF, Set Address, Set Display Start Page, Read Status, Set Up / Down mode
- Low power consumption
- Logic power supply : 5V ± 10%
- 80-pin flat plastic package

BLOCK DIAGRAM



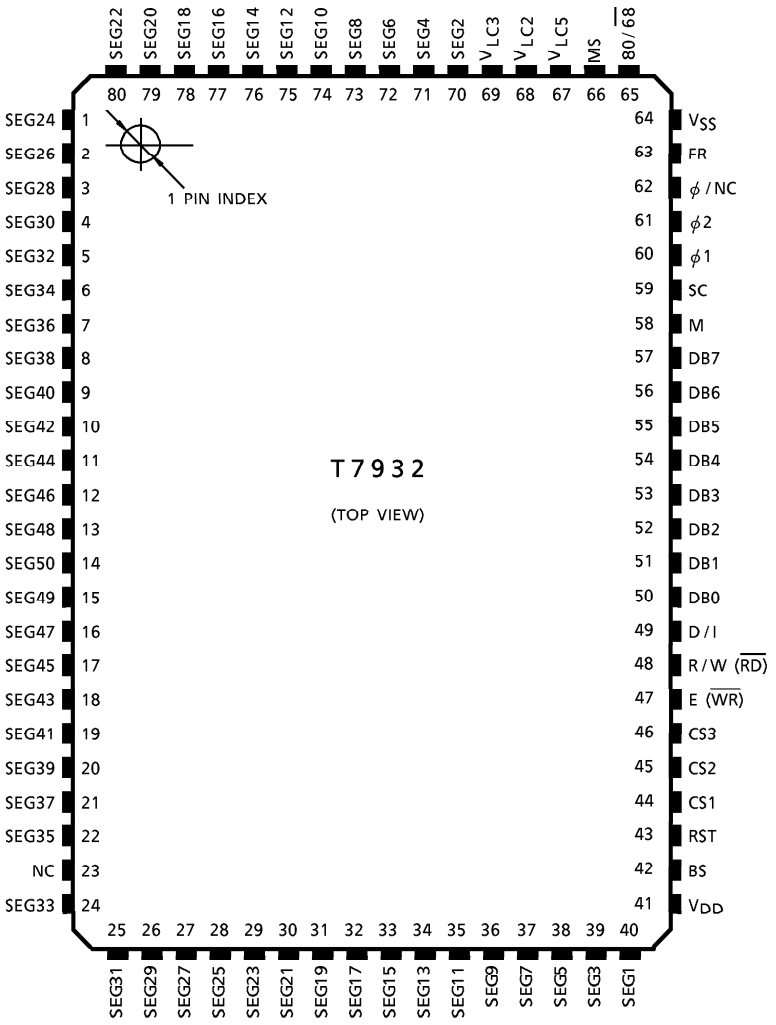
PIN ASSIGNMENT

(MS = H)



PIN ASSIGNMENT

(MS = L)



PIN FUNCTIONS

<table>
<tr><th>PIN NAME</th><th>I/O</th><th>FUNCTIONS</th><th>LEVEL</th></tr>
<tr><td>SEG1 to SEG50</td><td>Output</td><td>LCD drive signal outputs</td><td>V_{DD} to V_{LC5}</td></tr>
<tr><td>CS1 to CS3</td><td>Input</td><td>Chip select
<table>
<tr><th>CS1</th><th>CS2</th><th>CS3</th><th>STATE</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>disable</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>disable</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>disable</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>READ/WRITE enable</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>WRITE enable only</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>WRITE enable only</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>WRITE enable only</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>READ/WRITE enable</td></tr>
</table></td><td>V_{DD} to V_{SS}</td></tr>
<tr><td>E ($\overline{WR}$)</td><td>Input</td><td>① E (68-series MPU)
● R/W = L write data : Data of DB0 to DB7 latch to the input register at the falling edge of E.
● R/W = H read data : Data of DB0 to DB7 output to MPU when E = H
② $\overline{WR}$ (80-series MPU)
● Write operation : Data of DB0 to DB7 latch to the input register at the rising edge of $\overline{WR}$.</td><td>V_{DD} to V_{SS}</td></tr>
<tr><td>R/W ($\overline{RD}$)</td><td>Input</td><td>① R/W (68-series MPU)
● R/W = H : Data output to MPU when E = H and CS2, CS3 = H.
● R/W = L : The input register can accept data when CS2, CS3 = H or CS1 = H.
② $\overline{RD}$ (80-series MPU)
● $\overline{RD}$ = L : Data output to MPU when CS2, CS3 = H.
● $\overline{RD}$ = H : The input register can accept data when CS2, CS3 = H or CS1 = H.</td><td>V_{DD} to V_{SS}</td></tr>
<tr><td>D/I</td><td>Input</td><td>Select data/instruction
D/I = H : Data DB0 to DB7 is display data.
D/I = L : Data DB0 to DB7 is instruction data.</td><td>V_{DD} to V_{SS}</td></tr>
<tr><td>DB0 to DB7</td><td>I/O</td><td>Data bus : bi-directional three-state bus.
<table>
<tr><th>E ($\overline{WR}$)</th><th>R/W ($\overline{RD}$)</th><th>CS1</th><th>CS2</th><th>CS3</th><th>STATE OF DB0 TO DB7</th></tr>
<tr><td>H</td><td>H</td><td>*</td><td>H</td><td>H</td><td>Output</td></tr>
<tr><td>*</td><td>L</td><td>H</td><td>*</td><td>*</td><td rowspan="2">Input</td></tr>
<tr><td>*</td><td>L</td><td>*</td><td>H</td><td>H</td></tr>
<tr><td colspan="5">OTHERS</td><td>High impedance</td></tr>
</table>
* : Don't Care
(Note) 68-series MPU</td><td>V_{DD} to V_{SS}</td></tr>
</table>

PIN NAME	I/O	FUNCTIONS	LEVEL
FR	Input	Frame signal	V_{DD} to V_{SS}
SC	Input	Shift Clock Pulse T7932 output column signal corresponds to display data synchronized to the rising edge of SC.	V_{DD} to V_{SS}
M	Input	Display synchronous signal M sets the 5-bit display line counter and synchronizes a row signal to the frame timing when M becomes high.	V_{DD} to V_{SS}
ϕ1, ϕ2	Input	2-phase clock signal for internal operation	V_{DD} to V_{SS}
80 / $\overline{68}$	Input	Select CPU type 80 / $\overline{68}$ = H : 80-series MPU 80 / $\overline{68}$ = L : 68-series MPU	V_{DD} to V_{SS}
ϕ / NC	Input	80 / $\overline{68}$ = H : input terminal for ϕ or CLK signal. 80 / $\overline{68}$ = L : not connected	V_{DD} to V_{SS}
RST	Input	Reset signal RST = L sets display OFF, and sets mode to Y-address counter. Maintains this state until changed by another command.	V_{DD} to V_{SS}
BS	Input	Bus select BS = L : 8-bit interface (DB0 to DB7) BS = H : 4-bit interface (DB4 to DB7) first send upper 4 bits, then lower 4 bits.	V_{DD} to V_{SS}
MS	Input	Select pin assignment MS = L : Optional mode (odd / even output) MS = H : Normal output * See PIN ASSIGNMENT	V_{DD} to V_{SS}
V_{LC2}	Input	Power supply for LCD drive	—
V_{LC3}	Input	Power supply for LCD drive	
V_{LC5}	Input	Power supply for LCD drive	
V_{DD}	Input	Logic power supply (5.0V)	
V_{SS}	Input	Logic power supply (0V)	

FUNCTION OF EACH BLOCK

- Interface

  The T7932 can interface to a 4-bit or 8-bit MPU.

  (1) 4-bit mode (BS = H)

  The T7932 can transfer 8-bit data (4 bits × 2) when BS = H. The T7932 uses the upper 4 bits (DB4 to DB7) for data transfer. The upper 4 bits are transferred first, then the lower 4 bits.

  (2) 8-bit mode (BS = L)

  When BS is held at L, the T7932 uses DB0 to DB7 to data transfer.

- Input register

  8-bit data from the MPU is latched to this register. The D / I signal distinguishes between instruction data and display data.

- Output register

  8-bit data is read from the display RAM, latched to the output register, and the address is automatically incremented or decremented by 1. The MPU cannot read correct data on the first data reading, but reads the correct data on the second read operation.

- X-address register

  This register stores a page address for display RAM reading or writing.

- Y-address counter

  The Y-address counter has a 50-bit Up / Down counter. The T7932 increases or decreases the address with the display data read / write operation. The Up / Down mode and start address are determined by the instruction. RST = L sets Up mode for this counter.

- Z-address counter

  The counter points to the row of display data which will be displayed next. The senior two bits hold the page numbers, and the lower three bits hold the number of the row within the page. Data output is synchronized to SC, the row driver signal, and this counter is incremented by 1 on the falling edge of SC.

- Y-decoder

  The Y-decoder changes the order of the input or output data according to the MS signal. This is to allow for the alternative pin assignment that is available for the LSI. When MS = H, the regular pin assignment is used in which pins SEG1 to SEG50 are adjacent to one another. When MS = L, the even and odd-numbered pins are divided into separate blocks.
  See the sections DISPLAY DATA RAM and PIN ASSIGNMENT.

- Display ON / OFF flip-flop

  This flip-flop is set to the display ON / OFF state by the instruction. In the OFF state, outputs from the display RAM are set to 0 (display is all OFF). In the ON state, the T7932 outputs the display data held in the display RAM. This command never changes the display data in the display RAM.

- Display page register

  This register stores 2 bits of data which point to the display start page. The "M" signal sets the contents of this register to the value in the upper 2 bits of the Z-address counter.

- Up / Down flip-flop

  This flip-flop determines the count mode of the Y-address counter. In Up mode, the Y-address counter is increased by 1. If the Y-address = 49, the address becomes 0 after the operation. In Down mode, the Y-address counter is decreased by 1.

- Busy flag

  During the execution of an instruction, the T7932 sets the Busy flag (except for when it executes the Status Read instruction). The MPU can poll the Busy flag when the MPU performs a Read Status operation. While the T7932's Busy flag is set, the T7932 cannot accept any instructions other than Status Read. Hence the MPU must perform a Read Status before sending the next instruction.

  * Busy state time (T) is always shown as follows :

  $1/F \leqq T \leqq 2/F$ [s]

  F : $\phi 1$, $\phi 2$ frequency
  (T7933 oscillation frequency × 1 / 2)

- Latch

  The T7932 latches the data from the display RAM at the rising edge of SC.

- LCD drive circuit

  The T7932 has 50 column drivers. The display data in the latch circuit and the FR signal select one of four levels of LCD drive voltage.

DISPLAY CONTROL INSTRUCTIONS

(1) Set X, Y-address

R / W	D / I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0 to 49 (binary) (Address)						Page 0
0	0	0	1							Page 1
0	0	1	0							Page 2
0	0	1	1							Page 3

Y-Address
0, 2,··· ,3, 1 (MS = L)
0, 1,···48, 49 (MS = H)

00	Page 0
01	Page 1
10	Page 2
11	Page 3

Display Data RAM

(2) Set Up / Down

R / W	D / I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	1	1	1	0	1	1	Up mode
0	0	0	0	1	1	1	0	1	0	Down mode

This instruction selects the Up / Down mode for the Y-Address counter.

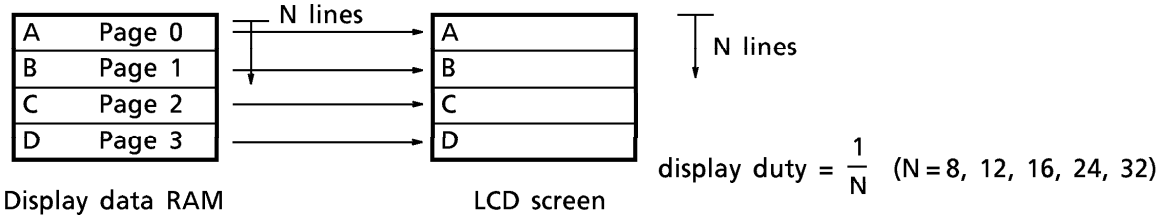
(3) Display Start Page

R / W	D / I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	1	1	1	1	1	0	Start page 0 : See Fig. 3-a
0	0	0	1	1	1	1	1	1	0	Start page 1 : See Fig. 3-b
0	0	1	0	1	1	1	1	1	0	Start page 2 : See Fig. 3-c
0	0	1	1	1	1	1	1	1	0	Start page 3 : See Fig. 3-d

This instruction specifies the RAM page whose data will be displayed at the top of the LCD screen. Data is displayed starting form the first line of the indicated page up to the end line at the duty factor specified by the T7933.

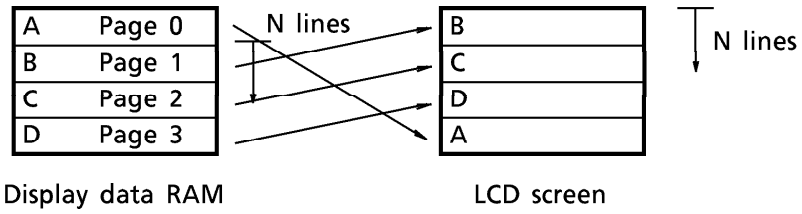
The relation between RAM page and display position is as follows:

(3-a) When start page = page 0

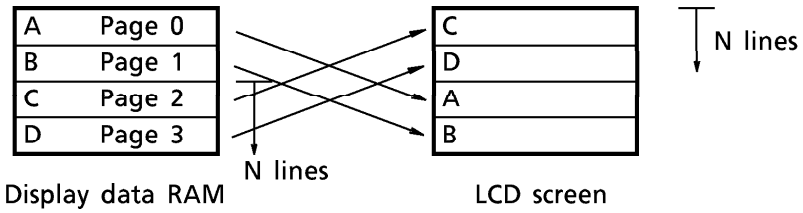


$$\text{display duty} = \frac{1}{N} \quad (N = 8, 12, 16, 24, 32)$$

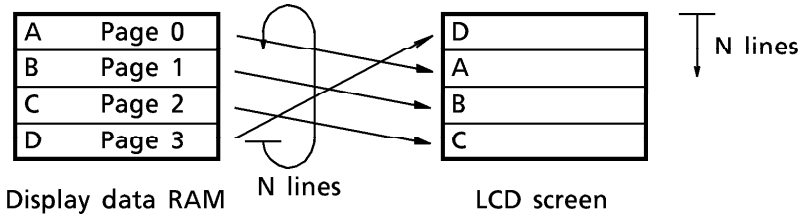
(3-b) When start page = page 1



(3-c) When start page = page 2



(3-d) When start page = page 3



(4) Display ON / OFF

R / W	D / I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	1	1	1	0	0	1	Display ON
0	0	0	0	1	1	1	0	0	0	Display OFF

This instruction controls the display ON / OFF setting. This instruction does not change the contents of the display RAM.

(5) Read / Write Display Data

R / W	D / I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	1	(Display Data)								Read : MPU←T7932
0	1									Write : MPU→T7932

This instruction sends data to or receives data from the display RAM address which is pointed to. However, the MPU cannot read the correct data on the first reading. (Refer to Output Register in the Section FUNCTION OF EACH BLOCK.)

(6) Status Read

R / W	D / I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	BUSY	UP / DOWN	OFF / ON	RST	0	0	0	0

1 : Reset 0 : operation

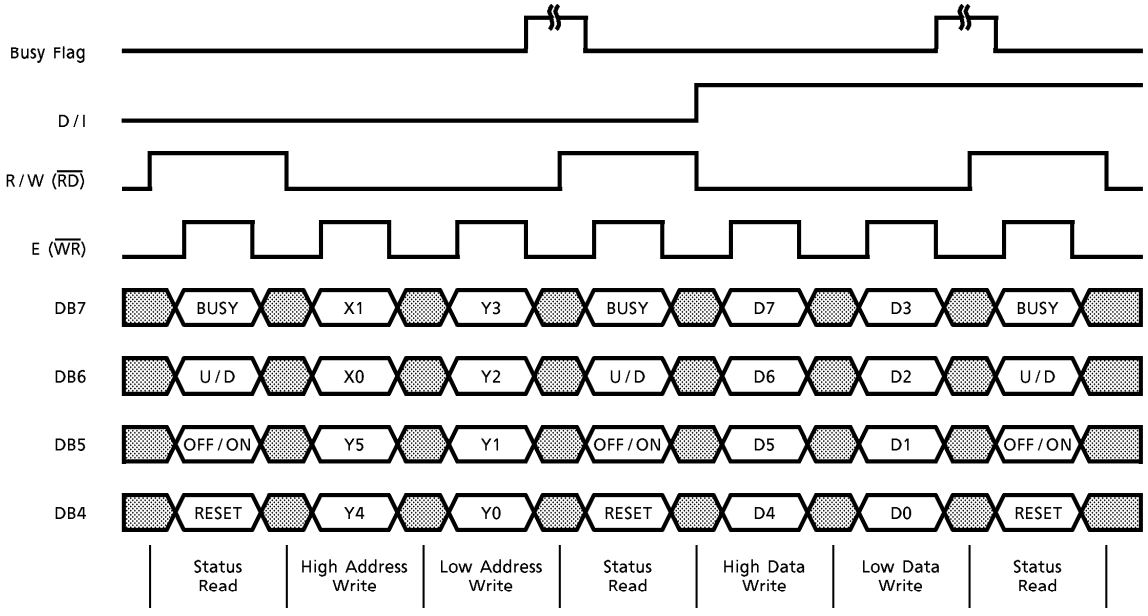
1 : Display OFF 0 : Display ON

1 : Y-Address counter Up mode
0 : Y-Address counter Down mode

1 : Busy state (except for Status Read)
T7932 cannot accept any other instruction

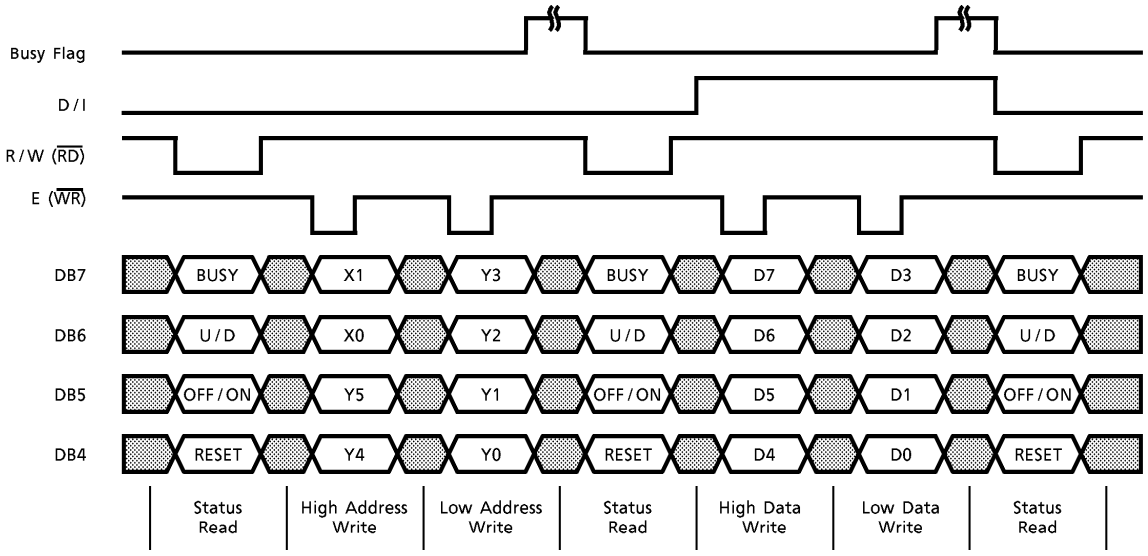
EXAMPLE OF TIMING

- 4-bit mode, 68-series MPU interface (80 / $\overline{68}$ = L)

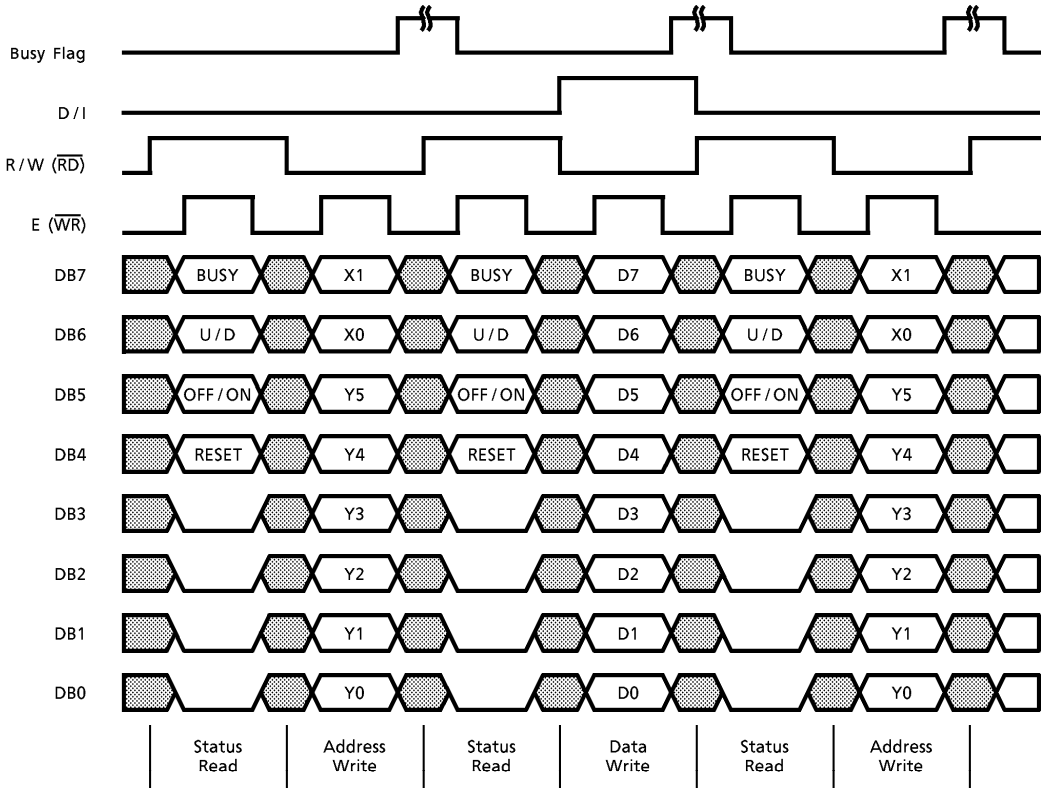


The Busy flag is set on the falling edge of the second E signal.
In this mode, it is not necessary to check the Busy flag between sending the upper data nybble and sending the lower data nybble.

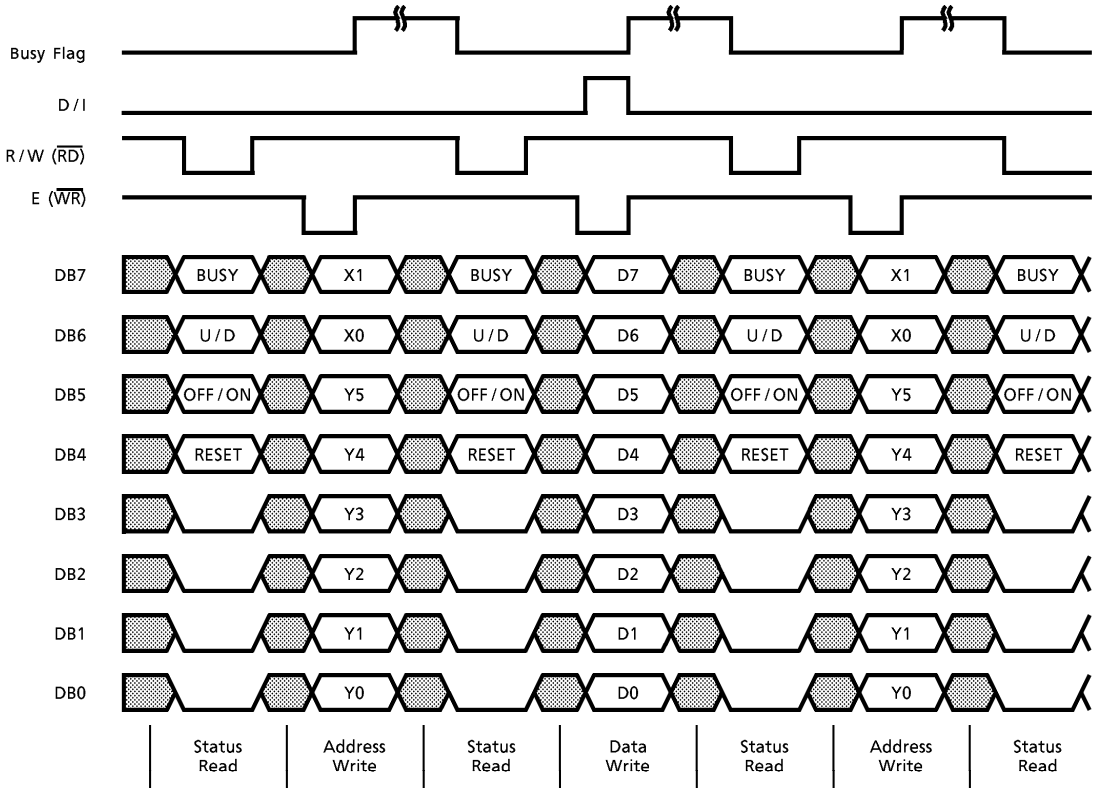
- 4-bit mode, 80-series MPU interface (80 / $\overline{68}$ = H)



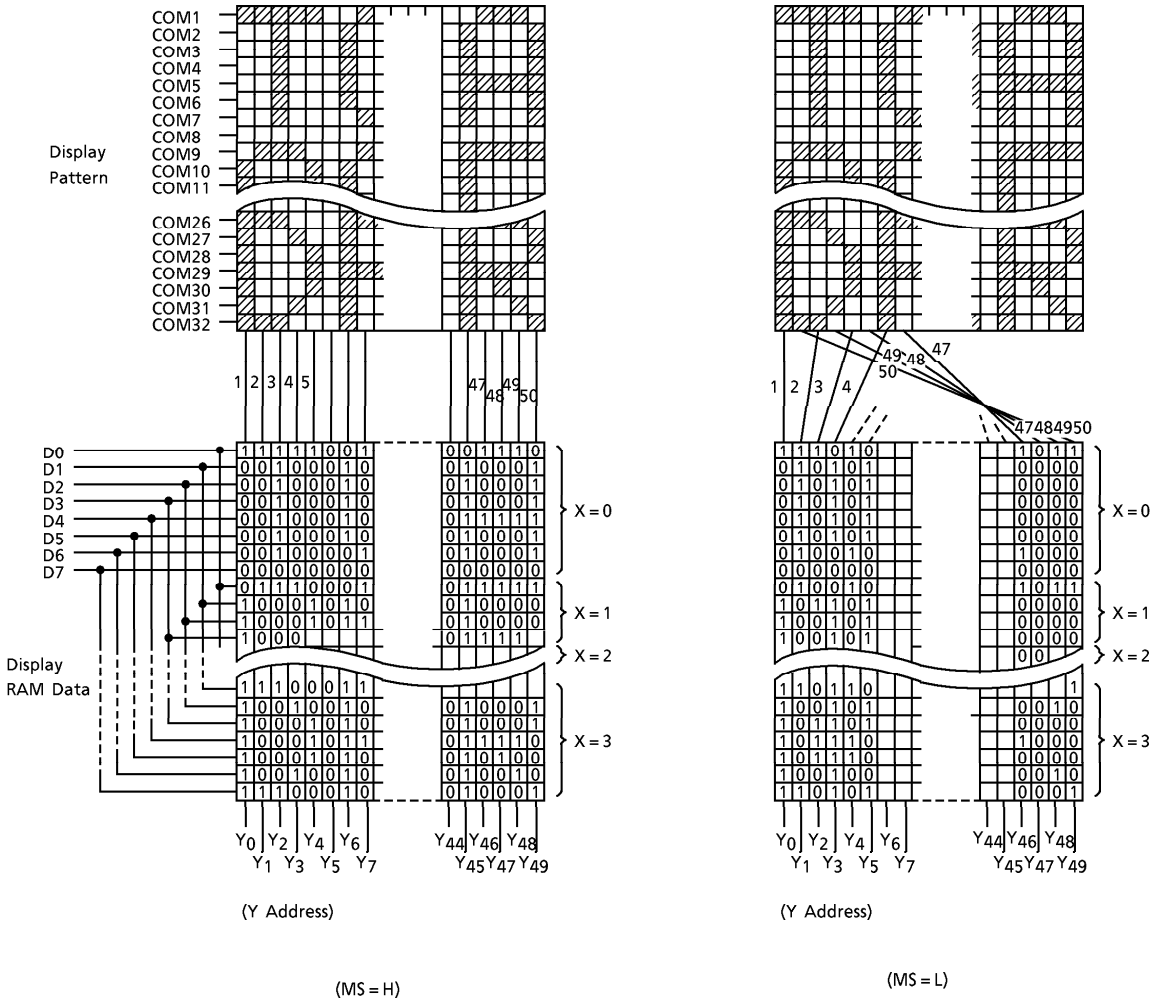
- 8-bit mode, 68-series MPU (80 / $\overline{68}$ = L)



- 8-bit mode, 80-series MPU (80 / $\overline{68}$ = H)



DISPLAY DATA RAM



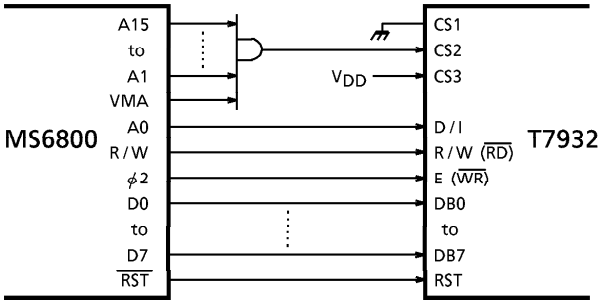
ALTERNATIVE PIN ASSIGNMENT MODE

This mode allows selection of the pin assignment.
In order to facilitate wiring, two alternative pin assignment layouts are available.
If MS = H, the standard assignment is selected. If MS = L, the odd and even output pins are divided into separate blocks.
See the PIN ASSIGNMENT sections.

INTERFACE TO MPU

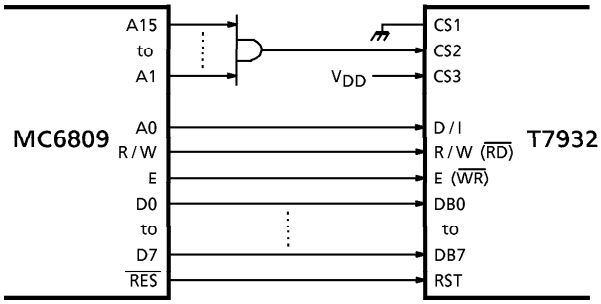
In each case, the address assigned to the T7932 is shown as follows.

- Example of connection to MC6800



☐ Read / Write the display data
$FFFF
☐ Write the display instruction
$FFFE
☐ Read the status
$FFFE

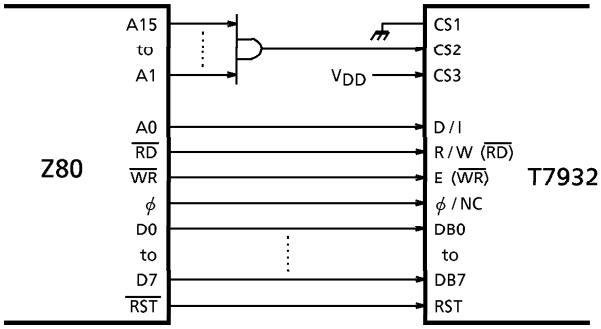
- Example of connection to MC6809



☐ Read / Write the display data
$FFFF
☐ Write the display instruction
$FFFE
☐ Read the status
$FFFE

MC6800 and MC6809 is a registered trademark of Motorola Semiconductor Products Inc.

- Example of connection to Z80



☐ Read / Write the display data
$FFFF
☐ Write the display instruction
$FFFE
☐ Read the status
$FFFE

Z80 is a registered trademark of Zilog Inc.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

ITEM	SYMBOL	RATING	UNIT
Supply Voltage (1)	V_{DD} (Note 1)	− 0.3 to 7.0	V
Supply Voltage (2)	V_{LC2}, V_{LC3}, V_{LC5} (Note 1, 2)	V_{DD} − 13.5 to V_{DD} + 0.3	V
Input Voltage	V_{IN} (Note 1)	− 0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opr}	− 20 to 75	°C
Storage Temperature	T_{stg}	− 55 to 125	°C

(Note 1) Referenced to V_{SS} = 0V
(Note 2) Ensure that the following condition is always maintained.
$V_{DD} \geqq V_{LC2} \geqq V_{LC3} \geqq V_{LC5}$

ELECTRICAL CHARACTERISTICS
DC CHARACTERISTICS
TEST CONDITIONS (Unless otherwise noted, V_{SS} = 0V, V_{DD} = 5.0V ± 10%, V_{LC5} = 0V, Ta = − 20 to 75°C)

ITEM		SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	PIN NAME
Operating Voltage (1)		—	—	—	4.5	5.0	5.5	V	V_{DD}
Operating Voltage (2)		—	—	—	V_{DD} − 11	—	V_{DD} − 3.0	V	V_{LC5}
Input Voltage	H Level	V_{IH}	—	—	V_{DD} − 1.0	—	V_{DD}	V	M, FR, SC, BS, 80/$\overline{68}$, MS, ϕ1, ϕ2
	L Level	V_{IL}	—	—	0	—	1.0	V	
Input Voltage	H Level	V_{IH}	—	—	2.2	—	V_{DD}	V	CS1 to CS3, E, R/W, D/I, DB0 to DB7, RST
	L Level	V_{IL}	—	—	0	—	0.8	V	
Output Voltage	H Level	V_{OH}	—	—	V_{DD} − 0.4	—	V_{DD}	V	DB0 to DB7
	L Level	V_{OL}	—	—	0	—	0.4	V	
Output Voltage	H Level	V_{OH}	—	—	V_{DD} − 0.3	—	V_{DD}	V	SEG1 to SEG50
	M Level	V_{OM}	—	$V_{LC2} = V_2$	V_2 − 0.3	—	V_2 + 0.3	V	
				$V_{LC3} = V_3$	V_3 − 0.3	—	V_3 + 0.3	V	
	L Level	V_{OL}	—	—	V_5	—	V_5 + 0.3	V	

ITEM		SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	PIN NAME
Output Resistance	H Level	ROH	—	$V_{OUT} = V_{DD} - 0.5V$	—	—	1.5	kΩ	DB0 to DB7
	L Level	ROL	—	$V_{OUT} = 0.5V$	—	—	0.2	kΩ	
Output Resistance	H Level	ROH	—	$V_{OUT} = V_{DD} - 0.5V$	—	—	5.0	kΩ	SEG1 to SEG50
	M Level	ROM	—	$V_{LC2} = V_2$, $V_{OUT} = V_2 \pm 0.5V$	—	—	5.0	kΩ	
			—	$V_{LC3} = V_3$, $V_{OUT} = V_3 \pm 0.5V$	—	—	5.0	kΩ	
	L Level	ROL	—	$V_{LC5} = V_5$, $V_{OUT} = V_5 + 0.5V$	—	—	5.0	kΩ	
Operating Frequency		f_{osc}	—	Ta = – 10 to 70°C	25	—	300	kHz	$\phi 1$, $\phi 2$
Current Consumption (Note 1)		I_{SS}	—	$V_{DD} = 5.0V$ $V_{LC5} = 0V$ $V_{LC3} = V_3$ $V_{LC2} = V_2$ $f_{FR} = 35Hz$ $f_{cp} = 215kHz$ SEG1 to SEG50 : no load (Note 3)	—	—	200	μA	V_{SS}
Current Consumption (Note 2)		I_{SS}	—	$V_{DD} = 5.0V$ $V_{LC5} = 0V$ $V_{LC3} = V_3$ $V_{LC2} = V_2$ $f_{FR} = 35Hz$ $f_{cp} = 215kHz$ SEG1 to SEG50 : no load (Note 3)	—	—	20	μA	V_{SS}

(Note 1) Current consumption while the internal data receiver is operating.
(Note 2) Current consumption while the internal data receiver is sleeping.

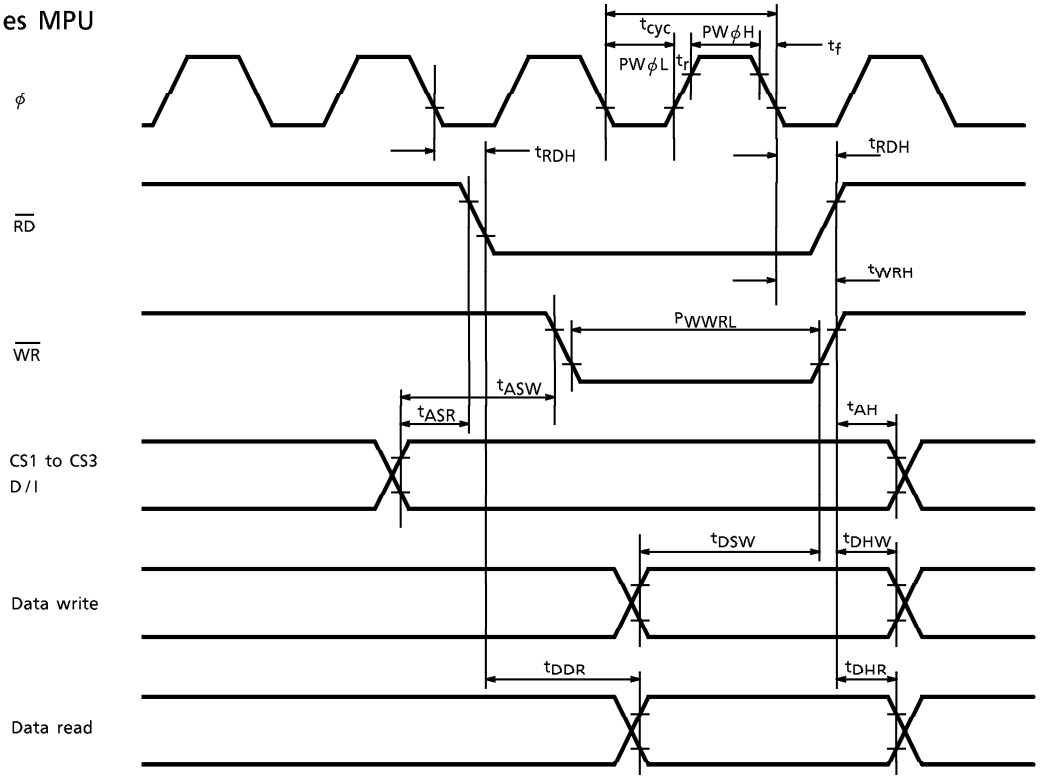
(Note 3) $V_3 = V_{DD} - \frac{3}{5}(V_{DD} - V_{LC5})$

$V_2 = V_{DD} - \frac{2}{5}(V_{DD} - V_{LC5})$

Data Level : H = 5.0V, L = 0V

AC CHARACTRISTICS

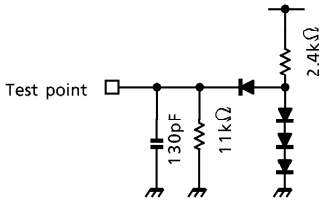
- 80-series MPU



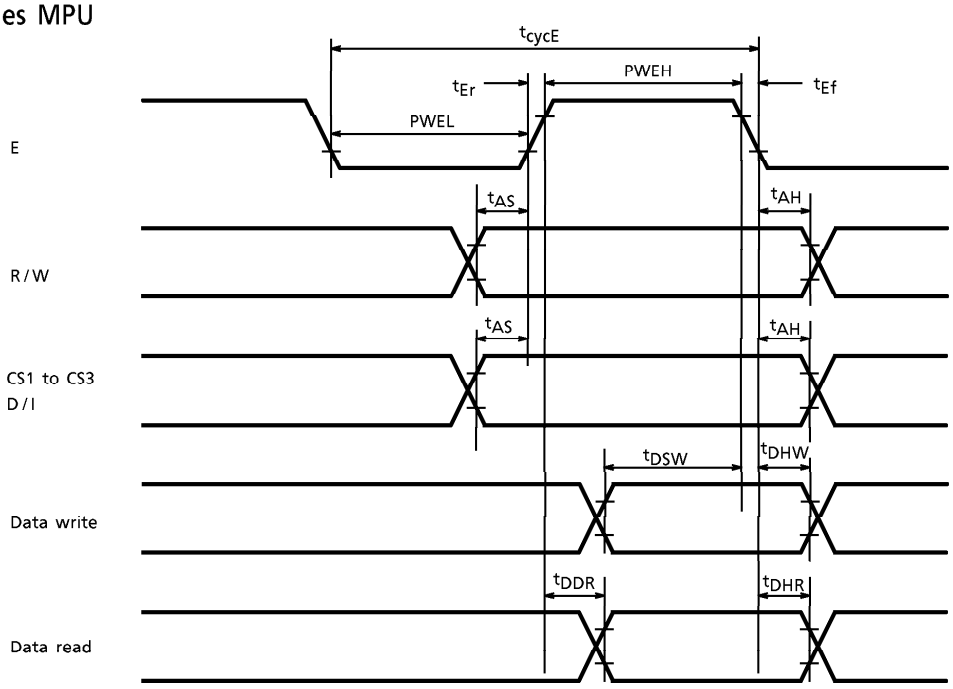
TEST CONITIONS (V_{SS} = 0V, V_{DD} = 5V ± 10%, Ta = – 20 to 75°C)

ITEM	SYMBOL	MIN	MAX	UNIT
ϕ Cycle Time	$t_{cycE\phi}$	250	—	ns
ϕ Pulse Width H, L	PWϕH, PWϕL	110	—	ns
ϕ Pulse Rise / Fall Time	t_r, t_f	—	30	ns
RD Hold Time	t_{RDH}	0	100	ns
WR Hold Time	t_{WRH}	0	100	ns
WR Pulse Width L	P_{WWRL}	300	—	ns
Write mode Address Set-up Time	t_{ASW}	0	—	ns
Read mode Address Set-up Time	t_{ASR}	0	—	ns
Address Hold Time	t_{AH}	10	—	ns
Data Set-up Time	t_{DSW}	100	—	ns
Data Delay Time	t_{DDR}	—	200	ns
Write Mode Data Hold Time	t_{DHW}	10	—	ns
Read Mode Data Hold Time	t_{DHR}	20	—	ns

Test Load



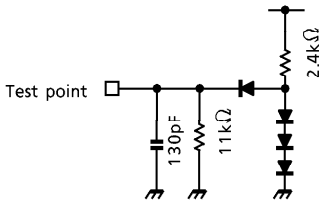
- 68-series MPU



TEST CONDITIONS (V_{SS} = 0V, V_{DD} = 5V ± 10%, Ta = − 20 to 75°C)

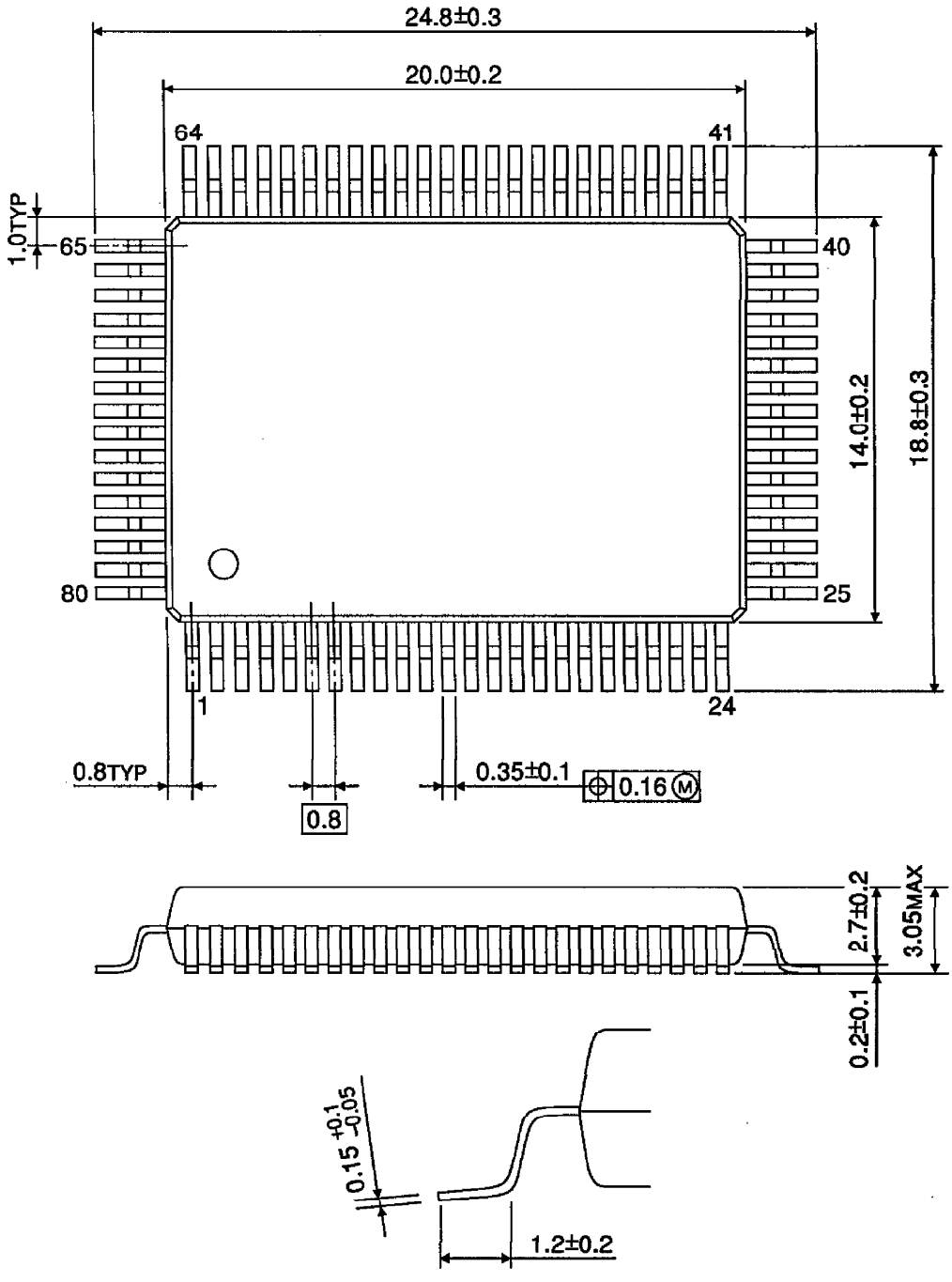
ITEM	SYMBOL	MIN	MAX	UNIT
E Cycle Time	t_{cycE}	500	—	ns
E Pulse Width H	PWEH	220	—	ns
E Pulse Width L	PWEL	220	—	ns
E Pulse Rise Time	t_r	—	20	ns
E Pulse Fall Time	t_f	—	20	ns
Address Set-up Time	t_{AS}	40	—	ns
Address Hold Time	t_{AH}	10	—	ns
Data Set-up Time	t_{DSW}	60	—	ns
Data Delay Time	t_{DDR}	—	140	ns
Write Mode Data Hold Time	t_{DHW}	10	—	ns
Read Mode Data Hold Time	t_{DHR}	20	—	ns

Test Load



OUTLINE DRAWING

QFP80-P-1420-0.80A Unit : mm



Weight : 1.5g (Typ.)