

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T 7 9 3 3**ROW DRIVER LSI FOR DOT MATRIX LCD**

The T7933 is a row (common) driver LSI for a small- or medium-scale dot matrix LCD. The T7933 realizes low power LCD systems using the CMOS Si-Gate process.

The T7933 generates timing signals for the display using a built-in oscillator and also controls the T7932 column (segment) LCD driver.

Five duty options are available : 1/8, 1/12, 1/16, 1/24 and 1/32. The T7933 has 32 low-impedance output row drivers ($1\text{k}\Omega$ max).

The T7933 includes internal resistors to the divide bias voltage for 1/16 duty and 1/32 duty displays.



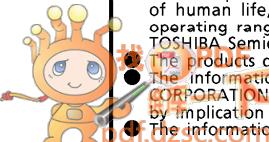
Weight: 1.1g (typ.)

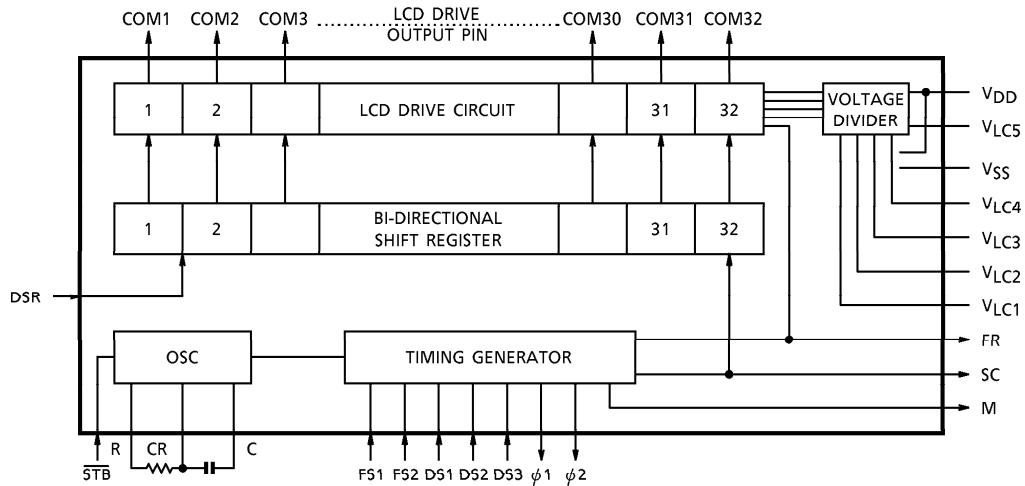
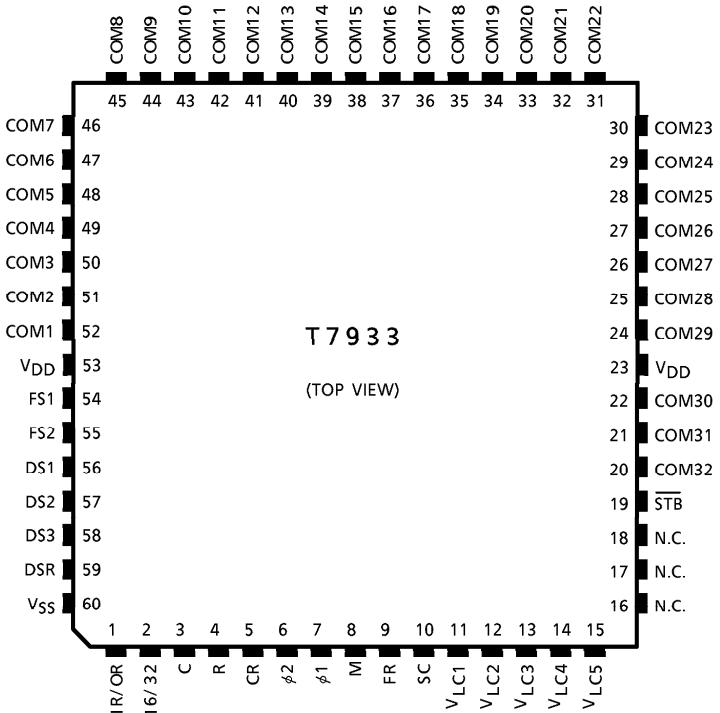
FEATURES

- Row signal output for LCD
- LCD drive outputs : 32 (low impedance)
- Built-in oscillator (additional external resistor and capacitor)
- Built-in voltage dividers for 1/16 and 1/32 duty cycle
- Duty : 1/8, 1/12, 1/16, 1/24, 1/32
- Low power consumption
- Logic power supply : $V_{DD} = 5V \pm 10\%$
- 60-pin flat plastic package

961001EBA2

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BLOCK DIAGRAM**PIN ASSIGNMENT**

PIN FUNCTIONS

PIN NAME	I/O	FUNCTIONS	SIGNAL VOLTAGE																														
COM1 to COM32	Output	LCD drive signal outputs	VDD to VLC5																														
CR, R, C	—	Pins for oscillator	—																														
FR	Output	Frame signal output	VDD to VSS																														
SC	Output	Shift clock pulse output	VDD to VSS																														
M	Output	Display synchronous signal	VDD to VSS																														
DS1 to DS3	Input	<p>Display select pin</p> <table border="1"> <tr> <td>DISPLAY DUTY</td><td>1/8</td><td>1/16</td><td>1/12</td><td>1/32</td><td>1/24</td></tr> <tr> <td>DS1</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td></tr> <tr> <td>DS2</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td></tr> <tr> <td>DS3</td><td>L</td><td>L</td><td>H</td><td>L</td><td>H</td></tr> </table>	DISPLAY DUTY	1/8	1/16	1/12	1/32	1/24	DS1	L	L	L	H	H	DS2	L	H	H	L	L	DS3	L	L	H	L	H	VDD to VSS						
DISPLAY DUTY	1/8	1/16	1/12	1/32	1/24																												
DS1	L	L	L	H	H																												
DS2	L	H	H	L	L																												
DS3	L	L	H	L	H																												
FS1, FS2	Input	<p>Selects frequency Select oscillation frequency The relation between f_{FR} and f_{osc} is as follows:</p> <table border="1"> <tr> <th>FS1</th><th>FS2</th><th>f_{osc} (kHz)</th><th>f_M (Hz)</th><th>f_{FR}</th><th>f_{CP} (kHz)</th></tr> <tr> <td>L</td><td>L</td><td>107.5</td><td>70</td><td>35</td><td>53.8</td></tr> <tr> <td>H</td><td>L</td><td>107.5</td><td>70</td><td>35</td><td>53.8</td></tr> <tr> <td>L</td><td>H</td><td>215.0</td><td>70</td><td>35</td><td>107.5</td></tr> <tr> <td>H</td><td>H</td><td>430.0</td><td>70</td><td>35</td><td>215.0</td></tr> </table> <p>f_{osc} : Oscillation frequency f_M : Synchronous signal frequency f_{FR} : Frame frequency f_{CP} : Frequencies of ϕ_1, ϕ_2</p>	FS1	FS2	f_{osc} (kHz)	f_M (Hz)	f_{FR}	f_{CP} (kHz)	L	L	107.5	70	35	53.8	H	L	107.5	70	35	53.8	L	H	215.0	70	35	107.5	H	H	430.0	70	35	215.0	VDD to VSS
FS1	FS2	f_{osc} (kHz)	f_M (Hz)	f_{FR}	f_{CP} (kHz)																												
L	L	107.5	70	35	53.8																												
H	L	107.5	70	35	53.8																												
L	H	215.0	70	35	107.5																												
H	H	430.0	70	35	215.0																												
STB	Input	Input pin for test: usually connected to VDD	—																														
DSR	Input	Shift Register Shift direction select pin	VDD to VSS																														
ϕ_1, ϕ_2	Output	Operating clock output pins for T7932 The frequency of $\phi_1, \phi_2 = f_{osc} \times \frac{1}{2}$	VDD to VSS																														
IR / OR	Input	IR / OR = H : LCD power supply divided by built-in voltage divider IR / OR = L : LCD power supply external input	VDD to VSS																														

PIN NAME	I/O	FUNCTIONS	SIGNAL VOLTAGE
16 / 32	Input	Select voltage divide factor. (LCD voltage supply using built-in divider) $16 / 32 = H : \frac{1}{16}$ duty, $16 / 32 = L : \frac{1}{32}$ duty	V _{DD} to V _{SS}
V _{LC1} to V _{LC5}	—	Power supply for LCD drive <ul style="list-style-type: none"> ● When IR / OR = H V_{LC1}, V_{LC4} : Output V_{LC2}, V_{LC3} : Output V_{LC5} : Input ● When IR / OR = L V_{LC1}, V_{LC4}, V_{LC5} : Input V_{LC2}, V_{LC3} : High Impedance 	—
V _{DD}	—	Power supply (5V)	
V _{SS}	—	Power supply (0V)	

FUNCTION OF EACH BLOCK

- On-chip oscillator

The T7933 includes a built-in oscillator. (An external resistor must be connected between R and CR, and an external capacitor must be connected between C and CR). The external resistor and capacitor cause the oscillation frequency to change.

- Timing generator

This circuit divides the oscillation frequency and generates display timing signals suitable for the duty factor. The DS1 to DS3 inputs set the duty factor.

- Bi-directional shift register

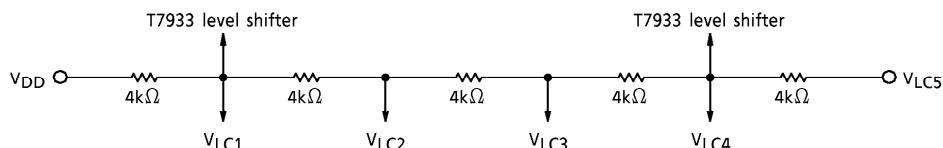
The T7933 has a 32-bit bi-directional shift register. The DSR input sets the shift direction. The data shift is synchronized to the SC signal.

- LCD driver

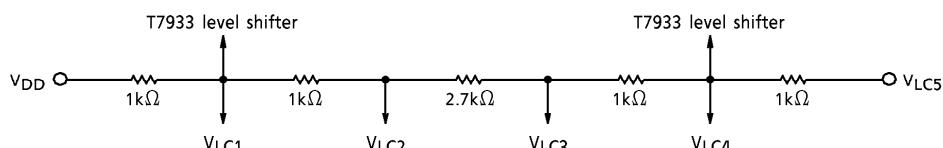
The T7933 has 32 row drivers and four LCD drive voltage output levels. The display data latched from the latch circuit and the FR signal select one of the four LCD drive voltage levels.

- On-chip voltage divider (IR / OR = H)

(1) $16 / 32 = H$



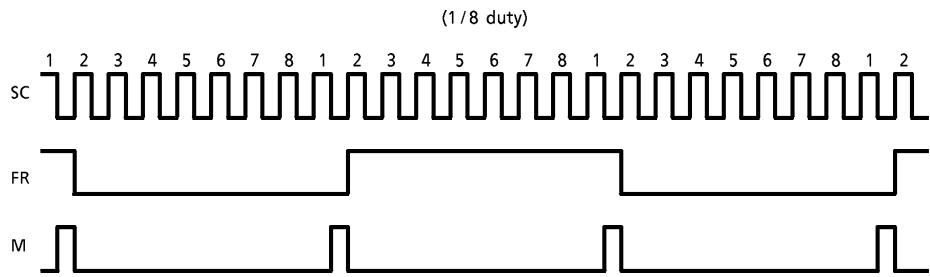
(2) $16 / 32 = L$



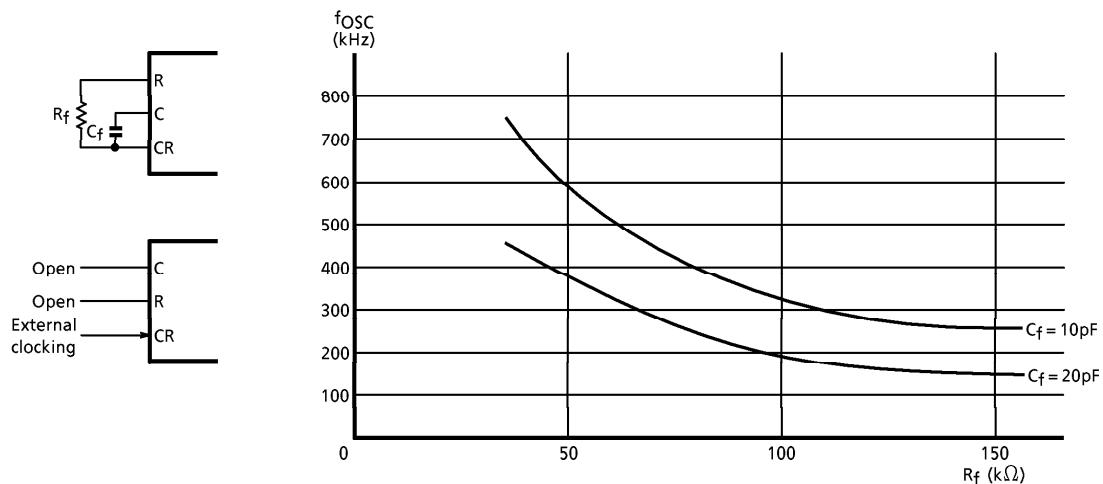
(Note 1) The T7933 can receive an external power supply via VLC1 and VLC4 when IR / OR = L.

(Note 2) The T7933 can supply power to an external driver via VLC2 and VLC3 when IR / OR = H.

RELATION BETWEEN SC, FR AND M OF RELATIONAL



RELATION BETWEEN OSCILLATION FREQUENCY, RF AND CF

 R_f , C_f connection

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

ITEM	SYMBOL	RATING	UNIT
Supply Voltage (1)	V_{DD} (Note 1)	-0.3 to 7.0	V
Supply Voltage (2)	$V_{LC1}, V_{LC4}, V_{LC5}$ (Note 1, 2)	$V_{DD} - 13.5$ to $V_{DD} + 0.3$	V
Input Voltage	V_{IN} (Note 1)	-0.3 to $V_{DD} + 0.3$	V
Operating Temperature	T_{opr}	-20 to 75	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to 125	$^\circ\text{C}$

(Note 1) Referenced to $V_{SS} = 0\text{V}$

(Note 2) Ensure that the following condition is always maintained.

$$V_{DD} \geq V_{LC1} \geq V_{LC4} \geq V_{LC5}$$

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

TEST CONDITIONS (Unless otherwise noted, $V_{SS} = 0\text{V}$, $V_{DD} = 5.0\text{V} \pm 10\%$, $V_{LC5} = 0\text{V}$, $T_a = -20$ to 75°C)

ITEM	SYM-BOL	TEST CIR-CUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	PIN NAME
Operating Voltage (1)	—	—	—	4.5	5.0	5.5	V	V_{DD}
Operating Voltage (2)	—	—	—	$V_{DD} - 11$	—	$V_{DD} - 3.0$	V	V_{LC5}
Input Voltage	H Level	V_{IH}	—	$V_{DD} - 1.0$	—	V_{DD}	V	CR, FS1, FS2, DS1 to DS3, M, \overline{STB} , IR/OR, DSR, 16/32, SC
	L Level	V_{IL}	—	0	—	1.0	V	
Output Voltage	H Level	V_{OH}	—	$V_{DD} - 0.3$	—	V_{DD}	V	M, FR, SC, $\phi 1, \phi 2$
	L Level	V_{OL}	—	0	—	0.3	V	M, FR, SC, $\phi 1, \phi 2$
Output Voltage	H Level	V_{OH}	—	$V_{DD} - 0.3$	—	V_{DD}	V	COM1 to COM32
	M Level	V_{OM}	$V_{LC1} = V_1$ $V_{LC4} = V_4$ $V_{LC2} = V_2$ $V_{LC3} = V_3$	$V_1 - 0.3$	—	$V_1 + 0.3$	V	COM1 to COM32
				$V_4 - 0.3$	—	$V_4 + 0.3$	V	COM1 to COM32
				$V_2 - 0.3$	—	$V_2 + 0.3$	V	V_{LC2}
				$V_3 - 0.3$	—	$V_3 + 0.3$	V	V_{LC3}
	L Level	V_{OL}	—	V_5	—	$V_5 + 0.3$	V	COM1 to COM32

ITEM		SYM-BOL	TEST CIR-CUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	PIN NAME
Output Resistance	H Level	R _{OH}	—	V _{OUT} = V _{DD} - 0.5V	—	—	1.0	kΩ	M, FR, SC, φ1, φ2
	L Level	R _{OL}	—	V _{OUT} = 0.5V	—	—	1.0	kΩ	M, FR, SC, φ1, φ2
Output Resistance	H Level	R _{OH}	—	V _{OUT} = V _{DD} - 0.5V	—	—	1.0	kΩ	COM1 to COM32
	M Level	R _{OM}	—	V _{LC1} = V ₁ , V _{OUT} = V ₁ ± 0.5V	—	—	1.0	kΩ	COM1 to COM32
				V _{LC4} = V ₄ , V _{OUT} = V ₄ ± 0.5V	—	—	1.0	kΩ	COM1 to COM32
	L Level	R _{OL}	—	V _{OUT} = V ₅ + 0.5V V _{LC5} = V ₅	—	—	1.0	kΩ	COM1 to COM32
Operating Frequency	f _{osc}	—	Ta = -10 to 70°C	70	—	500	kHz		CR
Current Consumption	I _{SS}	—	V _{DD} = 5.0V V _{LC5} = 0V V _{LC1} = V ₁ V _{LC4} = V ₄ f _{osc} = 430kHz (Duty: 1/16) COM1 to COM32: No Load	—	—	400	μA		V _{SS}

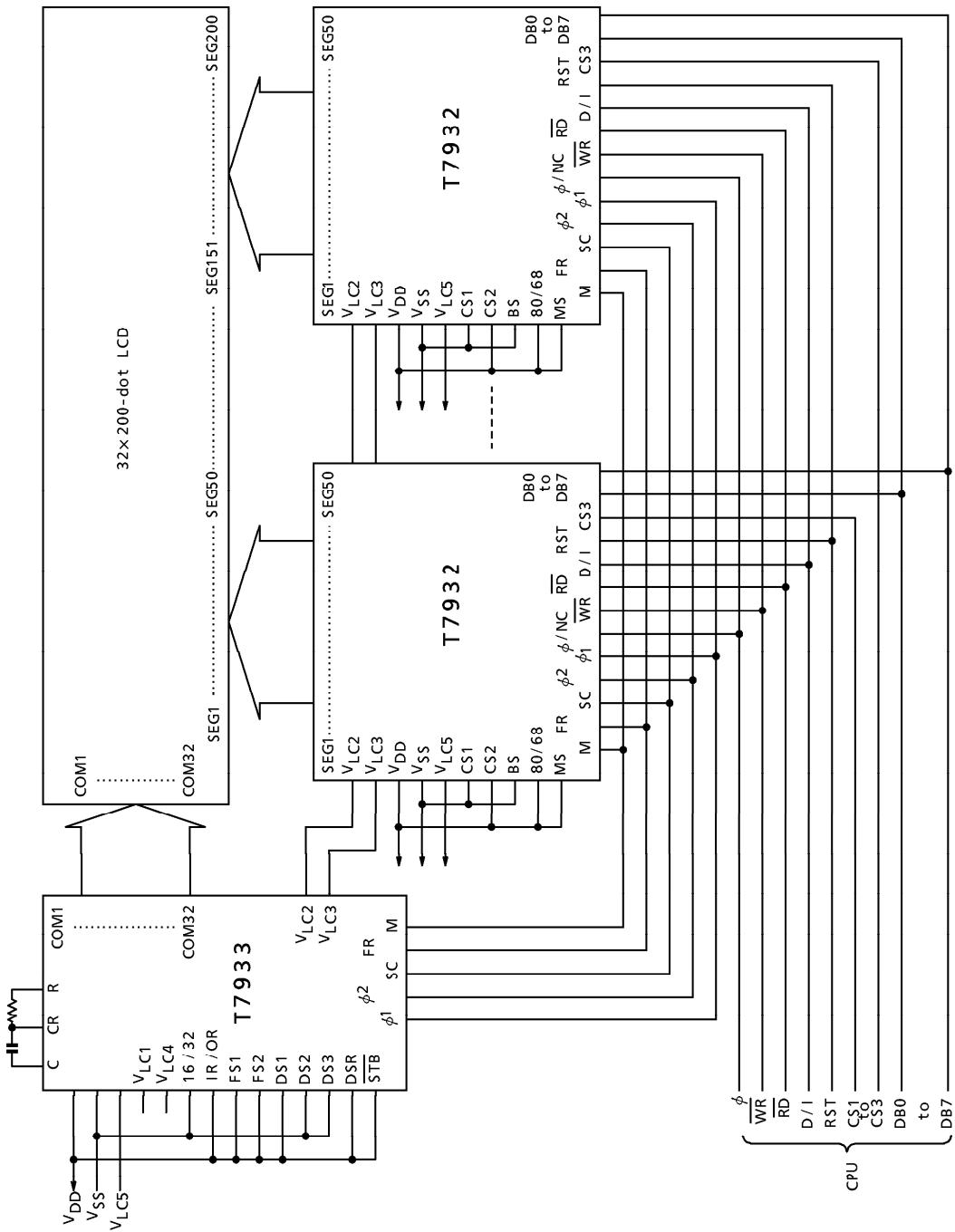
$$(Note\ 1)\ V_1 = V_{DD} - \frac{1}{5}(V_{DD} - V_{LC5}),\ V_2 = V_{DD} - \frac{2}{5}(V_{DD} - V_{LC5})$$

$$V_4 = V_{DD} - \frac{4}{5}(V_{DD} - V_{LC5}),\ V_3 = V_{DD} - \frac{3}{5}(V_{DD} - V_{LC5})$$

$$V_5 = V_{LC5}$$

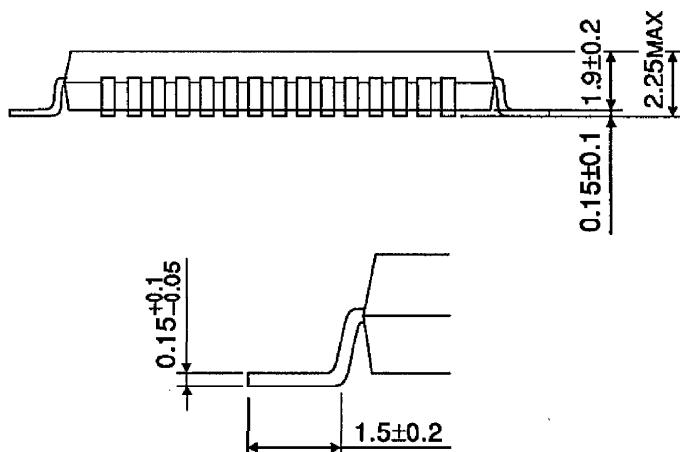
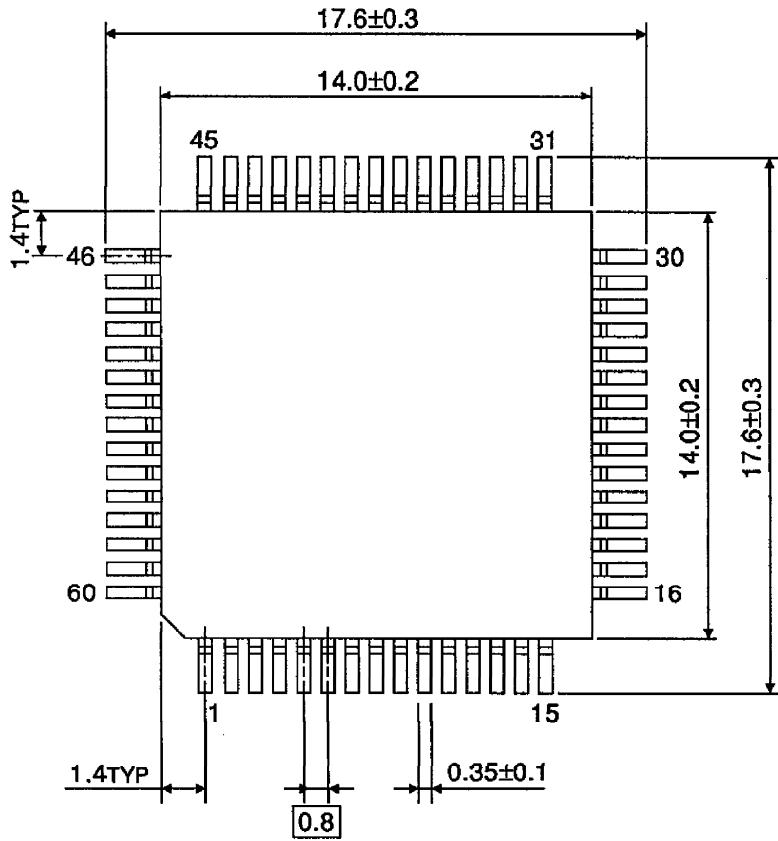
(Note 2) Output resistance measured when the on-chip voltage dividers are not used.

APPLICATION CIRCUIT



OUTLINE DRAWING
QFP60-P-1414-0.80A

Unit : mm



Weight : 1.1g (Typ.)