ST952

D.A.A. LINE INTERFACE

PRELIMINARY DATA

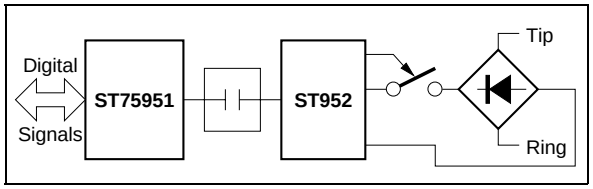
- HOOK SWITCH DRIVER
- RING INDICATOR
- LINE INTERFACE
  - DC TERMINATION (4V AT 20mA)
  - 2W/4W HYBRID CONVERTER
  - FLAT FREQUENCY RESPONSE DOWN TO 10Hz FOR 56Kps MODEM
- INTERFACE WITH CAPACITIVE ISOLATION BARRIER
- CALLER ID INTERFACE
- DIGITAL PHONE LINE OR OVER LOOP CURRENT LIMIT DETECT
- PHONE LINE IN USE CHECK

APPLICATIONS

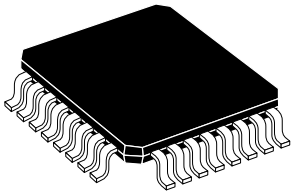
- MODEMS UP TO V.34, 33.6KBPS AND 56Kbps
- PCMCIA CARDS
- FAX MACHINES
- PERSONAL DIGITAL ASSISTANTS
- ANSWERING MACHINES
- HIGH FEATURE PHONES
- WEBPHONES AND SET TOP BOXES

DESCRIPTION

ST952 is a line interface designed to implement Modem application up to 56Kbps and Voice applications.
ST952 interfaces between telephone line and capacitive isolation barrier.
A complete D.A.A. is made with ST75951 which interfaces between capacitive isolation barrier and the DSP or HSP signals.



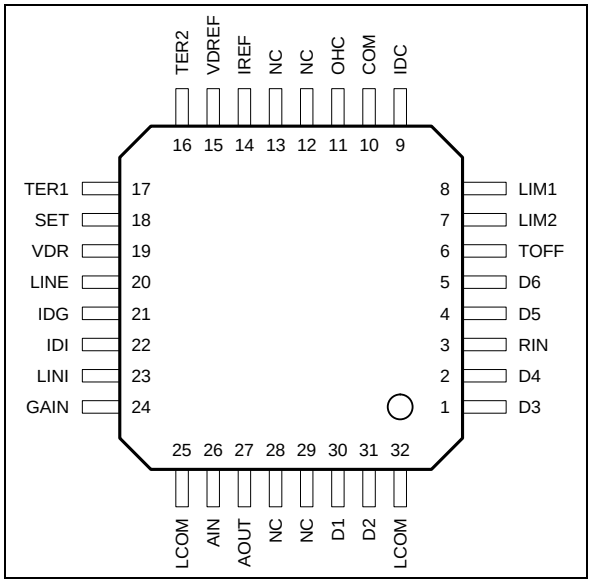
It incorporates Krypton Isolation Inc. patented silicon DAA technology.
The ring burst signal is detected by ST952 and is sent to ST75951 through the capacitive isolation barrier.
Using the control signals given by ST75951, through the capacitive isolation barrier, ST952 activates the off-hook or the CLID external transistor switch.



TQFP32 (7 x 7 x 1.4mm)
(Thin Plastic Quad Flat Pack)
ORDER CODE : ST952TQF7

If CLID external transistor switch is enabled, a limited amount of current, less than 1mA, is drawn from the line.
In off-hook state, ST952 DC voltage, 4V at a 20mA line current, allows to interface with most of public networks in the world.
The return loss is externally adjustable to real or complex impedance.
In case of a wrong connection in a digital phone line, ST952 detects the over current value and sends to ST75951 an alert signal through the capacitive isolation barrier.
Before starting a line connection, ST952 is abled to check if the line is used by an other terminal connected on the same telephone line.

PIN CONNECTIONS



PIN LIST

Pin Number	Name	Type	Description
1	D3	Output	Isolation Signal Output
2	D4	Output	Isolation Signal Output
3	RIN	Input	Ring Signal Input
4	D5	Input	Isolation Control Signal Input
5	D6	Input	Isolation Control Signal Input
6	TOFF	Supply	Internal Reference Supply
7	LIM2	Input	Loop Current Limiter Control
8	LIM1	Output	Loop Current Limiter Control
9	IDC	Output	Caller ID Control Output
10	COM	Output	Off-hook & ID Commun Output
11	OHC	Output	Off-hook Control Output
12	N.C.	-	Not Connected
13	N.C.	-	Not Connected
14	IREF	Input	Current Reference Setting
15	VDREF	Supply	Internal Reference Pin
16	TER2	Output	Current Regulator Control Feedback
17	TER1	Output	Current Regulator Control Output
18	SET	Input	Current Regulator Filter
19	VDR	Supply	Line DC Voltage Regulator
20	LINE	Output	Line AC Signal Output
21	IDG	Input	Caller ID Voltage Reference Input
22	IDI	Input	Caller ID Signal Input
23	LINI	Input	Line AC Signal Input
24	GAIN	Input	Transmit Gain / Trans-Hybrid Loss Set
25	LCOM	Ground	Line Side Common Ground
26	AIN	Input	Analog Transmit Signal Input
27	AOUT	Output	Analog Transmit Signal Output
28	N.C.	-	Not Connected
29	N.C.	-	Not Connected
30	D1	Input	Isolation Signal Input
31	D2	Input	Isolation Signal Input
32	LCOM	Ground	Line Side Common Ground

952-01.TBL

Note : Pins 12, 13, 28 and 29 must be left opened.

PIN DESCRIPTION

D1 - D2

These pins input the AC signal modulated at Fmod coming from ST75951 through the capacitive isolation barrier.

D3 - D4

These pins output the AC signal modulated at Fmod in off-hook mode and at Fmod/2 in CLID mode to ST75951 through the capacitive isolation barrier.

In ring mode, these pins output the ring information, a differential $6V_{PP}$/1MHz signal.

D5 - D6

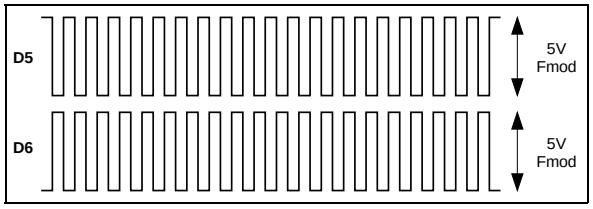
These control pins input a $5V_{PP}$/Fmod signal coming from ST75951 through the capacitive isolation barrier.

These signals control the off-hook and CLID external transistor switches and are sent to the internal transmit demodulator and receive modulator.

Off-hook mode is enabled with a $5V_{PP}$/Fmod signal sent on D5 and D6 inputs with an opposite phase (see Figure 1). With a dedicated application it is possible to reduce the input level to $3V_{PP}$.

CLID mode is enabled with a $5V_{PP}$/Fmod signal sent on D5 input only (see Figure 2). With a dedicated application it is possible to reduce the input level to $3V_{PP}$.

Figure 1



LINE

DC positive line connection and line AC signal output.

LCOM

Negative line connection.

LINI

Line AC signal input in off-hook mode.

AIN - AOUT

The transmit signal coming from AIN pin is injected in AOUT pin to the 2W/4W internal converter stage. The line echo is minimized if R3, connected between LINE and VDR pins is equal to 620Ω.

GAIN

R1 connected on this pin fixes the transmit gain. The R1 recommanded value, on a 600Ω AC line termination, is 82Ω.

RIN

During the ring burst, a 1MHz oscillator is powered on this pin and a $6V_{PP}$/1MHz signal is sent on D3 and D4 to indicate the ring presence.

IREF

Internal reference current source setting, R4 must be equal to 82kΩ.

VDR

Power supply for the transmit and receive paths in Off-Hook mode.

VDREF

Internal resistor reference.

SET

Line gyrator AC/DC filter.

OHC

When D5 and D6 inputs a $5V_{PP}$/Fmod signal in opposite phase, this pin puts ON the hook switch external Q1/Q2 transistor stage.

IDC

When D5 input a $5V_{PP}$/Fmod signal, this pin puts ON the CLID external Q3/Q4 transistor stage. R2 limits the line current in CLID mode at 1mA max.

COM

Commun output for off-hook and CLID external transistor stages

TER1 - TER2

These pins control the external Q5 transistor, in which the main part of the line current goes through to meet the line DC, $V = f(I_L)$, termination requirements.

IDI

Line AC signal input in CLID mode.

IDG

Power supply for the receive path in CLID mode.

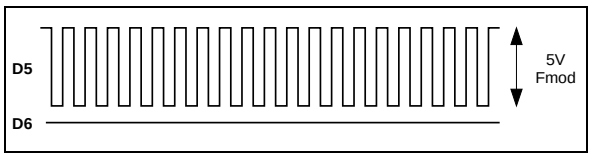
LIM1 - LIM2

200mA over current detection for device protection.

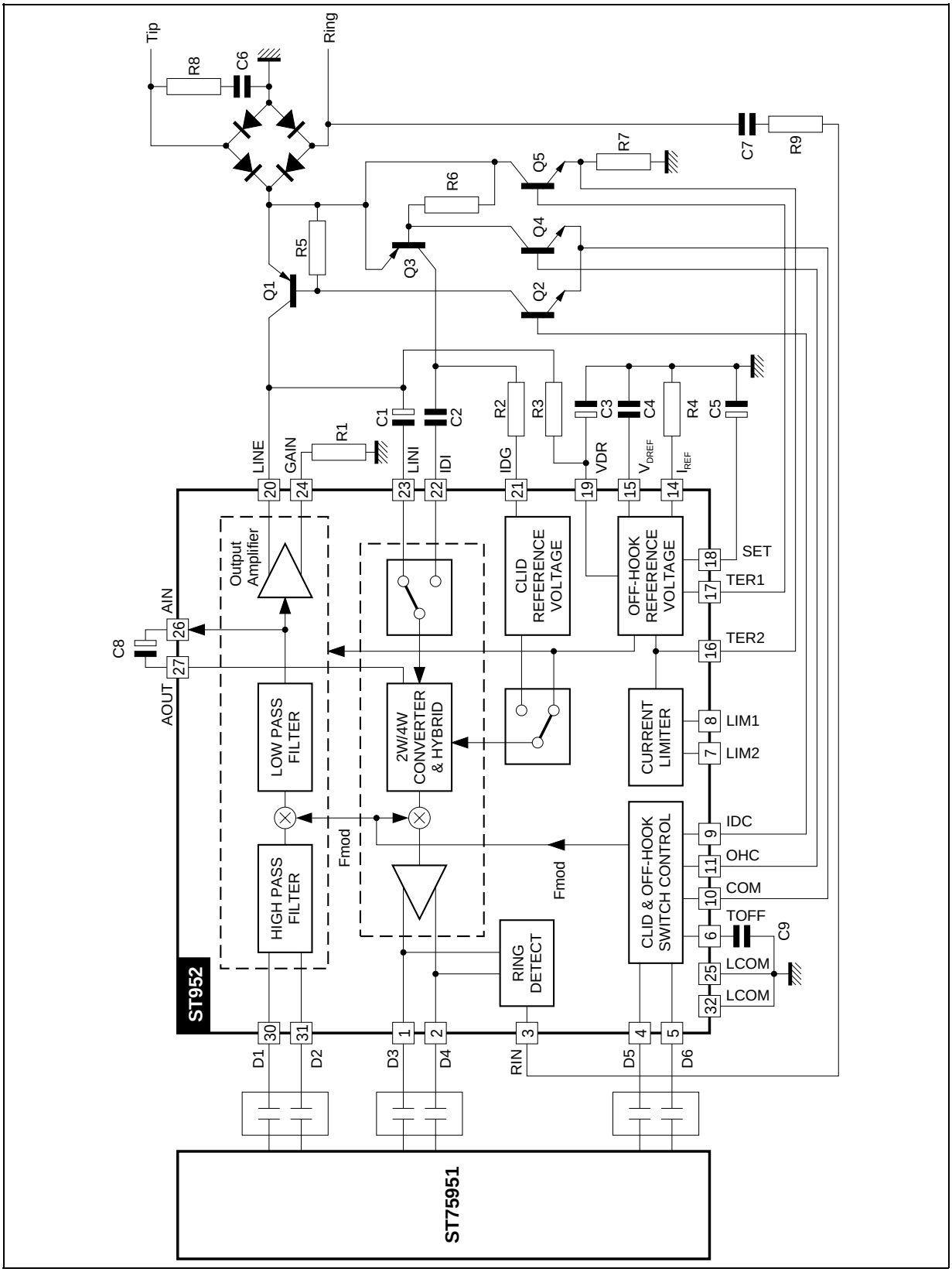
TOFF

Internal Reference Supply.

Figure 2



BLOCK DIAGRAM



952-05.EPS

ABSOLUTE MAXIMUM RATING (AGND = DGND = 0V, all voltages with respect to 0V)

Symbol	Parameter	Value	Unit
V_{MLINE}	Positive Line Voltage Continuous	14	V
T_{oper}	Operating Temperature	0, +70	°C
Tstg	Storage Temperature	-55, +150	°C

952-02.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Max.	80	°C/W

952-03T.BL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DC AND AC TERMINATION (see Figure 3)						
V_{LINE}	Line Voltage	I_L = 20mA I_L = 120mA		4.1 10.5		V V
ZLOSS	Return Loss	I_L = 20mA, V_{LAC} = -6dBV f = 200 to 4000Hz	 24			dB dB
RECEIVE PATH (I_L = 20mA, f = 1kHz, see Figure 4)						
Grx	Receive Gain	V_{LAC} = 0dBV, V_{TAC} = 0	-0.5	0	0.5	dB
Grf	Receive Frequency Response	V_{LAC} = 0dBV, V_{TAC} = 0 f = 200 to 3400Hz f = 50 to 200Hz	 -0.1 -0.5		 +0.1 +0.5	 dB dB
Rxhd	Receive 2nd/3th/4th Harmonic Distortion	V_{LAC} = 0dBV, V_{TAC} = 0 f = 150Hz f = 1000Hz		 -79 -82		 dBV dBV
Thl	Trans-Hybrid Loss	V_{LAC} = 0, V_{TAC} = -6dBV, Fmod = 1.5MHz	30	35		dB
Rn	Receive Noise Floor	V_{LAC} = V_{TAC} = 0, f = 200-3400Hz, 100Hz BW		-93		dBV
TRANSMIT PATH (I_L = 20mA, f = 1kHz, V_{LAC} = 0, see Figure 4)						
Gtx	Transmit Gain	V_{TAC} = -6dBV	-0.5	0	0.5	dB
Gtf	Transmit Frequency Response	V_{TAC} = -6dBV, f = 200 to 4000Hz	-0.2		+0.2	dB
Txhd	Transmit 2nd/3th/4th Harmonic Distortion	V_{TAC} = -6dBV, Fmod = 1.5MHz		-82		dBV
Txmax	Max Line Drive Voltage			3		V_{PP}
Tn	Transmit Noise Floor	V_{TAC} = 0, f = 200-3400Hz, 100Hz BW		-93		dBv
POWER AND DC LOGIC INPUT (see Figure 5)						
I_{LINE}	Line Current	ST952 Line Pin + Ic(Q5)	10		120	mA
V_{OFH}	Hook Switch Input	D5 and D6 Input Active (Off-hook) Inactive (On-hook)	 2.7		 5.25 0.8	 V V
V_{CLID}	CLID Input	D5 Input Active (CLID On) Inactive (On-hook)	 2.7		 5.25 0.8	 V V
CALLER ID RECEIVE PATH (see Figure 6)						
G_{RID}	CLID Receive Gain	V_{TAC} = -15dBV	-1	0	+1	dB
I_{LID}	CLID Line Current				1	mA
RING INDICATOR (see Figure 7)						
V_{RIOF} V_{RION}	D3 & D4 Ring indicator	D3 = D4 = 0 D3 = D4 = 3VPP	 18		8	V V

952-04.TBL

Note : D3 and D4 are complementary outputs.

Figure 3 : Test 1

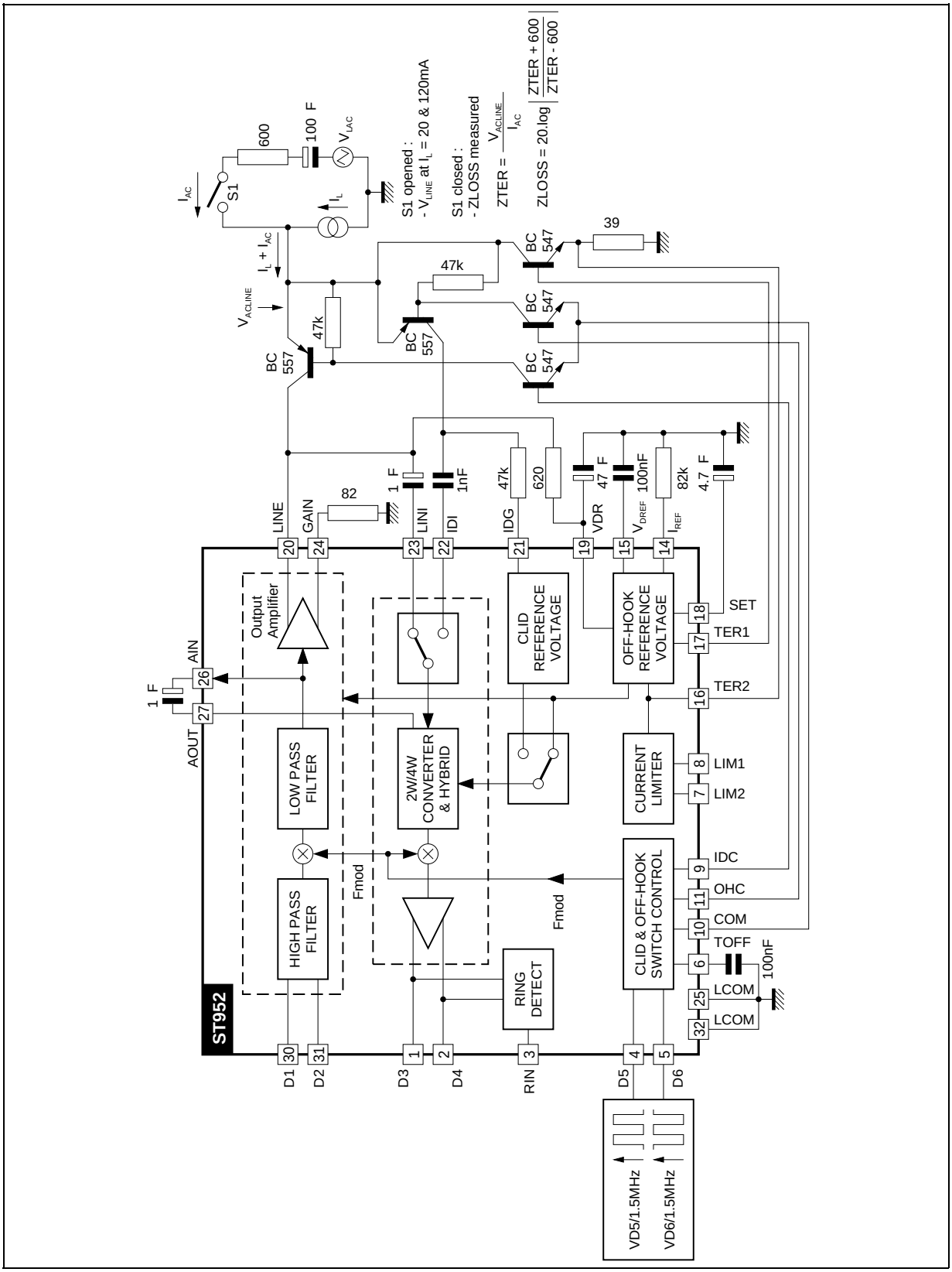


Figure 4 : Test 2

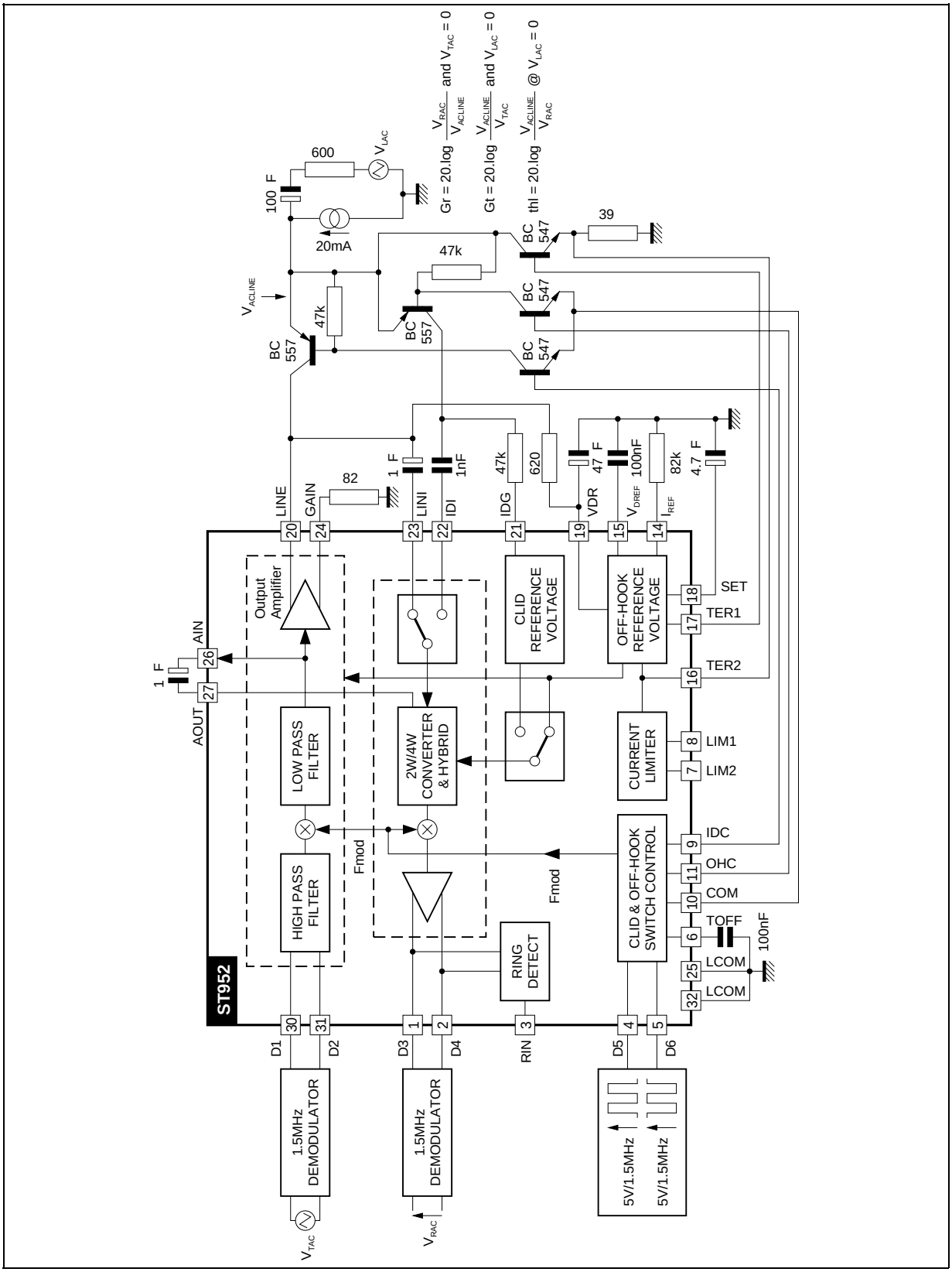


Figure 5 : Test 3

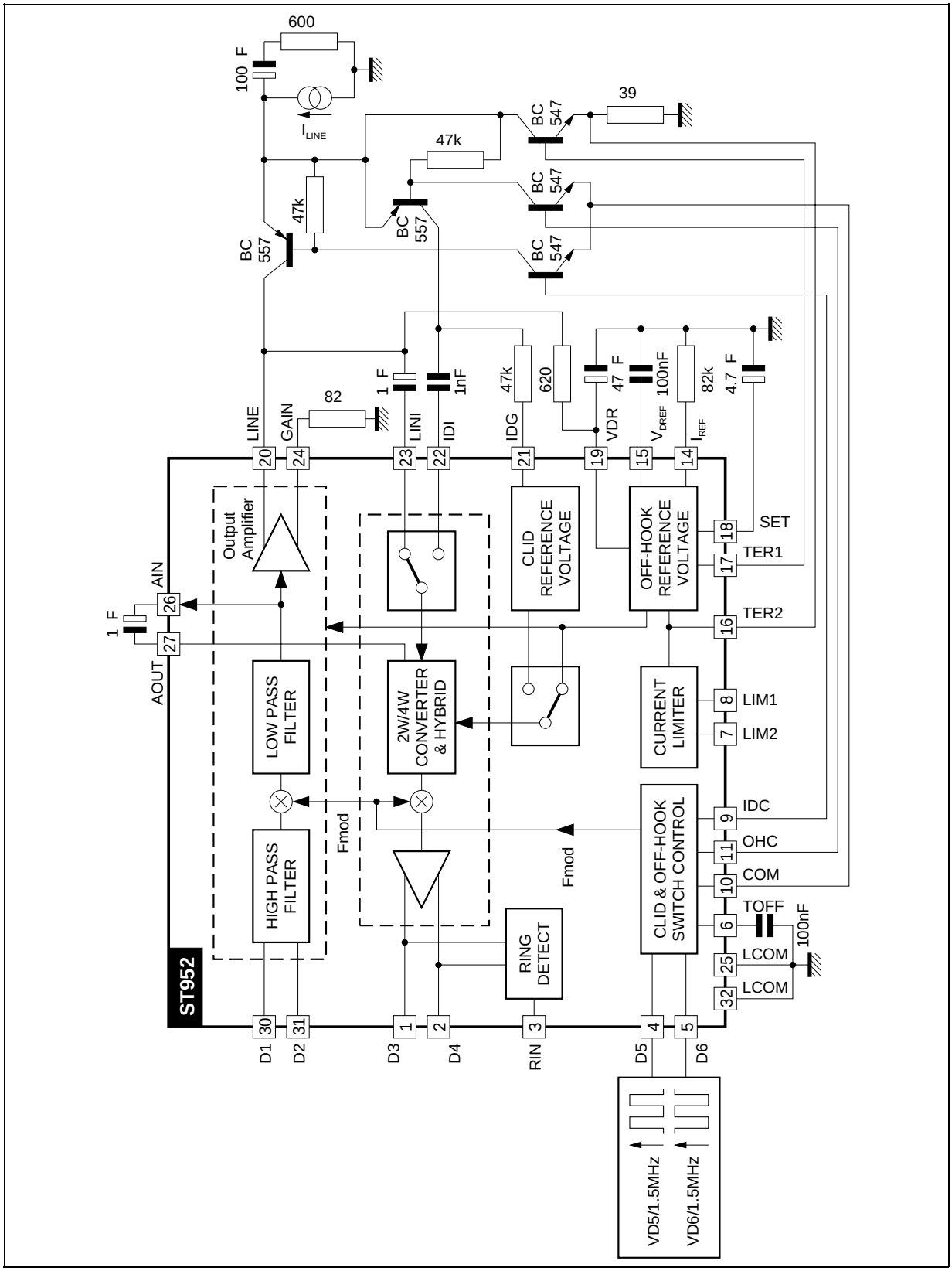


Figure 6 : Test 4

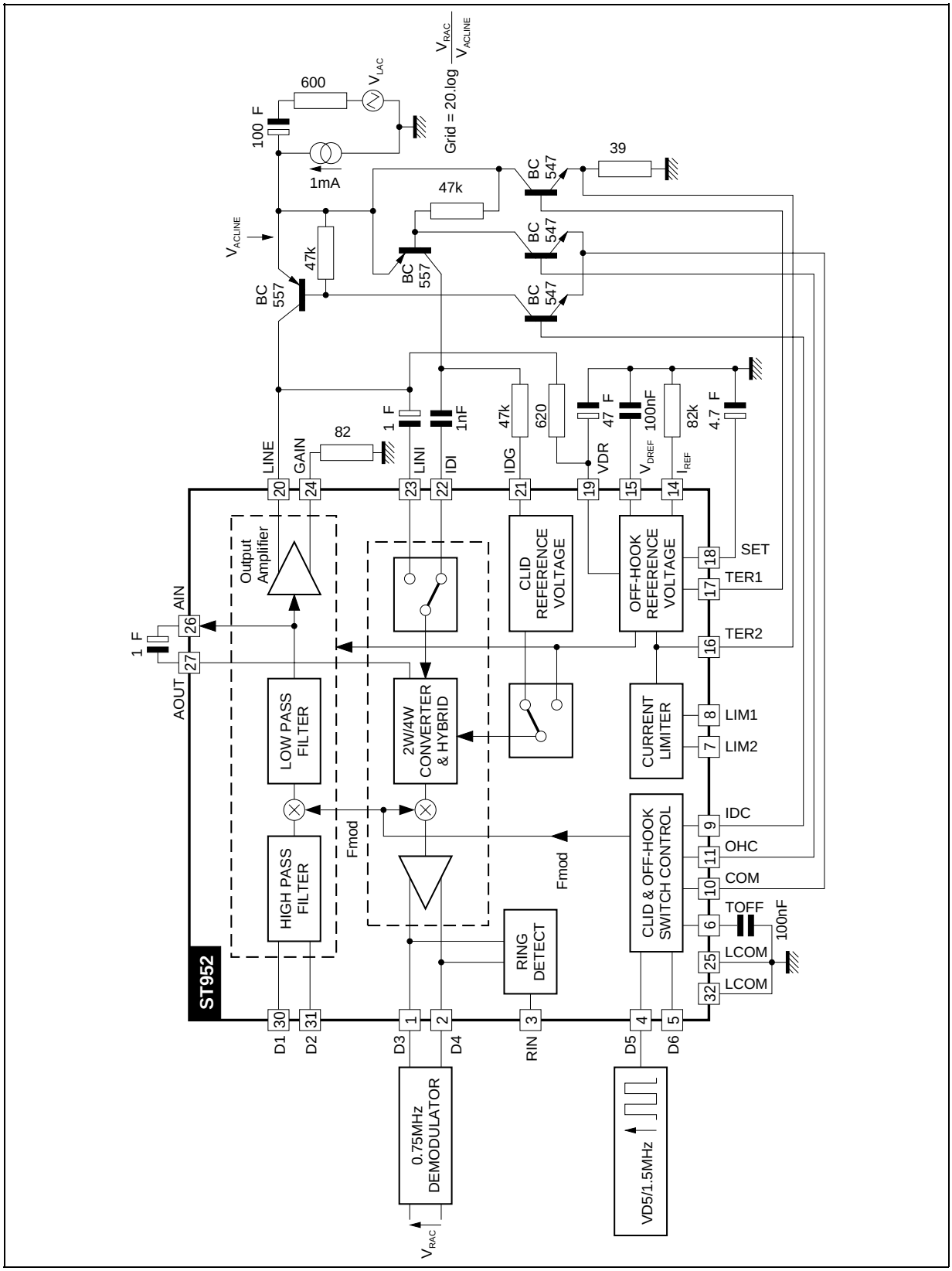
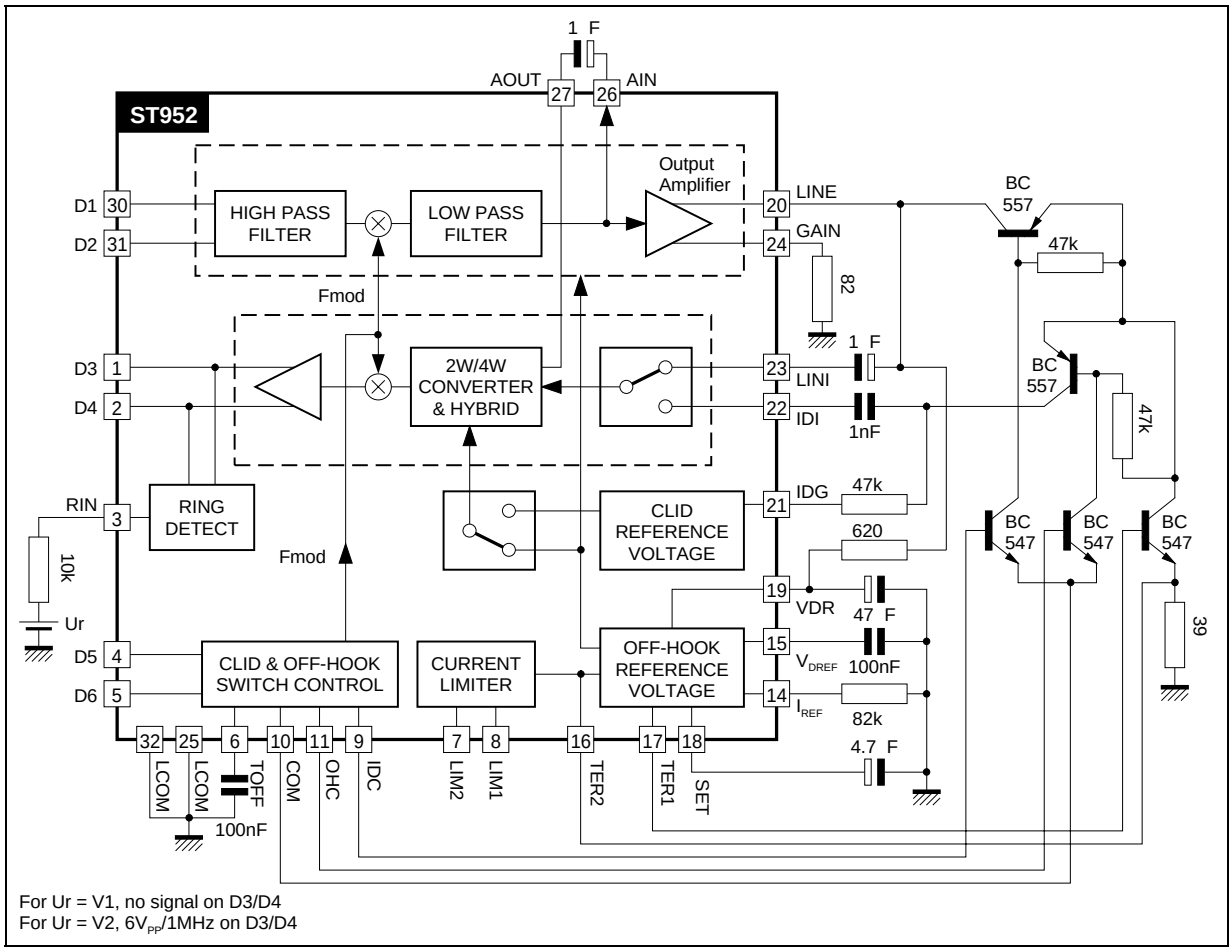
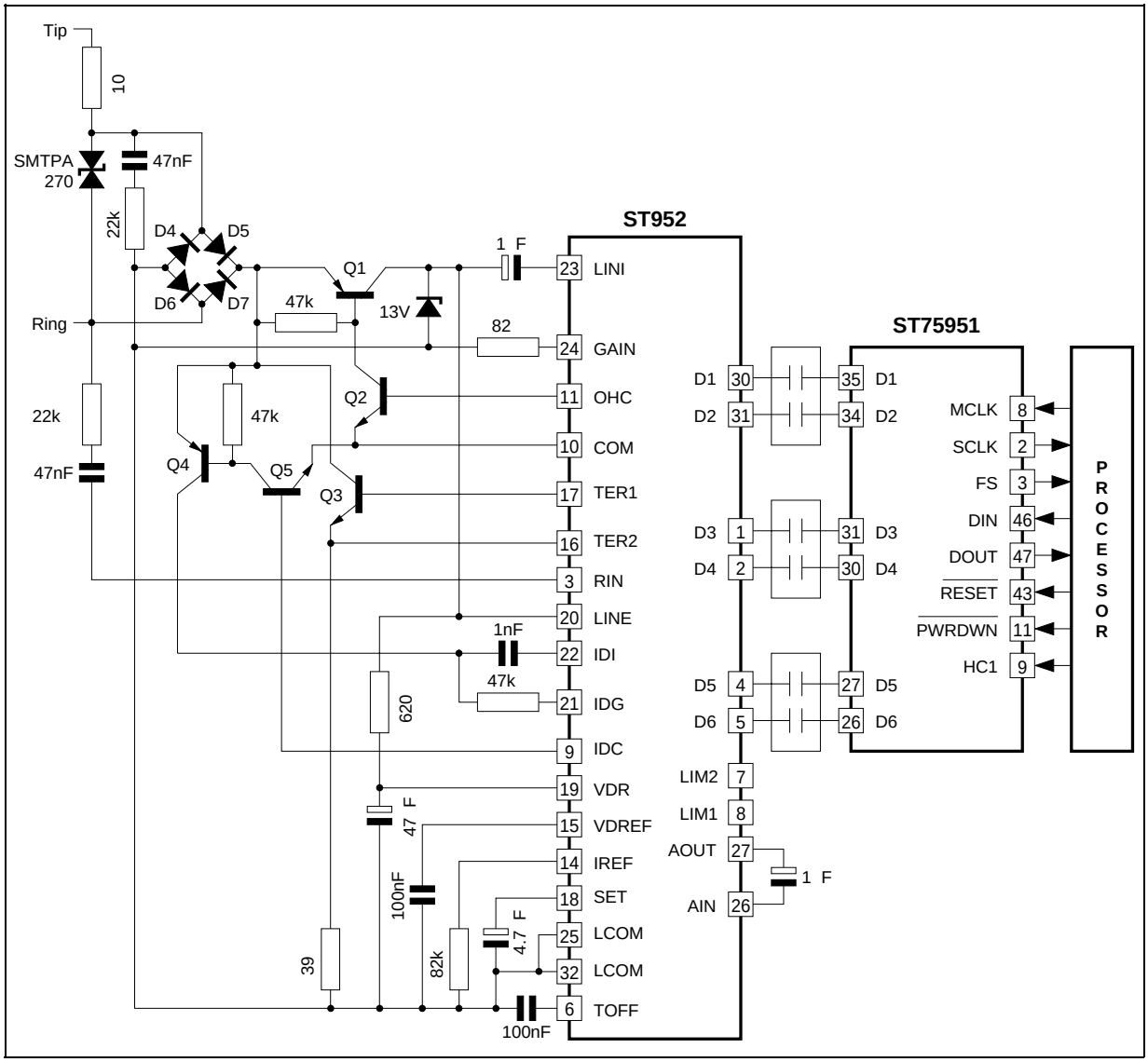


Figure 7 : Test 5

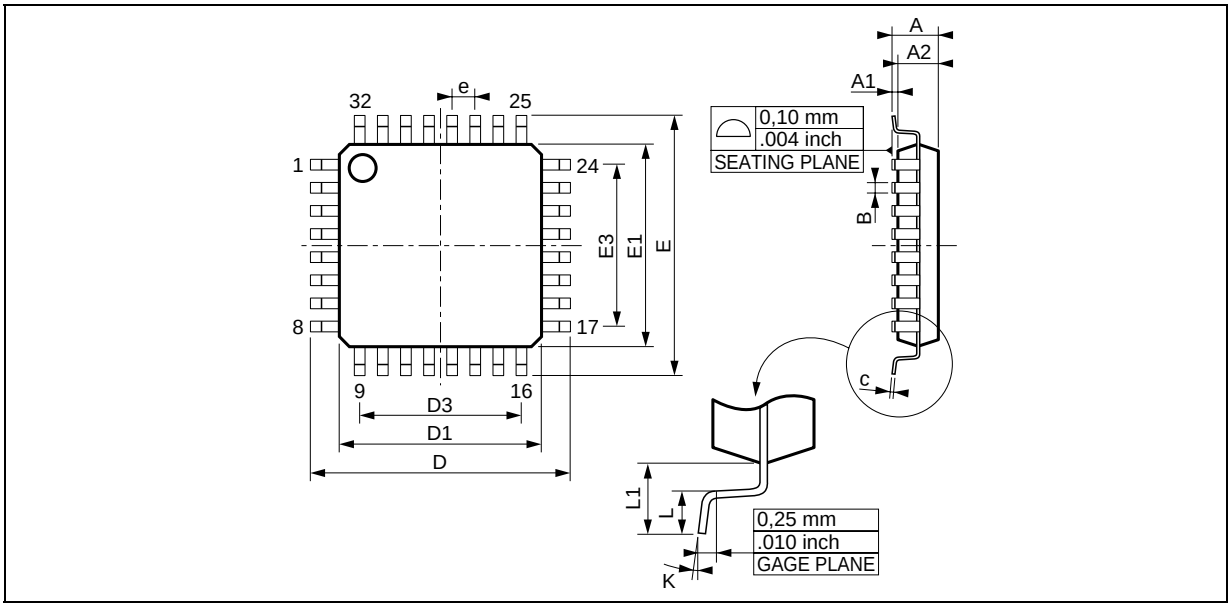


TYPICAL APPLICATION (5V Supply on ST75951)



PACKAGE MECHANICAL DATA

32 PINS - PLASTIC THIN QUAD FLAT PACK (TQFP)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
D3		5.60			0.220	
e		0.80			0.031	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.60			0.220	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0^o (Min.), 7^o (Max.)					

5V.TBL