

TOSHIBA Bipolar Linear Integrated Circuit Silicon Monolithic

TA1318N

SYNC Processor, Frequency Counter IC for TV Component Signals

TA1318N is a sync processor for TV component signals.

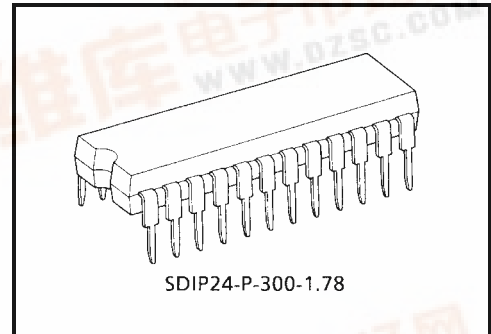
TA1318N provides sync and frequency counter processing for external input signals.

These functions are integrated in a 24 pin dual-in-line shrink-type plastic package.

TA1318N provides I²C bus interface, so various functions and controls are adjustable via the bus.

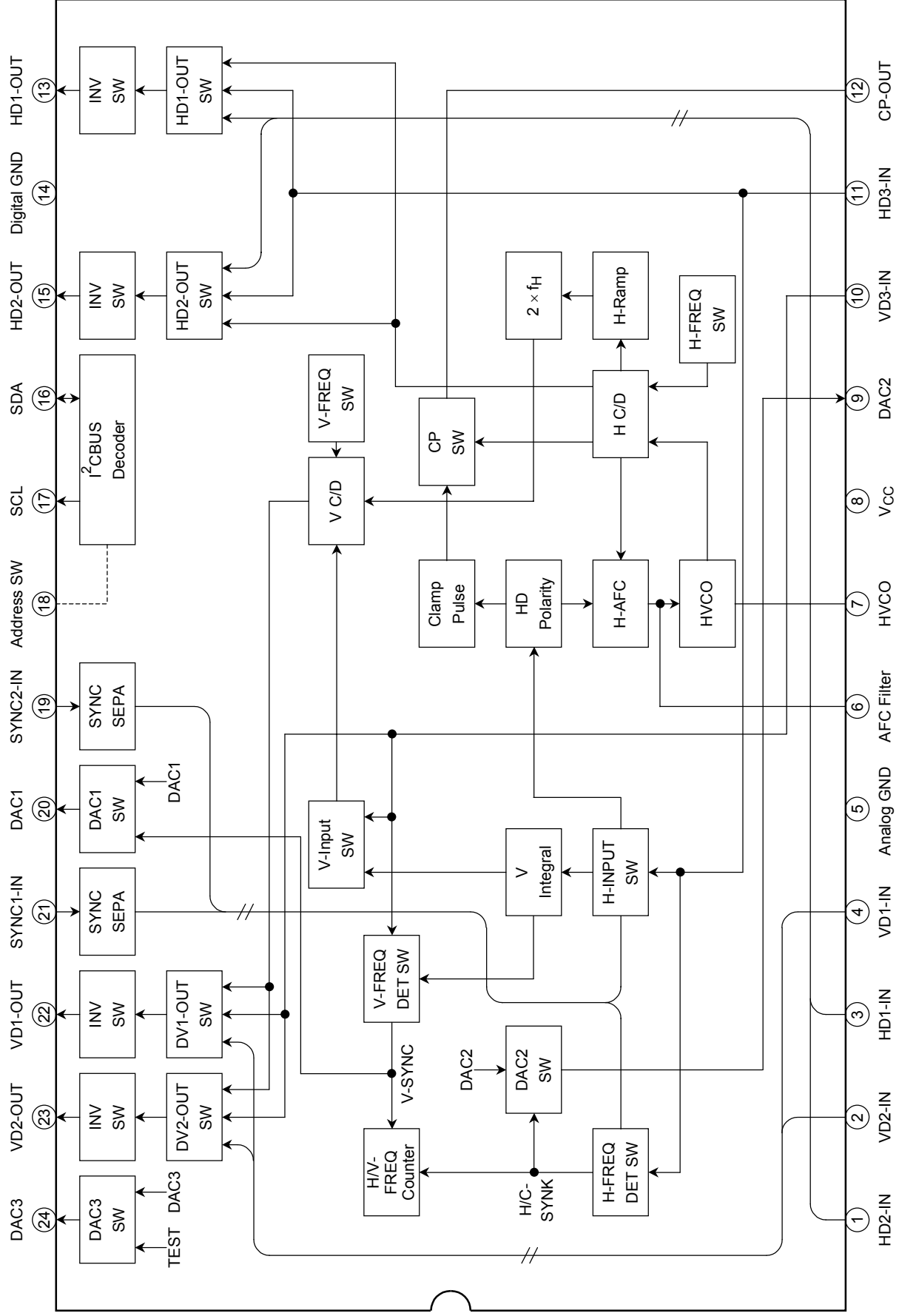
Features

- Horizontal synchronization circuit (15.75 kHz, 31.5 kHz, 33.75 kHz, 45 kHz)
- Vertical synchronization circuit (525I, 525P, 625I, 750P, 1125I, 1125P, PAL 100 Hz, NTSC 120 Hz)
- Horizontal and vertical frequency counter
- Horizontal PLL
- Accepts 2-level and 3-level sync
- Accepts both negative and positive HD and VD
- Clamp pulse output
- HD, VD output (polarity inverter)
- Separated sync output
- Mask for the copy guard signal



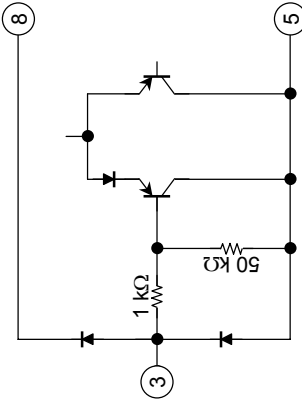
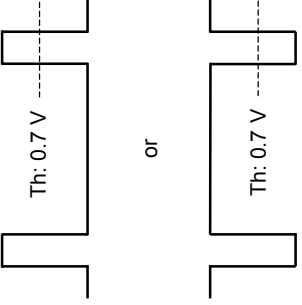
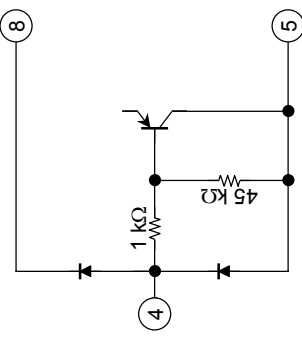
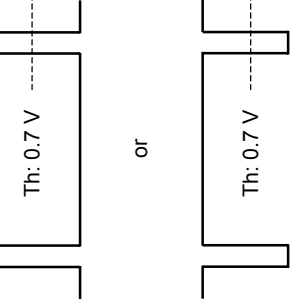
Weight: 1.22 g (typ.)

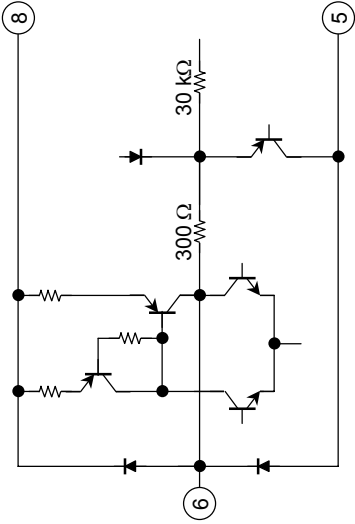
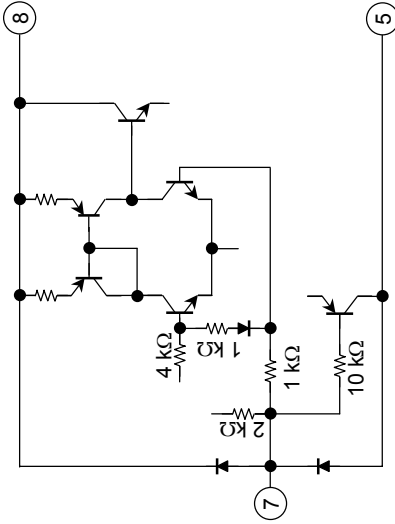
Block Diagram



Pin Functions

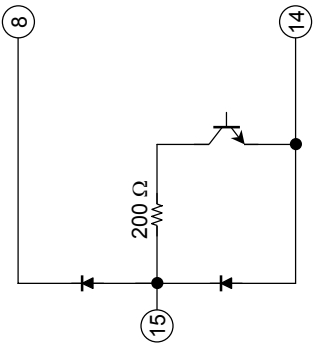
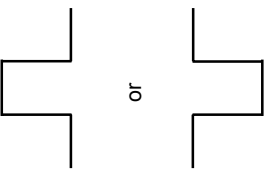
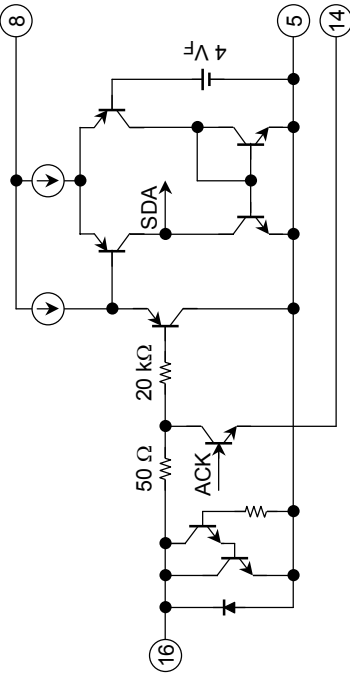

| Pin No. | Pin Name | Function | Interface Circuit | Input Signal/Output Signal |
|---------|----------|---|-------------------|----------------------------|
| 1 | HD2-IN | <p>Inputs horizontal sync signal. Accepts input of both positive and negative polarity. Input signal from this pin is not synchronized.</p> | | |
| 2 | VD2-IN | <p>Inputs vertical sync signal. Accepts input of both positive and negative polarity. Input signal from this pin is not synchronized.</p> | | |

| Pin No. | Pin Name | Function | Interface Circuit | Input Signal/Output Signal |
|---------|------------|--|---|---|
| 3 | HD1-IN | Inputs horizontal sync signal. Accepts input of both positive and negative polarity. Input signal from this pin is not synchronized. |  |  |
| 4 | VD1-IN | Inputs vertical sync signal. Accepts input of both positive and negative polarity. Input signal from this pin is not synchronized. |  |  |
| 5 | Analog GND | GND pin for analog circuit blocks. | — | — |

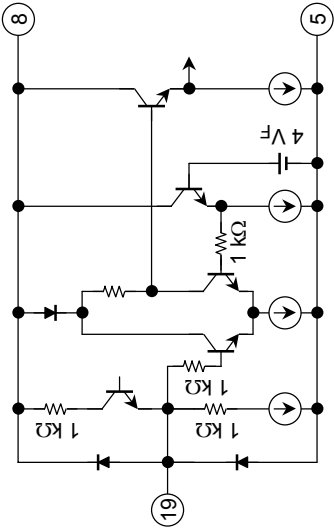
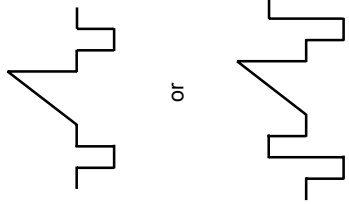
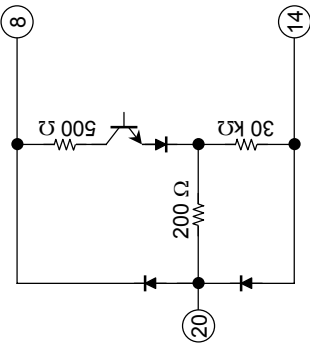
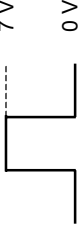
| Pin No. | Pin Name | Function | Interface Circuit | Input Signal/Output Signal |
|---------|-----------------|--|---|----------------------------|
| 6 | AFC Filter | <p>Connects filter for horizontal AFC. Voltage on this pin determines horizontal output frequency.</p> |  | DC |
| 7 | HVCO | <p>Connects ceramic oscillator for horizontal oscillation. Use Murata CSBLA503K/ECZF30.</p> |  | — |
| 8 | V _{CC} | <p>V_{CC} pin. Connects 9 V (typ.).</p> | — | — |

| Pin No. | Pin Name | Function | Interface Circuit | Input Signal/Output Signal |
|---------|-------------------------|--|-------------------|-------------------------------|
| 9 | DAC2 (H/C. SYNC output) | <p>DAC2 output pin.</p> <p>In Test mode, outputs HD or composite sync signal to frequency counter.</p> <p>To improve the driving ability, it is possible to connect a resistor (minimum: 2 kΩ) between this pin and GND. However, when the resistor is added, the output DC voltage is down.</p> | | <p>DC or H/C SYNC</p> |
| 10 | VD3-IN | <p>Inputs vertical sync signal.</p> <p>Accepts input of both positive and negative polarity.</p> | | |
| 11 | HD3-IN | <p>Inputs horizontal sync signal.</p> <p>Accepts input of both positive and negative polarity.</p> | | |

| Pin No. | Pin Name | Function | Interface Circuit | Input Signal/Output Signal |
|---------|-------------|--|-------------------|----------------------------|
| 12 | CP-OUT | Clamp pulse (CP) output pin. Outputs CP generated by sync circuit. | | |
| 13 | HD1-OUT | HD output pin. Open collector output. HD1/HD2 input signal is output from this pin without synchronization. Polarity is switched by BUS write function. | | |
| 14 | Digital GND | GND pin for logic blocks. | — | — |

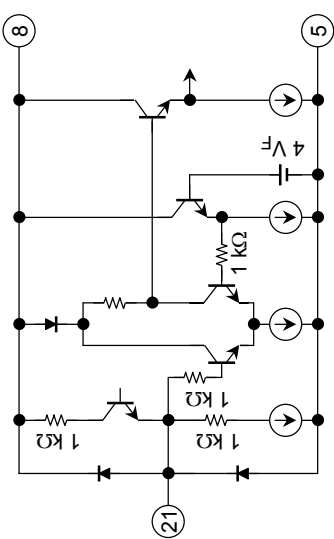
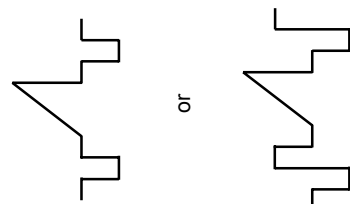
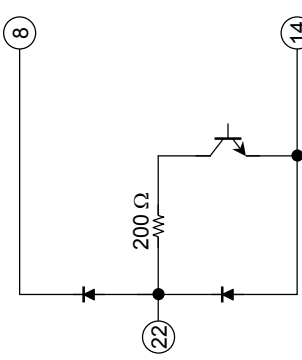
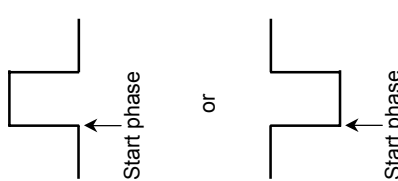
| Pin No. | Pin Name | Function | Interface Circuit | Input Signal/Output Signal |
|---------|----------|--|---|---|
| 15 | HD2-OUT | HD output pin. Open collector output. HD1/HD2 input signal is output from this pin without synchronization. Polarity is switched by BUS write function. |  |  |
| 16 | SDA | SDA pin for I ² C bus. |  |  |

| Pin No. | Pin Name | Function | Interface Circuit | Input Signal/Output Signal |
|---------|------------|---|-------------------|---|
| 17 | SCL | SCL pin for I ² C bus. | | — |
| 18 | Address SW | Slave address switch pin. When this pin is connected to V _{CC} (GND), used for DC/DDH (D8/D9H); when left open, DA/DBH. | | DC/DD — 9 V — 7.5 V DA/DB D8/D9 — 1.5 V — 0 V |

| Pin No. | Pin Name | Function | Interface Circuit | Input Signal/Output Signal |
|---------|----------------------|---|--|--|
| 19 | SYNC2-IN | Inputs Y signal (Note 1) for sync separation circuit. Input via clamp capacitor. |  | White 100% = 1 V _{p-p}  |
| 20 | DAC1 (V SYNC output) | DAC1 output pin. In Test mode, outputs VD or composite sync signal to frequency counter. To improve the driving ability, it is possible to connect a resistor (minimum: 2 kΩ) between this pin and GND. However, when the resistor is added, the output DC voltage is down. |  | DC or V SYNC  |

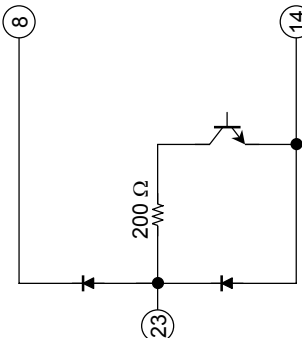
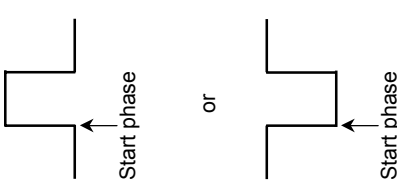
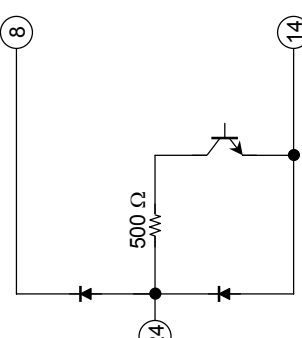
Note 1: The signal format for SYNC1-IN (pin 21) and SYNC2-IN (pin 19)
 NTSC (525/60 Hz), PAL/SECAM (625/50 Hz), NTSC Double Scan (525/120 Hz), PAL/SECAM Double Scan (625/100 Hz), 525P/60 Hz, 750P/60 Hz, 1125/60 Hz, 1125P/30 Hz

This IC doesn't have the sync-separation circuit for non-standard signals like weak strength signal, ghost signal and so on.

| Pin No. | Pin Name | Function | Interface Circuit | Input Signal/Output Signal |
|---------|----------|---|--|---|
| 21 | SYNC1-IN | Inputs Y signal (Note 1) for sync separation circuit. Input via clamp capacitor. |  | <p>White 100% = 1 V_{p-p}</p>  |
| 22 | VD1-OUT | VD output pin. Open collector output. VD1/VD2 input signal is output from this pin without synchronization. Polarity is switched by BUS write function. (Note) When HD PHASE will be changed, synchronized VD width will change. Use the start phase of VD. |  |  |

Note 1: The signal format for SYNC1-IN (pin 21) and SYNC2-IN (pin 19)
 NTSC (525/60 Hz), PAL/SECAM (625/50 Hz), NTSC Double Scan (525/120 Hz), PAL/SECAM Double Scan (625/100 Hz), 525P/60 Hz, 750P/60 Hz,
 1125/60 Hz, 1125P/30 Hz

This IC doesn't have the sync-separation circuit for non-standard signals like weak strength signal, ghost signal and so on.

| Pin No. | Pin Name | Function | Interface Circuit | Input Signal/Output Signal |
|---------|----------|--|--|--|
| 23 | VD2-OUT | <p>VD output pin. Open collector output. VD1/VD2 input signal is output from this pin without synchronization. Polarity is switched by BUS write function. (Note) When HD PHASE will be changed, synchronized VD width will change. Use the start phase of VD.</p> |  |  |
| 24 | DAC3 | <p>DAC3 output pin. Open collector output. In Test mode, outputs test pulse for shipping.</p> |  | <p>DC or test pulse for shipping</p> |

Bus Control Map

Write Mode

Slave Address: D8/DA/DC_H

| Sub-Add | D7 MSB | D6 | D5 | D4 | D3 | D2 | D1 | D0 LSB | Preset | |
|---------|-------------|----|----------------|---------|----------------|------|------------|---------|--------|------|
| | | | | | | | | | MSB | LSB |
| 00 | H-FREQUENCY | | HD1/VD1-OUT SW | | HD2/VD2-OUT SW | | SEPA LEVEL | | 1000 | 0000 |
| 01 | DAC1 | | DAC2 | | DAC3 | TEST | HD1-INV | HD2-INV | 1000 | 0000 |
| 02 | V-FREQUENCY | | | CLP-PHS | FREQ DET SW | | INPUT SW | | 1000 | 0000 |
| 03 | HD PHASE | | | | | | VD1-INV | VD2-INV | 1000 | 0000 |

Read Mode

Slave Address: D9/DB/DD_H

| | D7 MSB | D6 | D5 | D4 | D3 | D2 | D1 | D0 LSB |
|---|--------|-----------------|----|----|----|----|----|--------|
| 0 | POR | V FREQUENCY DET | | | | | | |
| 1 | HD-IN | H FREQUENCY DET | | | | | | |

Bus Control Functions

Write Mode (*: Preset)

- H-FREQUENCY (Horizontal oscillation frequency)
Switches horizontal frequency.
(00): 15.75 kHz (01): 31.5 kHz *(10): 33.75 kHz (11): 45 kHz
- HD1/VD1-OUT SW (HD1/VD1 output switch)
Switches output from pin 13/22. When set to 00, 01, or 10, outputs HD/VD without synchronization. When set to 11, outputs HD/VD from the sync circuit. (Note) Synchronized VD width will change, when HD PHASE will be changed.
*(00): HD1/VD1 (01): HD2/VD2 (10): HD3/VD3 (11): Synchronized HD/VD
- HD2/VD2-OUT SW (HD2/VD2 output switch)
Switches output from pin 15/23. When set to 00, 01, or 10, outputs HD/VD without synchronization. When set to 11, outputs HD/VD from the sync circuit.
*(00): HD1/VD1 (01): HD2/VD2 (10): HD3/VD3 (11): Synchronized HD/VD
- SEPA LEVEL (Sync separation level switch)
Switches sync separation level of pin 19/21. Set values are the levels from sync tip. Sync separation level is changed according to the ratio of H-SYNC width during 1H period.
*(00): 10IRE (01): 15IRE (10): 20IRE (11): 25IRE (at 1125I/60)
- DAC1 (DAC1 control)
Controls 2-bit DAC (pin 9).
(00): 1 V (01): 3 V *(10): 5 V (11): 7 V
- DAC2 (DAC2 control)
Controls 2-bit DAC (pin 20).
*(00): 1 V (01): 3 V (10): 5 V (11): 7 V
- DAC3 (DAC3 control)
Controls open collector 1-bit DAC (pin 24).
*(0): OPEN (HIGH) (1): ON (LOW)
- TEST (Test mode)
Switches DAC1, 2, and 3 outputs. Also used to test IC for shipping.
*(0): DAC outputs are used as DAC.
(1): DAC1 outputs V. SYNC to the frequency counter.
DAC2 outputs H. SYNC or C. SYNC to the frequency counter.
DAC3 outputs IC test pulse for shipping.

- HD1-INV (HD1 output polarity switch)
Switches HD1 output (pin 13) polarity. When set to 0, positive HD input is output as negative HD. When set to 0, output from the sync circuit is output as negative HD.
*(0): Normal (1): Inverse
- HD2-INV (HD2 output polarity switch)
Switches HD1 output (pin 15) polarity. When set to 0, positive HD input is output as negative HD. When set to 0, output from the sync circuit is output as negative HD.
*(0): Normal (1): Inverse
- V-FREQUENCY (Vertical frequency switch (pull-in range))
Sets vertical frequency pull-in range, VD-STOP, or free-running frequency.
Free-running frequency is controlled by H-FREQUENCY.

| | Pull-in Range | Format/H (V) Frequency |
|--------|---------------|---|
| *(000) | 48~1281 H | 1125P/30 Hz (33.75 kHz) |
| (001) | 48~849 H | 750P/60 Hz (45 kHz) |
| (010) | FREE-RUN | Free-running frequency is controlled by H-FREQUENCY. (00): 262 H (01): 525 H (10): 562 H (11): 750 H |
| (011) | 48~637 H | 1125I/60 Hz (33.75 kHz) |
| (100) | 48~613 H | 525P/60 Hz (31.5 kHz) |
| (101) | 48~363 H | PAL/SECAM/50 Hz (15.625 kHz) PAL/SECAM double scan/100 Hz (31.5 kHz) |
| (110) | 48~307 H | NTSC/60 Hz (15.734 kHz) NTSC double scan /120 Hz (31.5 kHz) |
| (111) | VP STOP | VD output is HIGH |

- CLP PHS (Clamp pulse phase switch)
Switches clamp pulse phase.
If no signal input, 0.9 μs pulse is output from the H-C/D circuit.
*(0): 1 μs (3.4%) delay following HD stop phase, 0.8 μs (2.7%) pulse
(1): 0.5 μs (1.7%) delay following HD stop phase, 0.8 μs (2.7%) pulse
- FREQ DET SW (Horizontal/vertical frequency counter switch)
Switches input signal used for horizontal/vertical frequency counter. This switch is controlled independently from INPUT SW. The detection result is output as read BUS data.
*(00): SYNC1 input (01): SYNC2 input (10)/(11): HD3/VD3 inputs
- INPUT SW (Input signal switch for synchronization)
Switches input signal used for synchronization.
*(00): SYNC1 input (01): SYNC2 input (10)/(11): HD3/VD3 inputs
- HD PHASE (HD phase adjustment)
Adjusts phase of HD output from the sync circuit. The phase of the adjustment center value is the same as that of input H-SYNC or input HD. (Note) Synchronized VD width will change, when HD PHASE will be changed.
(000000): -5% (H periodically)
*(100000): 0%
(111111) : 5%
- VD1-INV (VD1 output polarity switch)
Switches VD1 output (pin 22) polarity. When set to 0, negative VD input is output as negative VD. When set to 0, output from the sync circuit is output as negative VD.
*(0): Normal (1): Inverse
- VD2-INV (VD2 output polarity switch)
Switches VD2 output (pin 23) polarity. When set to 0, negative VD input is output as negative VD. When set to 0, output from the sync circuit is output as negative VD.
*(0): Normal (1): Inverse

Read Mode

- POR (Power on reset)
 - (0): Status read (at second data read and subsequent)
 - (1): Power on (at first data read)
- HD-IN (Input signal self-check result)
 - Detects HD or H-SYNC input signal selected by INPUT SW.
 - (0): No signal input (1): Signal input
- V FREQ DET (Vertical frequency of SYNC or VD input selected by FREQ DET SW)
 - (0000000)~(0001100): No-VD
 - (0001101): Vicinity of 162 Hz
 - (1111110) : Vicinity of 17 Hz

How to calculate vertical frequency (X):

Convert V-FREQ DET read data into decimal and define the resulting value as Y.

Where H-FREQUENCY is 15.75 kHz/31.5 kHz, Z = 476.2 μs

Where H-FREQUENCY is 33.75 kHz/45 kHz, Z = 474.1 μs

$$\text{Vertical frequency (X)} = 1 \div (Y \times Z) \text{ [Hz]}$$

Error of Y is +1, -0. If vertical frequency is 162 Hz or more, the frequency cannot be accurately measured. Time constant used to separate V.SYNC from integrated C.SYNC is 9 μs (error: ±1 μs).

- H FREQ DET (Horizontal frequency of SYNC or HD input selected by FREQ DET SW)
 - (0000000): No signal input (1111110): 53 kHz or more

How to calculate horizontal frequency (X):

X, Y, and Z are defined same as for V FREQ.

$$\text{Horizontal frequency (X)} = Y \div (5 \times Z) \text{ [kHz]}$$

Error of Y is +1, -0. If horizontal frequency is 53 kHz or more, the frequency cannot be accurately measured. When V-SYNC or VD is not input, horizontal frequency cannot be measured, resulting in data = (0000000).

Note 1: The start trigger for frequency counting is the internal reset-pulse made from ACK of 2nd byte in BUS read mode. The counting period is between the first V-sync (VD) and the second V-sync (VD) after the trigger.

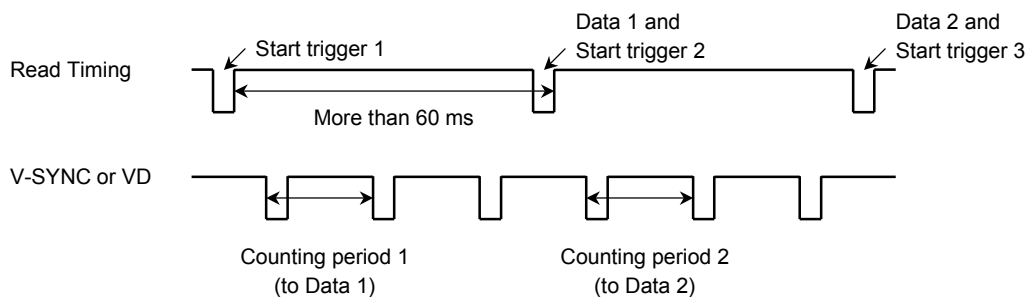
The counted data will have +1 or -0 error according to the read timing.

To assume stable data reading;

1. Set BUS reading interval more than 60 ms.
2. Don't use the first data because it is unsettled.

are recommended.

Note 2: Ignore data (1111111). This data may be obtained in case the trigger pulse and the V-sync (VD) are simultaneous.



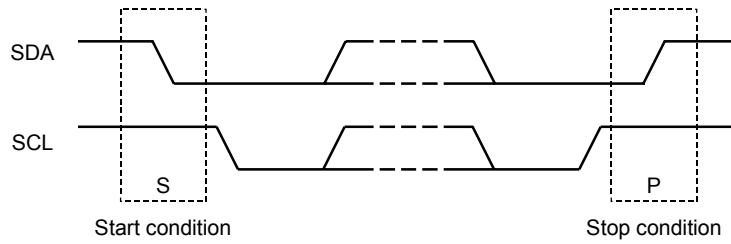
Decision algorithm (detection range, detection times and so on) should be determined under consideration of Note 1, Note 2 and the other factors such as signal strength, existence of ghost signal, H-AFC stability, I²C BUS data transmission and so on via prototype TV set evaluation.

Data Transfer Format via I²C BUS

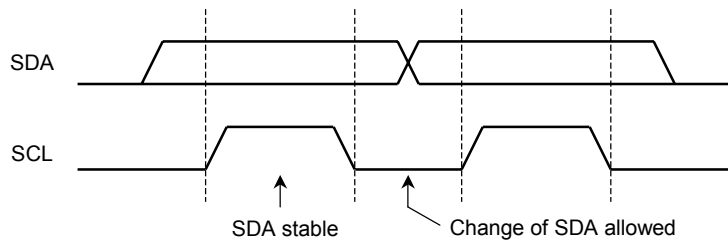
Slave Address: D8/DA/DC_H

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | W/R |
|----|----|----|----|----|-----|-----|-----|
| 1 | 1 | 0 | 1 | 1 | 0/1 | 0/1 | 0/1 |

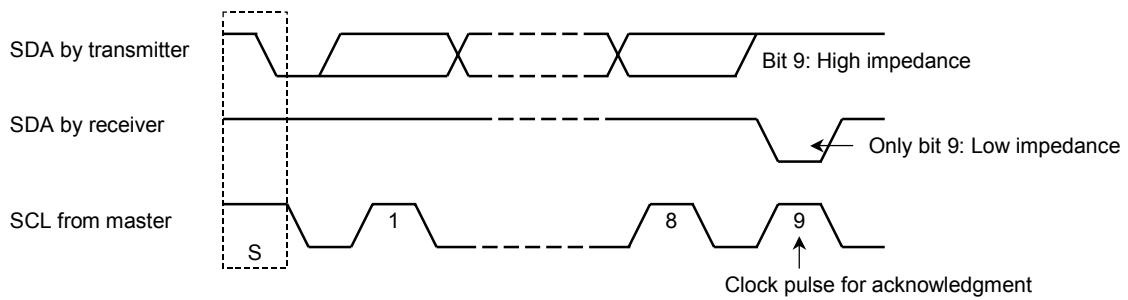
Start and Stop Condition



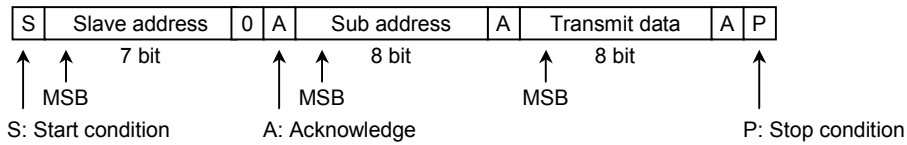
Bit Transfer



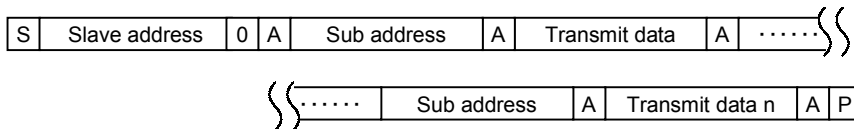
Acknowledge



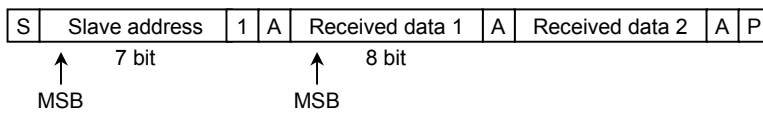
Data Transmit Format 1



Data Transmit Format 2



Data Receive Format



At the moment of the first acknowledge, the master transmitter becomes a master receiver and the slave transmitter. This acknowledge is still generated by this slave.

The Stop condition is generated by the master.

(* important) The data read from THIS IC should always be completed in whole two words, not one word, otherwise the IICBUS may cause error.

Optional Data Transmit Format: Automatic Increment Mode



In this transmission method, data is set on automatically incremented sub-address from the specified sub-address.

Purchase of TOSHIBA I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Maximum Ratings (Ta = 25°C)

| Characteristics | Symbol | Rating | Unit |
|----------------------------------|-------------|---------|-----------|
| Supply voltage | V_{CCmax} | 12 | V |
| Input pin signal voltage | e_{inmax} | 9 | V_{p-p} |
| Power dissipation | P_D (*1) | 1250 | mW |
| Power dissipation reduction rate | $1/Q_{ja}$ | -10 | $mW/°C$ |
| Operating temperature | T_{opr} | -20~65 | °C |
| Storage temperature | T_{stg} | -55~150 | °C |

Note: Refer to the figure below.

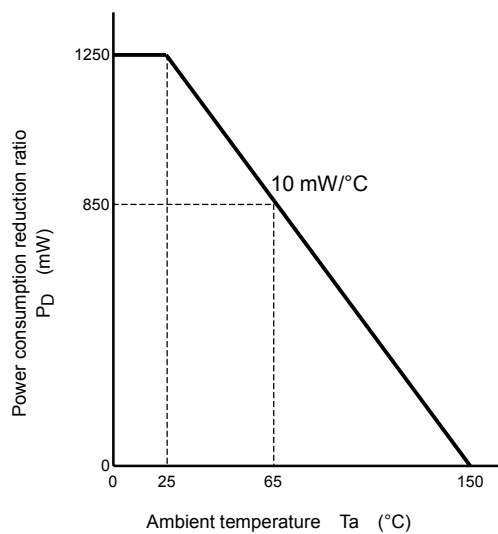


Figure PD - Ta Curve

Operating Condition

| Characteristics | | Description | Min | Typ. | Max | Unit | |
|--------------------------------------|---------------------|---|--------------------|------|-------|-----------|---|
| Power supply voltage (V_{CC}) | | Pin 8 | 8.5 | 9.0 | 9.5 | V | |
| HD1, HD2, HD3 Input level | | Pin 3, 1, 11 | 2.0 | 5.0 | 9.0 | V_{p-p} | |
| VD1, VD2, VD3 Input level | | Pin 4, 2, 10 | 2.0 | 5.0 | 9.0 | | |
| HD3 input width | Synchronization | Pin 11 | 0.02 | — | 0.20 | H | |
| | Frequency detection | Pin 11 | 0.45 μ s | — | 0.25H | — | |
| VD3 input width | Synchronization | Pin 10 | 1 μ s | — | 47H | — | |
| | Frequency detection | Pin 10 | 1 | — | 400 | μ s | |
| SYNC1, SYNC2 Input level | | Pin 21, 19, white 100% with negative sync | 0.9 | 1.0 | 1.1 | V_{p-p} | |
| HD1, HD2, VD1, VD2-OUT Input current | | Pin 13, 15, 22, 23 | — | 0.9 | 1.5 | mA | |
| DAC3 Input current | | Pin 24 | — | 0.5 | 1.0 | | |
| Address switching voltage | | Pin 18 | D8/D9 _H | 0 | 0 | 1.0 | V |
| | | | DC/DD _H | 8.0 | 9.0 | 9.0 | |

Electrical Characteristics (V_{CC} = 9 V, Ta = 25°C, unless otherwise specified)

Current Dissipation

| Pin Name | Symbol | Test Circuit | Min | Typ. | Max | Unit |
|-----------------|-----------------|--------------|-----|------|-----|------|
| V _{CC} | I _{CC} | — | 32 | 38 | 44 | mA |

AC Characteristics

Horizontal Block

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|--|--------------------|--------------|----------------|-------|-------|-------|------------------|
| Sync1/2 input horizontal sync phase | S _{1PH} | — | (Note HA01) | 0.6 | 0.7 | 0.8 | μs |
| | S _{2PH} | — | | 0.6 | 0.7 | 0.8 | |
| HD3 input horizontal sync phase | HD _{3PH} | — | (Note HA02) | 0.6 | 0.7 | 0.8 | μs |
| Polarity distinction active range | HD-DUTY1 | — | (Note HA03) | 61 | 66 | 71 | % |
| | HD-DUTY2 | — | | 48 | 53 | 58 | |
| Sync1 input threshold amplitude Sync2 input threshold amplitude | V _{thS10} | — | (Note HA04) | 0.040 | 0.070 | 0.100 | V _{p-p} |
| | V _{thS11} | — | | 0.060 | 0.106 | 0.152 | |
| | V _{thS12} | — | | 0.081 | 0.142 | 0.203 | |
| | V _{thS13} | — | | 0.102 | 0.178 | 0.255 | |
| | V _{thS20} | — | | 0.040 | 0.070 | 0.100 | |
| | V _{thS21} | — | | 0.060 | 0.106 | 0.152 | |
| | V _{thS22} | — | | 0.081 | 0.142 | 0.203 | |
| V _{thS23} | — | 0.102 | 0.178 | 0.255 | | | |
| HD3 input threshold amplitude (Synchronization block) | V _{thHD3} | — | (Note HA05) | 0.65 | 0.75 | 0.85 | V _{p-p} |
| HD1 input threshold voltage HD2 input threshold voltage HD3 input threshold voltage (SW block) | V _{thHD1} | — | (Note HA06) | 0.65 | 0.75 | 0.85 | V _{p-p} |
| | V _{thHD2} | — | | 0.65 | 0.75 | 0.85 | |
| | V _{thHD3} | — | | 0.65 | 0.75 | 0.85 | |
| HD output phase adjustment variable range | ΔHP0- | — | (Note HA07) | 2.86 | 3.18 | 3.49 | μs |
| | ΔHP0+ | — | | 2.86 | 3.18 | 3.49 | |
| | ΔHP1- | — | | 1.43 | 1.59 | 1.75 | |
| | ΔHP1+ | — | | 1.43 | 1.59 | 1.75 | |
| | ΔHP2- | — | | 1.33 | 1.48 | 1.63 | |
| | ΔHP2+ | — | | 1.33 | 1.48 | 1.63 | |
| | ΔHP3- | — | | 1.00 | 1.11 | 1.22 | |
| ΔHP3+ | — | 1.00 | 1.11 | 1.22 | | | |
| Clamp pulse phase/width/level | CP _{S0} | — | (Note HA08) | 0.85 | 1.00 | 1.15 | μs |
| | CP _{W0} | — | | 0.65 | 0.80 | 0.95 | μs |
| | CP _{V0} | — | | 4.7 | 5.0 | 5.3 | V |
| | CP _{S1} | — | | 0.35 | 0.50 | 0.65 | μs |
| | CP _{W1} | — | | 0.65 | 0.80 | 0.95 | μs |
| | CP _{V1} | — | | 4.7 | 5.0 | 5.3 | V |
| | CP _{S3} | — | | 0 | — | 1 | μs |
| | CP _{W3} | — | | 0.50 | 0.90 | 1.30 | μs |
| CP _{V3} | — | 4.7 | 5.0 | 5.3 | V | | |

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---------------------------------------|------------|--------------|----------------|-----|------|-----|---------------|
| Delayed HD pulse width | W_{d-HD} | — | (Note HA09) | 1.0 | 1.2 | 1.4 | μs |
| HD1 output voltage | V13TH0 | — | — | 4.5 | 5.0 | 5.5 | V |
| | V13TL0 | — | | — | 0.1 | 0.5 | |
| | V13TH1 | — | | 4.5 | 5.0 | 5.5 | |
| | V13TL1 | — | | — | 0.1 | 0.5 | |
| | V13TH2 | — | | 4.5 | 5.0 | 5.5 | |
| | V13TL2 | — | | — | 0.1 | 0.5 | |
| | V13TH3 | — | | 4.5 | 5.0 | 5.5 | |
| | V13TL3 | — | | — | 0.1 | 0.5 | |
| HD2 output voltage | V15TH0 | — | — | 4.5 | 5.0 | 5.5 | V |
| | V15TL0 | — | | — | 0.1 | 0.5 | |
| | V15TH1 | — | | 4.5 | 5.0 | 5.5 | |
| | V15TL1 | — | | — | 0.1 | 0.5 | |
| | V15TH2 | — | | 4.5 | 5.0 | 5.5 | |
| | V15TL2 | — | | — | 0.1 | 0.5 | |
| | V15TH3 | — | | 4.5 | 5.0 | 5.5 | |
| | V15TL3 | — | | — | 0.1 | 0.5 | |
| HD1 output voltage (polarity inverse) | V13IH0 | — | — | 4.5 | 5.0 | 5.5 | V |
| | V13IL0 | — | | — | 0.1 | 0.5 | |
| | V13IH1 | — | | 4.5 | 5.0 | 5.5 | |
| | V13IL1 | — | | — | 0.1 | 0.5 | |
| | V13IH2 | — | | 4.5 | 5.0 | 5.5 | |
| | V13IL2 | — | | — | 0.1 | 0.5 | |
| | V13IH3 | — | | 4.5 | 5.0 | 5.5 | |
| | V13IL3 | — | | — | 0.1 | 0.5 | |
| HD2 output voltage (polarity inverse) | V15IH0 | — | — | 4.5 | 5.0 | 5.5 | V |
| | V15IL0 | — | | — | 0.1 | 0.5 | |
| | V15IH1 | — | | 4.5 | 5.0 | 5.5 | |
| | V15IL1 | — | | — | 0.1 | 0.5 | |
| | V15IH2 | — | | 4.5 | 5.0 | 5.5 | |
| | V15IL2 | — | | — | 0.1 | 0.5 | |
| | V15IH3 | — | | 4.5 | 5.0 | 5.5 | |
| | V15IL3 | — | | — | 0.1 | 0.5 | |
| AFC phase detection current | ID1 | — | (Note HB01) | 310 | 385 | 460 | μA |
| | ID2 | — | | 310 | 385 | 460 | |
| | ID3 | — | | 520 | 650 | 780 | |
| | ID4 | — | | 520 | 650 | 780 | |
| VCO oscillation start voltage | V_{VCO} | — | (Note HB02) | 3.9 | 4.2 | 4.5 | V |
| HD output pulse width (free-run) | TH00 | — | (Note HB03) | 1.4 | 1.8 | 2.2 | μs |
| | TH01 | — | | 1.4 | 1.8 | 2.2 | |
| | TH10 | — | | 1.4 | 1.8 | 2.2 | |
| | TH11 | — | | 1.4 | 1.8 | 2.2 | |

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|--|--------------------|--------------|----------------|-------|--------|-------|-------|
| Horizontal free-run frequency | F00 | — | (Note HB04) | 15.59 | 15.75 | 15.91 | kHz |
| | F01 | — | | 31.19 | 31.5 | 31.82 | |
| | F10 | — | | 33.41 | 33.75 | 34.09 | |
| | F11 | — | | 44.55 | 45 | 45.45 | |
| | F50 | — | | 15.47 | 15.625 | 15.78 | |
| Horizontal oscillation control sensitivity | BH00 | — | (Note HB05) | 2.4 | 3.0 | 3.6 | kHz/V |
| | BH01 | — | | 4.8 | 6.0 | 7.2 | |
| | BH10 | — | | 4.8 | 6.0 | 7.2 | |
| | BH10 | — | | 7.1 | 8.9 | 10.7 | |
| DAC1 output voltage | VDAC ₁₀ | — | — | 0.5 | 1.0 | 1.5 | V |
| | VDAC ₁₁ | — | | 2.7 | 3.0 | 3.3 | |
| | VDAC ₁₂ | — | | 4.7 | 5.0 | 5.3 | |
| | VDAC ₁₃ | — | | 6.5 | 7.0 | 7.5 | |
| DAC2 output voltage | VDAC ₂₀ | — | — | 0.5 | 1.0 | 1.5 | V |
| | VDAC ₂₁ | — | | 2.7 | 3.0 | 3.3 | |
| | VDAC ₂₂ | — | | 4.7 | 5.0 | 5.3 | |
| | VDAC ₂₃ | — | | 6.5 | 7.0 | 7.5 | |
| DAC3 output voltage | VDAC ₃₀ | — | — | — | 0.5 | 0.7 | V |
| | VDAC ₃₁ | — | | 8.5 | 8.8 | — | |

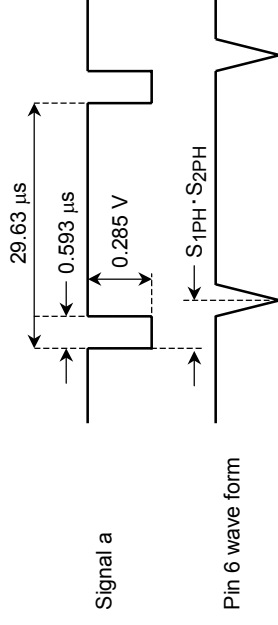
Vertical Block

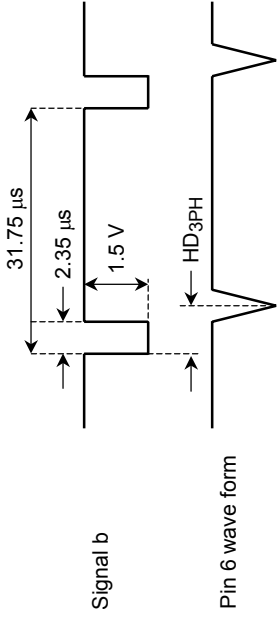
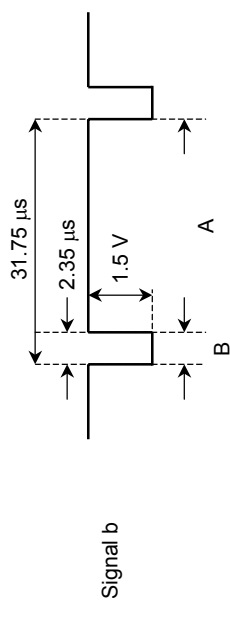
| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|-------------|--------------|----------------|------|------|------|-----------|
| VD1 input threshold voltage VD2 input threshold voltage VD3 input threshold voltage (SW block) | V_{thVD1} | — | (Note VA01) | 0.65 | 0.75 | 0.85 | V_{p-p} |
| | V_{thVD2} | — | | 0.65 | 0.75 | 0.85 | |
| | V_{thVD3} | — | | 0.65 | 0.75 | 0.85 | |
| VD3 input threshold voltage (synchronization block) | V_{thVD3} | — | (Note VA02) | 0.65 | 0.75 | 0.85 | V_{p-p} |
| VD1 output voltage | V22TH0 | — | — | 4.5 | 5.0 | 5.5 | V |
| | V22TL0 | — | | — | 0.1 | 0.5 | |
| | V22TH1 | — | | 4.5 | 5.0 | 5.5 | |
| | V22TL1 | — | | — | 0.1 | 0.5 | |
| | V22TH2 | — | | 4.5 | 5.0 | 5.5 | |
| | V22TL2 | — | | — | 0.1 | 0.5 | |
| | V22TH3 | — | | 4.5 | 5.0 | 5.5 | |
| | V22TL3 | — | | — | 0.1 | 0.5 | |
| VD2 output voltage | V23TH0 | — | — | 4.5 | 5.0 | 5.5 | V |
| | V23TL0 | — | | — | 0.1 | 0.5 | |
| | V23TH1 | — | | 4.5 | 5.0 | 5.5 | |
| | V23TL1 | — | | — | 0.1 | 0.5 | |
| | V23TH2 | — | | 4.5 | 5.0 | 5.5 | |
| | V23TL2 | — | | — | 0.1 | 0.5 | |
| | V23TH3 | — | | 4.5 | 5.0 | 5.5 | |
| | V23TL3 | — | | — | 0.1 | 0.5 | |
| VD1 output voltage (polarity inverse) | V22IH0 | — | — | 4.5 | 5.0 | 5.5 | V |
| | V22IL0 | — | | — | 0.1 | 0.5 | |
| | V22IH1 | — | | 4.5 | 5.0 | 5.5 | |
| | V22IL1 | — | | — | 0.1 | 0.5 | |
| | V22IH2 | — | | 4.5 | 5.0 | 5.5 | |
| | V22IL2 | — | | — | 0.1 | 0.5 | |
| | V22IH3 | — | | 4.5 | 5.0 | 5.5 | |
| | V22IL3 | — | | — | 0.1 | 0.5 | |
| VD2 output voltage (polarity inverse) | V23IH0 | — | — | 4.5 | 5.0 | 5.5 | V |
| | V23IL0 | — | | — | 0.1 | 0.5 | |
| | V23IH1 | — | | 4.5 | 5.0 | 5.5 | |
| | V23IL1 | — | | — | 0.1 | 0.5 | |
| | V23IH2 | — | | 4.5 | 5.0 | 5.5 | |
| | V23IL2 | — | | — | 0.1 | 0.5 | |
| | V23IH3 | — | | 4.5 | 5.0 | 5.5 | |
| | V23IL3 | — | | — | 0.1 | 0.5 | |
| Vertical output pulse width | VP_{W0} | — | (Note VA03) | 251 | 286 | 321 | μs |
| | VP_{W1} | — | | 126 | 143 | 160 | |
| | VP_{W2} | — | | 117 | 133 | 150 | |
| | VP_{W3} | — | | 88 | 100 | 112 | |

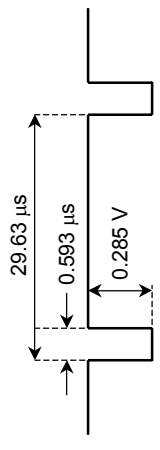
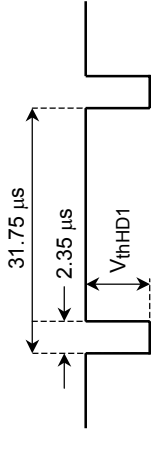
| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---------------------------------------|-----------|--------------|----------------|-------|-------|-------|------|
| Vertical free-run frequency | FV0 | — | (Note VA04) | 26.02 | 26.35 | 26.67 | Hz |
| | FV1 | — | | 39.21 | 39.75 | 40.30 | |
| | FV3 | — | | 52.20 | 52.98 | 53.77 | |
| | FV4 | — | | 54.24 | 55.06 | 55.89 | |
| | FV5 | — | | 91.28 | 92.98 | 94.69 | |
| | FV6 | — | | 107.8 | 109.9 | 112.1 | |
| | FV20 | — | | 57.0 | 60.0 | 63.0 | |
| | FV21 | — | | 57.0 | 60.0 | 63.0 | |
| | FV22 | — | | 57.0 | 60.0 | 63.0 | |
| | FV23 | — | | 57.0 | 60.0 | 63.0 | |
| Vertical pull-in range | FVPL0 | — | (Note VA05) | 311 | 321 | 332 | Hz |
| | FVPL1 | — | | 624 | 643 | 663 | |
| | FVPL2 | — | | 668 | 689 | 710 | |
| | FVPL3 | — | | 891 | 918 | 947 | |
| Sync input-VD output phase difference | 15.75 kHz | — | — | 9.6 | 11.8 | 14.0 | μs |
| | 31.50 kHz | — | | 5.7 | 6.8 | 7.9 | |
| | 33.75 kHz | — | | 5.3 | 6.4 | 7.5 | |
| | 45.00 kHz | — | | 4.4 | 5.2 | 6.0 | |

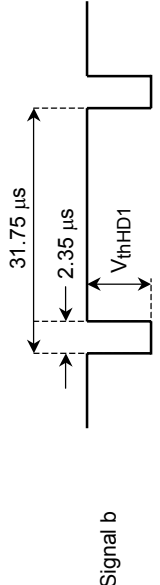
Test Conditions and Measuring Method

| Note | Item | SW Mode | | | | Test Conditions and Measuring Method (V _{CC} = 9 V, T _a = 25 ± 3°C, unless otherwise specified) |
|------|-------------------------------------|---------|-----|-------------|-------------|--|
| | | S06 | S18 | S19 | S21 | |
| HA01 | Sync1/2 input horizontal sync phase | c | b | a ↓ b | b ↓ a | <p>(1) Set sub-address (02) 60. (2) SW19-a and SW21-b. (3) Input Signal a (horizontal 33.75 kHz) to pin 21 (SYNC1-IN). (4) Set sub-address (02) 61. (5) Measure the phase difference S_{1PH} between pin 21 and pin 6 (AFC filter) wave form. (6) SW19-b and SW21-a. (7) Input Signal a (33.75 kHz) to pin 19 (SYNC2-IN). (8) Set sub-address (02) 01. (9) Measure the phase difference S_{2PH} between pin 19 and pin 6 (AFC filter) wave form.</p> |

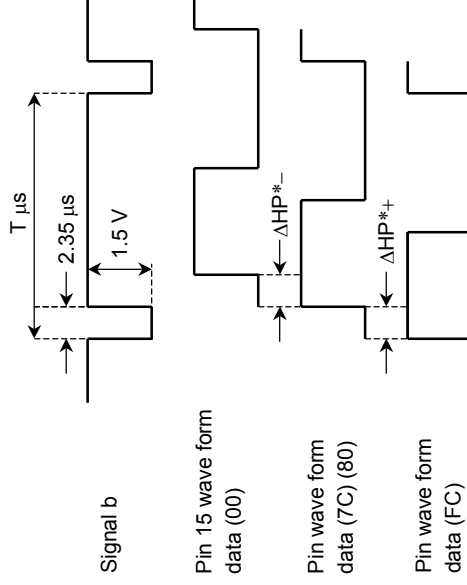


| Note | Item | SW Mode | | | | Test Conditions and Measuring Method (V _{CC} = 9 V, T _a = 25 ± 3°C, unless otherwise specified) |
|------|-----------------------------------|---------|-----|-----|-----|--|
| | | S06 | S18 | S19 | S21 | |
| HA02 | HD3 input horizontal sync phase | c | b | — | — | <p>(1) Set sub-address (00) 40 and (02) 82. (2) Input signal b (horizontal 31.5 kHz) to pin 11 (HD3-IN). (3) Measure the phase difference HD_{3PH} between pin 11 and pin 6 (AFC filter) wave form.</p>  |
| HA03 | Polarity distinction active range | c | b | — | — | <p>(1) Set sub-address (00) 70 and (02) 82. (2) Input signal b (horizontal 31.5 kHz) to pin 11 (HD3-IN). (3) Decreasing the duty of signal b to 0% (get negative period shorter), measure the duty of Signal b (HD-DUTY1) when the phase between pin 11 and pin 13 (HD1-OUT) change. (4) Increasing the duty of Signal b to 100% (get negative period longer), measure the duty of Signal b (HD-DUTY2) when the phase between pin 11 and pin 13 (HD1OUT) change.</p>  <p style="text-align: right;">* duty = A/(A + B) × 100 (%)</p> |

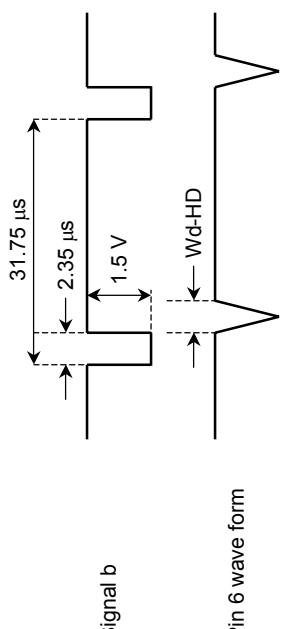
| Note | Item | SW Mode | | | | Test Conditions and Measuring Method (V _{CC} = 9 V, T _a = 25 ± 3°C, unless otherwise specified) |
|------|--|---------|-----|-------------|-------------|--|
| | | S06 | S18 | S19 | S21 | |
| HA04 | Sync1 input threshold amplitude Sync2 input threshold amplitude | c | b | a ↓ b | b ↓ a | <p>(1) Set sub-address (00) 0B and (02) 60.</p> <p>(2) Input Signal a (33.75 kHz) to pin 21 (SYNC1-IN). (V_{sync1})</p> <p>(3) Measure the sync. tip DC voltage of signal a on pin 21 (SYNC1-IN). (V_{sync1})</p> <p>(4) Supply external voltage via 100 kΩ to pin 21 and increase the voltage.</p> <p>(5) Measure the sync. tip DC voltage (V_{sync12}) when HD-OUT desynchronizes with signal a calculate V_{thS10}. V_{thS10} = V_{sync12} - V_{sync11}</p> <p>(6) Set sub-address (00) B1, B2 and B3 and calculate V_{thS11}, V_{thS12} and V_{thS13} as well.</p> <p>(7) Calculate V_{thS20}, V_{thS21}, V_{thS22} and V_{thS23} against pin 19 (SYNC2-IN) in the same way as 4 to 6.</p> |
| | | | | | |  <p style="text-align: center;">Signal a</p> |
| HA05 | HD3 input threshold amplitude (synchronization block) | c | b | — | — | <p>(1) Set sub-address (00) 70 and (02) 62.</p> <p>(2) Input Signal b (31.5 kHz) to pin 11 (HD3-IN).</p> <p>(3) Increasing the voltage of Signal b from 0 V, measure the voltage of Signal b V_{thHD3} when HD1-OUT lock.</p> |
| | | | | | |  <p style="text-align: center;">Signal b</p> |

| Note | Item | SW Mode | | | | Test Conditions and Measuring Method ($V_{CC} = 9\text{ V}$, $T_a = 25 \pm 3^\circ\text{C}$, unless otherwise specified) |
|------|---|---------|-----|-----|-----|--|
| | | S06 | S18 | S19 | S21 | |
| HA06 | HD1 input threshold voltage HD2 input threshold voltage HD3 input threshold voltage (SW block) | c | b | — | — | <p>(1) Set sub-address (00) 40. (2) Input Signal b (31.5 kHz) to pin 3 (HD1-IN). (3) Increasing the voltage of Signal b from 0 V, measure the voltage of Signal b V_{thHD1} when HD1-OUT lock. (4) Measure the voltage of pin 1 V_{thHD2}. Measure the voltage of pin 11 V_{thHD3} as well.</p>  <p style="text-align: center;">Signal b</p> |

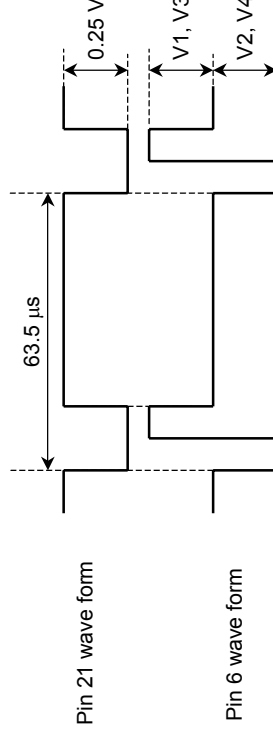
| Note | Item | SW Mode | | | | Test Conditions and Measuring Method ($V_{CC} = 9\text{ V}$, $T_a = 25 \pm 3^\circ\text{C}$, unless otherwise specified) |
|------|---|---------|-----|-----|-----|--|
| | | S06 | S18 | S19 | S21 | |
| HA07 | HD output phase adjustment variable range | c | b | — | — | <p>(1) Set sub-address (00) 30.</p> <p>(2) Input Signal b (horizontal period $T = 63.5\ \mu\text{s}$) to pin 11 (HD3-IN).</p> <p>(3) Set sub-address (02) 02.</p> <p>(4) Change form 00 to 7C sub-address (03), then measure the phase change quantity ($\Delta\text{HP0-}$) of pin 13 (HD1-OUT) wave form.</p> <p>(5) Change form 80 to FC sub-address (03), then measure the phase change quantity ($\Delta\text{HP0+}$) of pin 13 (HD1-OUT) wave form.</p> <p>(6) When horizontal period of Signal b is $T = 31.75\ \mu\text{s}$ measure $\Delta\text{HP1-}$ and $\Delta\text{HP1+}$ as well.</p> <p>(7) When horizontal period of Signal b is $T = 29.63\ \mu\text{s}$ measure $\Delta\text{HP2-}$ and $\Delta\text{HP2+}$ as well.</p> <p>(8) When horizontal period of Signal b is $T = 22.22\ \mu\text{s}$ measure $\Delta\text{HP3-}$ and $\Delta\text{HP3+}$ as well.</p> |



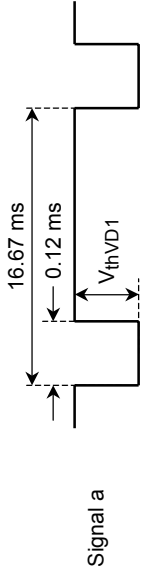
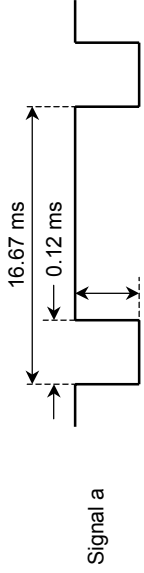
| Note | Item | SW Mode | | | | Test Conditions and Measuring Method ($V_{CC} = 9\text{ V}$, $T_a = 25 \pm 3^\circ\text{C}$, unless otherwise specified) |
|------|-------------------------------|---------|-----|-----|-----|--|
| | | S06 | S18 | S19 | S21 | |
| HA08 | Clamp pulse phase/width/level | c | b | — | — | <p>(1) Set sub-address (00) B0. (2) Input Signal a (horizontal 33.75 kHz) to pin 11 (HD3-IN). (3) Set sub-address (02) 02. (4) Measure the clamp pulse phase (CP_{S0}), width (CP_{W0}), output level (CP_{V0}) of pin 12 (CLP-OUT) against Signal a. (5) Set sub-address (02) 12. (6) Measure the clamp pulse phase (CP_{S1}), width (CP_{W1}), output level (CP_{V1}) of pin 12 (SCP-OUT) against Signal a. (7) Input no-signal to pin 11. (8) Measure the clamp pulse phase (CP_{S2}), width (CP_{W2}), output level (CP_{V2}) of pin 12 (SCP-OUT) against pin 13 (HD-OUT).</p> |

| Note | Item | SW Mode | | | | Test Conditions and Measuring Method (V _{CC} = 9 V, T _a = 25 ± 3°C, unless otherwise specified) |
|------|------------------------|---------|-----|-----|-----|---|
| | | S06 | S18 | S19 | S21 | |
| HA09 | Delayed HD pulse width | c | b | — | — | <p>(1) Set sub-address (00) 70. (2) Input Signal b (horizontal 31.5 kHz) to pin 11 (HD3-IN). (3) Set sub-address (02) 62. (4) Measure the pulse width (Wd-HD) of pin 6 (AFC filter) wave form.</p>  <p>The diagram consists of two waveforms. The top waveform, labeled 'Signal b', is a square wave. A horizontal double-headed arrow above it indicates a period of 31.75 μs. A shorter horizontal double-headed arrow above the pulse indicates a pulse width of 2.35 μs. A vertical double-headed arrow to the right of the pulse indicates a pulse height of 1.5 V. The bottom waveform, labeled 'Pin 6 wave form', shows a delayed HD pulse. A horizontal double-headed arrow below it indicates the pulse width, labeled 'Wd-HD'.</p> |

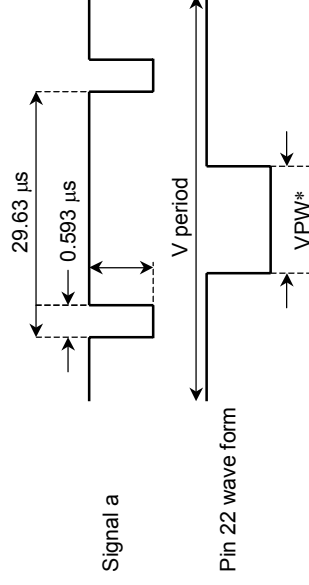
| Note | Item | SW Mode | | | | Test Conditions and Measuring Method (V _{CC} = 9 V, Ta = 25 ± 3°C, unless otherwise specified) |
|------|-------------------------------|---------|-----|-----|-----|--|
| | | S06 | S18 | S19 | S21 | |
| HB01 | AFC phase detection current | OPEN | b | a | b | <p>(1) BUS control data preset.</p> <p>(2) Horizontal oscillation frequency is 15.75 kHz (00).</p> <p>(3) SW6 open. Measure the Voltage of pin 6 V6 (no external supply).</p> <p>(4) Connect external supply with pin 6, and supply the voltage (V6).</p> <p>(5) Input signal (below figure) to pin 21 (SYNC1-IN). When INPUT SW is SYNC1-IN, measure V1 and V2 of pin 6 wave form.</p> <p>(6) Supply V6 – 0.1 V and V6 + 0.1 V to pin 6, then measure V3 and V4.</p> <p>(7) Calculate by following equations.</p> <p style="margin-left: 20px;">ID1 [μA] = (V1 [V] ÷ 1 [kΩ]) × 1000</p> <p style="margin-left: 20px;">ID2 [μA] = (V2 [V] ÷ 1 [kΩ]) × 1000</p> <p style="margin-left: 20px;">ID3 [μA] = (V3 [V] ÷ 1 [kΩ]) × 1000</p> <p style="margin-left: 20px;">ID4 [μA] = (V4 [V] ÷ 1 [kΩ]) × 1000</p> |
| HB02 | VCO oscillation start voltage | — | — | — | — | <p>(1) Increasing the voltage of pin 8 V_{CC} form 2.5V, measure the voltage V_{CO} when pin 7 appear oscillation wave form.</p> |



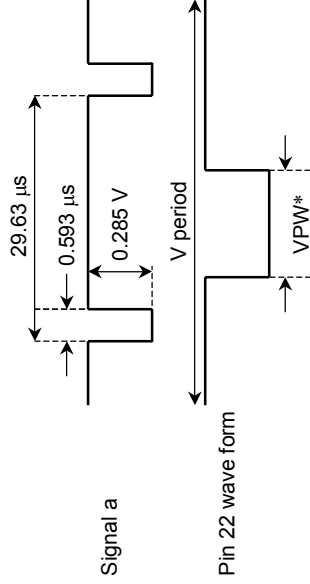
| Note | Item | SW Mode | | | | Test Conditions and Measuring Method (V _{CC} = 9 V, T _a = 25 ± 3°C, unless otherwise specified) |
|------|--|---------|-----|-----|-----|---|
| | | S06 | S18 | S19 | S21 | |
| HB03 | HD output pulse width (free-run) | c | b | — | — | <p>(1) BUS control data preset.</p> <p>(2) When horizontal oscillation frequency is 15.75 kHz (00), measure the output pulse width TH00 of pin 13 (HD1-OUT) wave form.</p> <p>(3) When horizontal oscillation frequency is 31.5 kHz (01), 33.75 kHz (10), 45 kHz (11), measure the output pulse width TH01, TH02, TH03 as well.</p> |
| | | | | | | <p style="text-align: center;">Pin 13 (HD1OUT) wave form</p> |
| HB04 | Horizontal free-run frequency | OPEN | b | — | — | <p>(1) BUS control data preset.</p> <p>(2) SW6 open. When horizontal oscillation frequency is 15.75 kHz (00), measure the oscillation frequency F00 of pin 13 (HD1-OUT) wave form.</p> <p>(3) When horizontal oscillation frequency is 31.5 kHz (01), 33.75 kHz (10), 45 kHz (11), measure the oscillation frequency F01, F10, F11 as well.</p> <p>(4) When horizontal oscillation frequency is 15.75 kHz (00) and vertical free-run frequency is (101), measure the oscillation frequency F50 of pin 15 wave form.</p> |
| HB05 | Horizontal oscillation control sensitivity | OPEN | b | — | — | <p>(1) BUS control data preset.</p> <p>(2) SW6 open.</p> <p>(3) Connect external voltage with pin 6. Horizontal oscillation frequency is 15.75 kHz (00). Supply V6 (about 6.3 V) + 0.05 V or V6 – 0.05 V to pin 6, then measure the frequency FA, FB of pin 13 (HD1-OUT) wave form. Calculate frequency changing ratio (BH00). BH00 = (FB – FA)/0.1</p> <p>(4) When horizontal oscillation frequency is 31.5 kHz (01), 33.75 kHz (10), 45 kHz (11), calculate BH01, BH10, BH11 as well.</p> |

| Note | Item | SW Mode | | | | Test Conditions and Measuring Method ($V_{CC} = 9\text{ V}$, $T_a = 25 \pm 3^\circ\text{C}$, unless otherwise specified) |
|------|---|---------|-----|-----|-----|---|
| | | S06 | S18 | S19 | S21 | |
| VA01 | VD1 input threshold voltage VD2 input threshold voltage VD3 input threshold voltage (SW block) | c | b | — | — | <p>(1) Set sub-address (00) 80. (2) Input Signal a (vertical 60 Hz) to pin 4 (VD1-IN). (3) Set sub-address (02) 00. (4) Increasing the voltage of Signal a from 0 V, measure the voltage of Signal b V_{thVD1} when VD1-OUT lock. (5) Measure V_{thVD2} and V_{thVD3} against pin 2 and pin 10 as well.</p>  <p style="text-align: center;">Signal a</p> |
| VA02 | VD3 input threshold voltage (synchronization block) | c | b | — | — | <p>(1) Set sub-address (00) 70. (2) Input Signal b (vertical 60 Hz) to pin 10 (VD3-IN). (3) Set sub-address (02) 03. (4) Increasing the voltage of Signal b from 0 V, measure the voltage of Signal a V_{thVD3} when VD1-OUT lock.</p>  <p style="text-align: center;">Signal a</p> |

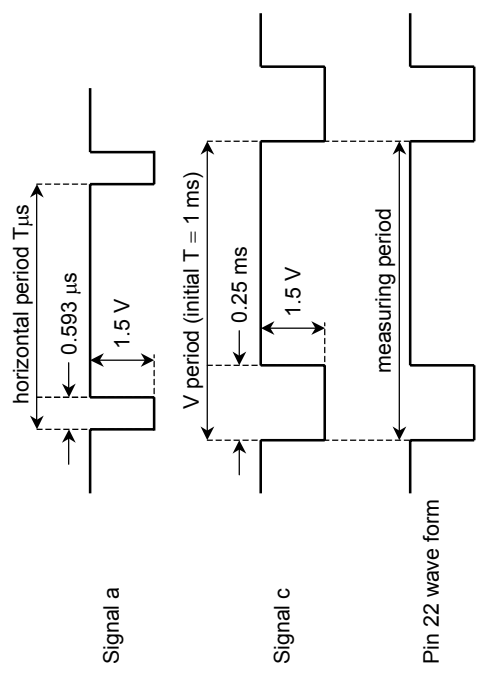
| Note | Item | SW Mode | | | | Test Conditions and Measuring Method (V _{CC} = 9 V, T _a = 25 ± 3°C, unless otherwise specified) |
|------|-----------------------------|---------|-----|-----|-----|--|
| | | S06 | S18 | S19 | S21 | |
| VA03 | Vertical output pulse width | c | b | — | — | <p>(1) Input Signal a (horizontal 33.75 kHz) to pin 11 (HD3-IN).</p> <p>(2) Set sub-address (02) 02.</p> <p>(3) When sub-address (00) is B0, measure the pulse width VPW2 of pin 22 (VD1-OUT) wave form.</p> <p>(4) When sub-address (00) is 30, 70, F0, measure the pulse width VPW0, VPW1, VPW3 of pin 22 (VD1-OUT) wave form as well.</p> |



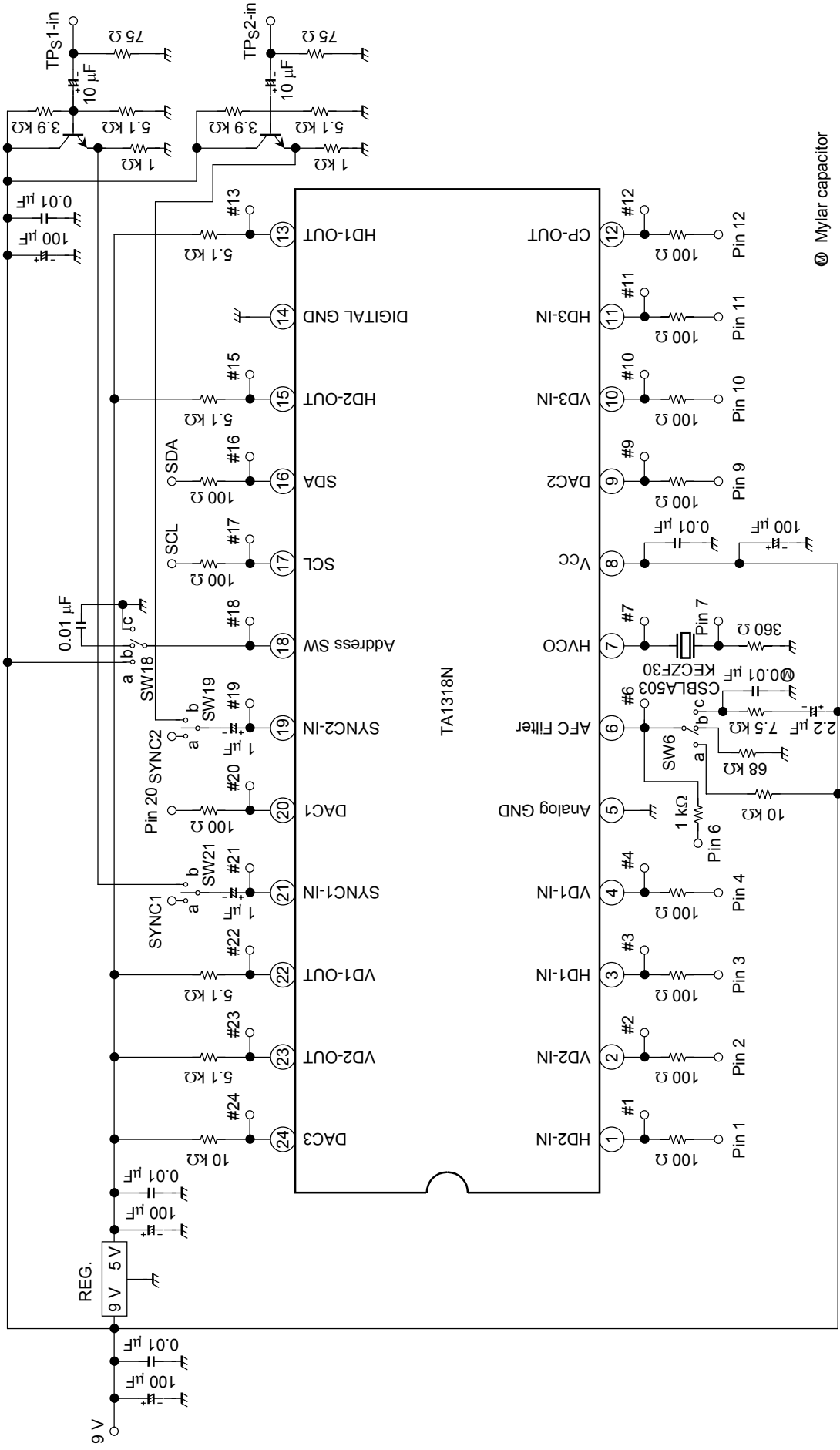
| Note | Item | SW Mode | | | | Test Conditions and Measuring Method ($V_{CC} = 9\text{ V}$, $T_a = 25 \pm 3^\circ\text{C}$, unless otherwise specified) |
|------|-----------------------------|---------|-----|-----|-----|--|
| | | S06 | S18 | S19 | S21 | |
| VA04 | Vertical free-run frequency | c | b | — | — | <p>(1) Input Signal a (horizontal 33.75 kHz) to pin 11 (HD3-IN).</p> <p>(2) Set sub-address (00) B0.</p> <p>(3) When sub-address (02) is 02, 22, 62, 82, A2 or C2, measure the frequency FV0, FV1, FV3, FV4, FV5 or FV6 of pin 22 (VD1-OUT) wave form.</p> <p>(4) Input no-signal to pin 3 (HD1-IN).</p> <p>(5) Set sub-address (02) 42.</p> <p>(6) When sub-address (00) is 30, 70, B0 or F0, measure the frequency FV20, FV21, FV22 or FV23 of pin 22 (VD1-OUT) wave form.</p> |



| Note | Item | SW Mode | | | | Test Conditions and Measuring Method (V _{CC} = 9 V, T _a = 25 ± 3°C, unless otherwise specified) |
|------|------------------------|---------|-----|-----|-----|---|
| | | S06 | S18 | S19 | S21 | |
| VA05 | Vertical pull-in range | c | b | — | — | <p>(1) Input Signal a (horizontal period T = 63.5 μs) to pin 11 (HD3-IN). (2) Set sub-address (02) 02. (3) Set sub-address (00) 30. (4) Input Signal C (vertical period initial T = 1ms) to pin 10 (VD3-IN). Increasing vertical period of Signal C, measure the frequency FVPL0 when pin 22 (VD1-OUT) wave form synchronize with Signal C. (5) Input Signal a (horizontal period T = 31.75 μs) to pin 11 (HD3-IN). (6) Set sub-address (00) 70. (7) Measure FVPL1 as well. (8) Input Signal a (horizontal period T = 29.63 μs) to pin 11 (HD3-IN). (9) Set sub-address (00) B0. (10) Measure FVPL2 as well. (11) Input Signal a (horizontal period T = 22.22 μs) to pin 11 (HD3-IN). (12) Set sub-address (00) F0. (13) Measure FVPL3 as well.</p> |

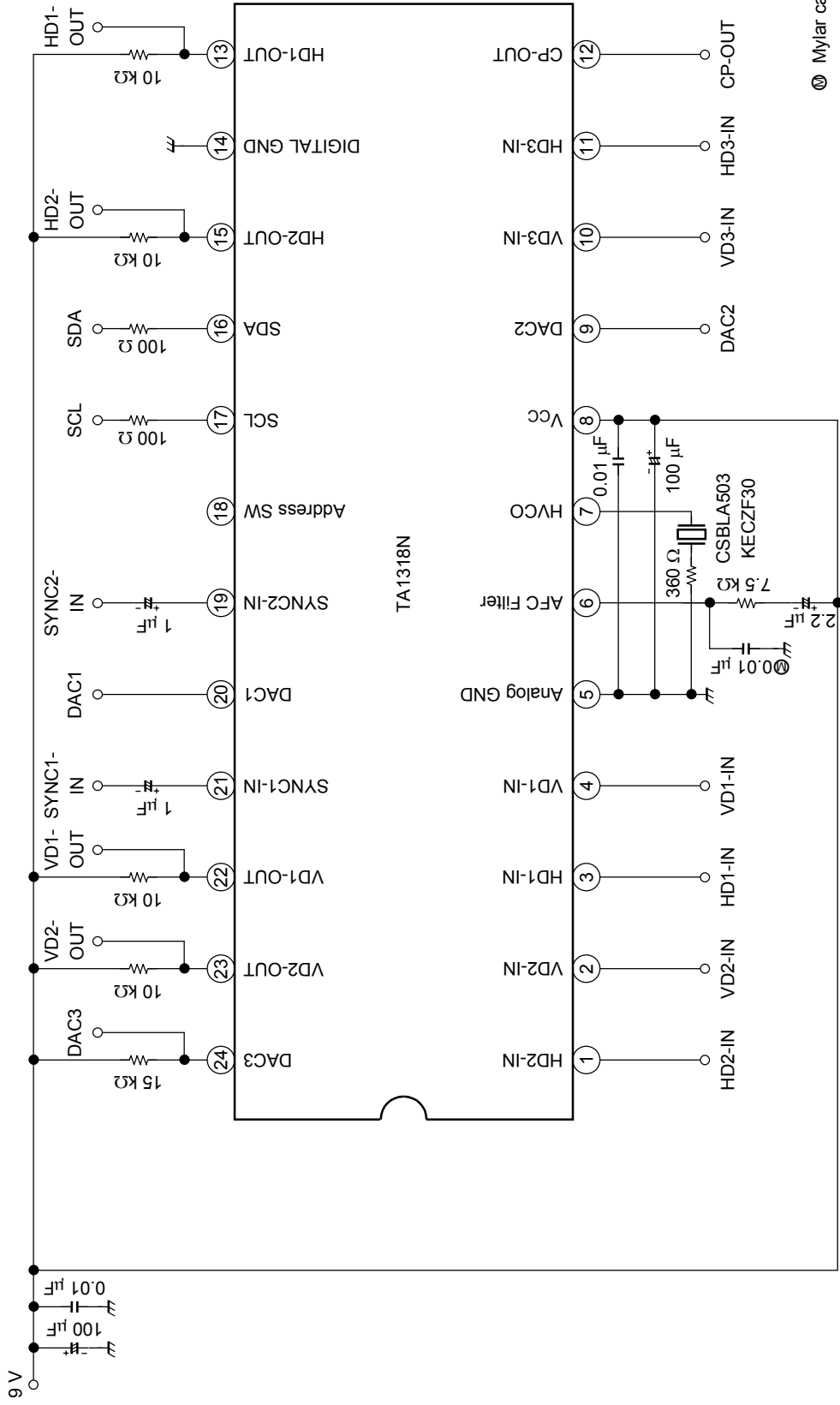


Test Circuit



⊗ Mylar capacitor

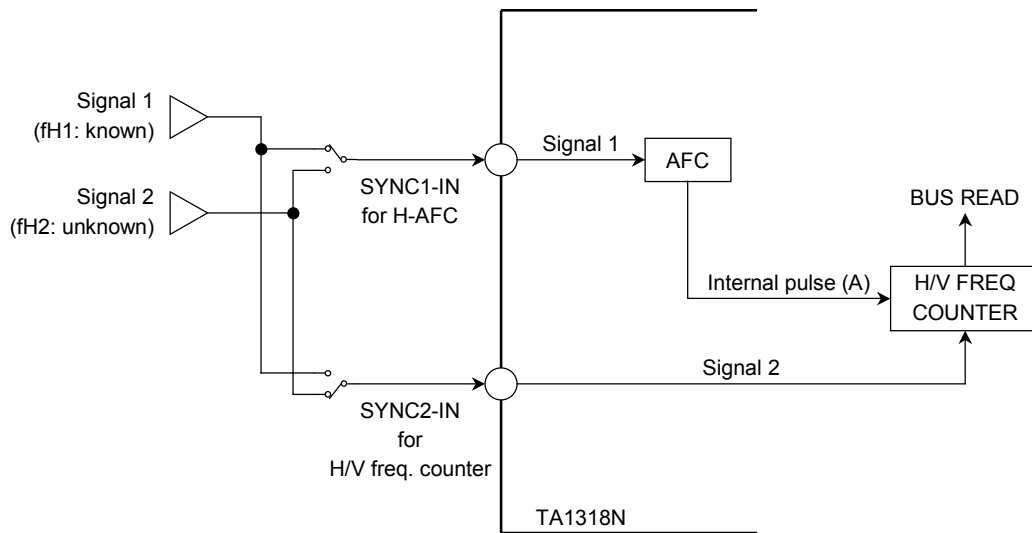
Application Circuit 1 (Typical values)



Ⓜ Mylar capacitor

Application Circuit 2 (How to measure H/V frequency)

To measure H/V frequency of signal 2 (f_{H2} : unknown) correctly, use two separated input terminals as the following figure. One is for frequency measuring (SYNC2-in) and the other is for the AFC (SYNC1-IN). And measure H/V frequency of signal 2 (f_{H2} : unknown) on condition that AFC is stable (AFC locks in signal 1 (f_{H1} : known).) or that AFC is free-run when SYNC1-IN is no-signal.



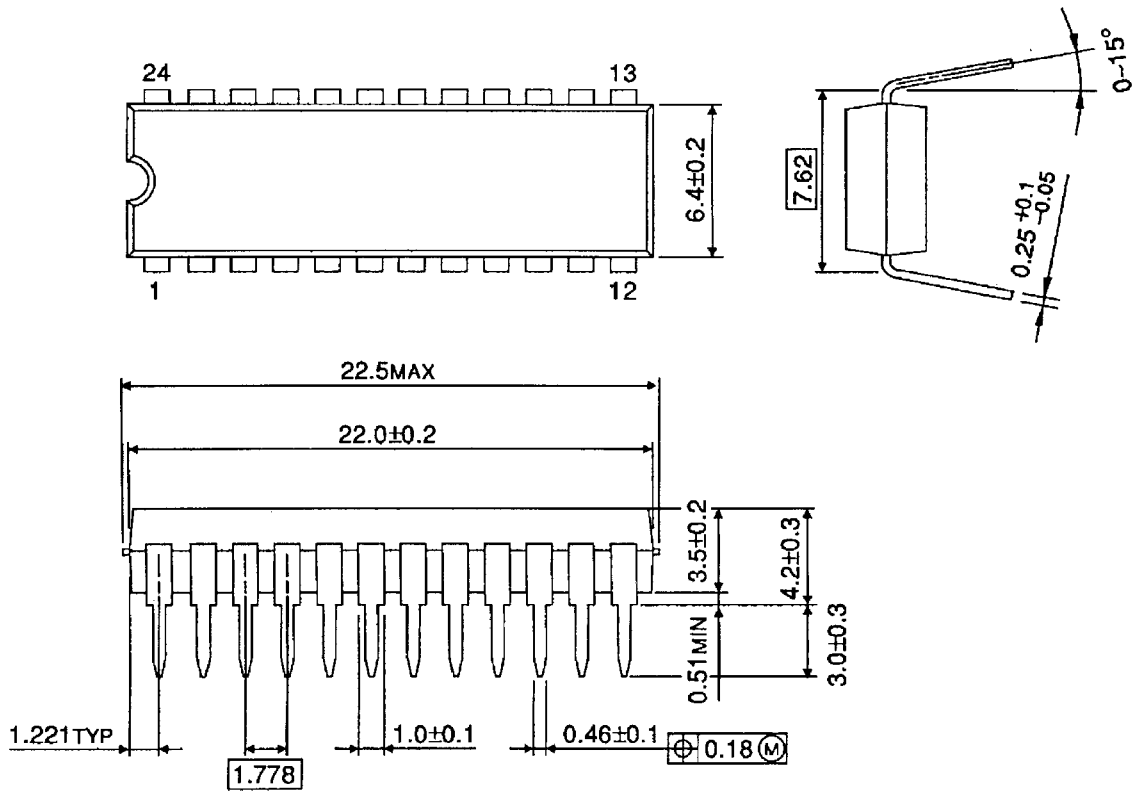
This IC's H/V frequency counting is done by internal pulse (A) which is made in AFC circuit. So, if AFC circuit doesn't lock in the regular frequency, the frequency of pulse (A) will not be correct and the H/V frequency data will not be showed correct data.

Decision algorithm of H/V frequency detection (detection range, detection times and so on) should be determined under consideration the factors such as signal strength, existence of ghost signal, H-AFC stability, I²C BUS data transmission and so on via prototype TV set evaluation.

Package Dimensions

SDIP24-P-300-1.78

Unit : mm



Weight: 1.22 g (typ.)

RESTRICTIONS ON PRODUCT USE

000707EBA

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's own risk.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.