TRIPATH

TA2021B

STEREO 25W (4Ω) CLASS-T™ DIGITAL AUDIO AMPLIFIER DRIVER USING DIGITAL POWER PROCESSING (DPP™) TECHNOLOGY

Technical Information Revision 4.0 – July 2003

General Description

The TA2021B is a 25W (4Ω) continuous average per channel Class-T Digital Audio Power Amplifier IC using Tripath's proprietary Digital Power Processing (DPP™) technology. Class-T amplifiers offer both the audio fidelity of Class-AB and the power efficiency of Class-D amplifiers.

Applications

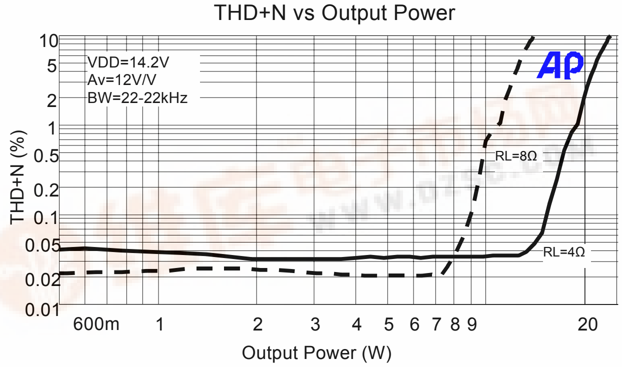
- DVD Receivers
- Mini/Micro Component Systems
- Computer / PC Multimedia
- Cable Set-Top Products
- Televisions
- Battery Powered Systems

Benefits

- Fully integrated solution with internal FETs
- Easier to design-in than Class-D
- Dramatically improves efficiency versus Class-AB amplifiers
- Signal fidelity equal to high quality linear amplifiers
- High dynamic range compatible with digital media such as CD and DVD, and internet audio

Typical Performance

THD+N vs Output Power



Features

- Class-T architecture
- Single Supply Operation
- "Audiophile" Quality Sound
  - 0.05% THD+N @ 13W 4Ω
  - 0.1% THD+N @15.5W 4Ω
  - 0.1% IHF-IM @ 1W 4Ω
- High Power
  - 25W @ 4Ω, 10% THD+N, V_{DD}=14.6V
  - 23.5W @ 4Ω, 10% THD+N, V_{DD}=14.2V
  - 14W @ 8Ω, 10% THD+N, V_{DD}=14.2V
- High Efficiency
  - 88% @ 13.5W 8Ω
  - 81% @ 25W 4Ω
- Dynamic Range = 100 dB
- Mute and Sleep inputs
- Turn-on & turn-off pop suppression
- Over-current protection
- Over-temperature protection
- Bridged outputs
- 36-pin PSOP "Slug-Up" package

Absolute maximum ratings (Note 1)

SYMBOL	PARAMETER	Value	UNITS
V_{DD}	Supply Voltage	16	V
V5	Input Section Supply Voltage	6.0	V
SLEEP	SLEEP Input Voltage	-0.3 to 6.0	V
MUTE	MUTE Input Voltage	-0.3 to V5+0.3	V
T_{STORE}	Storage Temperature Range	-40 to 150	°C
T_A	Operating Free-air Temperature Range	-40 to 85	°C
T_J	Junction Temperature	150	°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. See the table below for Operating Conditions.
Note 2: Human body model, 100pF discharged through a 1.5KΩ resistor.
Note 3: Machine model, 220pF discharged through all pins.

Operating Conditions (Note 4)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{DD}	Supply Voltage	8.5	14.2	14.6	V
V_{IH}	High-level Input Voltage (MUTE, SLEEP)	3.5			V
V_{IL}	Low-level Input Voltage (MUTE, SLEEP)			1	V

Note 4: Recommended Operating Conditions indicate conditions for which the device is functional. See Electrical Characteristics for guaranteed specific performance limits.

Thermal Characteristics

SYMBOL	PARAMETER	VALUE	UNITS
θ_{JC}	Junction-to-case Thermal Resistance	2.5	°C/W
θ_{JA}	Junction-to-ambient Thermal Resistance (still air)	50	°C/W

Electrical Characteristics (Notes 6, 7)

See Test/Application Circuit. Unless otherwise specified, V_{DD} = 14.2V, f = 1kHz, Measurement Bandwidth = 22kHz, R_L = 4Ω, T_A = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
P_O	Output Power (Continuous Average/Channel)	THD+N = 0.1% R_L = 4Ω R_L = 8Ω THD+N = 10% R_L = 4Ω R_L = 8Ω		15.5 9 23.5 14		W W W W
P_O	Output Power (V_{DD}=14.6V) (Continuous Average/Channel)	THD+N = 0.1% R_L = 4Ω R_L = 8Ω THD+N = 10% R_L = 4Ω R_L = 8Ω		16.5 9.5 25 14.8		W W W W
$I_{DD,MUTE}$	Mute Supply Current	MUTE = V_{IH}		5.5	7	mA
$I_{DD, SLEEP}$	Sleep Supply Current	SLEEP = V_{IH}		0.25	2	mA
I_q	Quiescent Current	V_{IN} = 0 V		64	75	mA
THD + N	Total Harmonic Distortion Plus Noise	P_O = 10W/Channel		0.035		%
IHF-IM	IHF Intermodulation Distortion	19kHz, 20kHz, 1:1 (IHF)		0.1	0.3	%
SNR	Signal-to-Noise Ratio	A-Weighted, P_{OUT} = 25W, R_L = 4Ω		100		dB
CS	Channel Separation	0dBr = 1W, R_L = 4Ω, f = 1 kHz	74	80		dB
PSRR	Power Supply Rejection Ratio	Vripple = 100mV	60	80		dB
η	Power Efficiency	P_{OUT} = 13.5W/Channel, R_L = 8Ω		88		%
V_{OFFSET}	Output Offset Voltage	No Load, MUTE = Logic low		50	150	mV
V_{OH}	High-level output voltage (FAULT & OVERLOADB)		3.5			V
V_{OL}	Low-level output voltage (FAULT & OVERLOADB)				1	V
e_{OUT}	Output Noise Voltage	A-Weighted, input AC grounded		100		μV

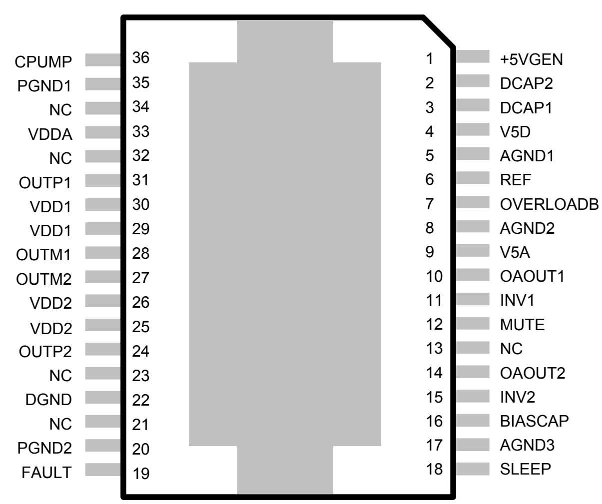
Note 6: Minimum and maximum limits are guaranteed but may not be 100% tested.
Note 7: For operation in ambient temperatures greater than 25°C, the device must be de-rated based on the maximum junction temperature and the thermal resistance determined by the mounting technique.

Pin Description

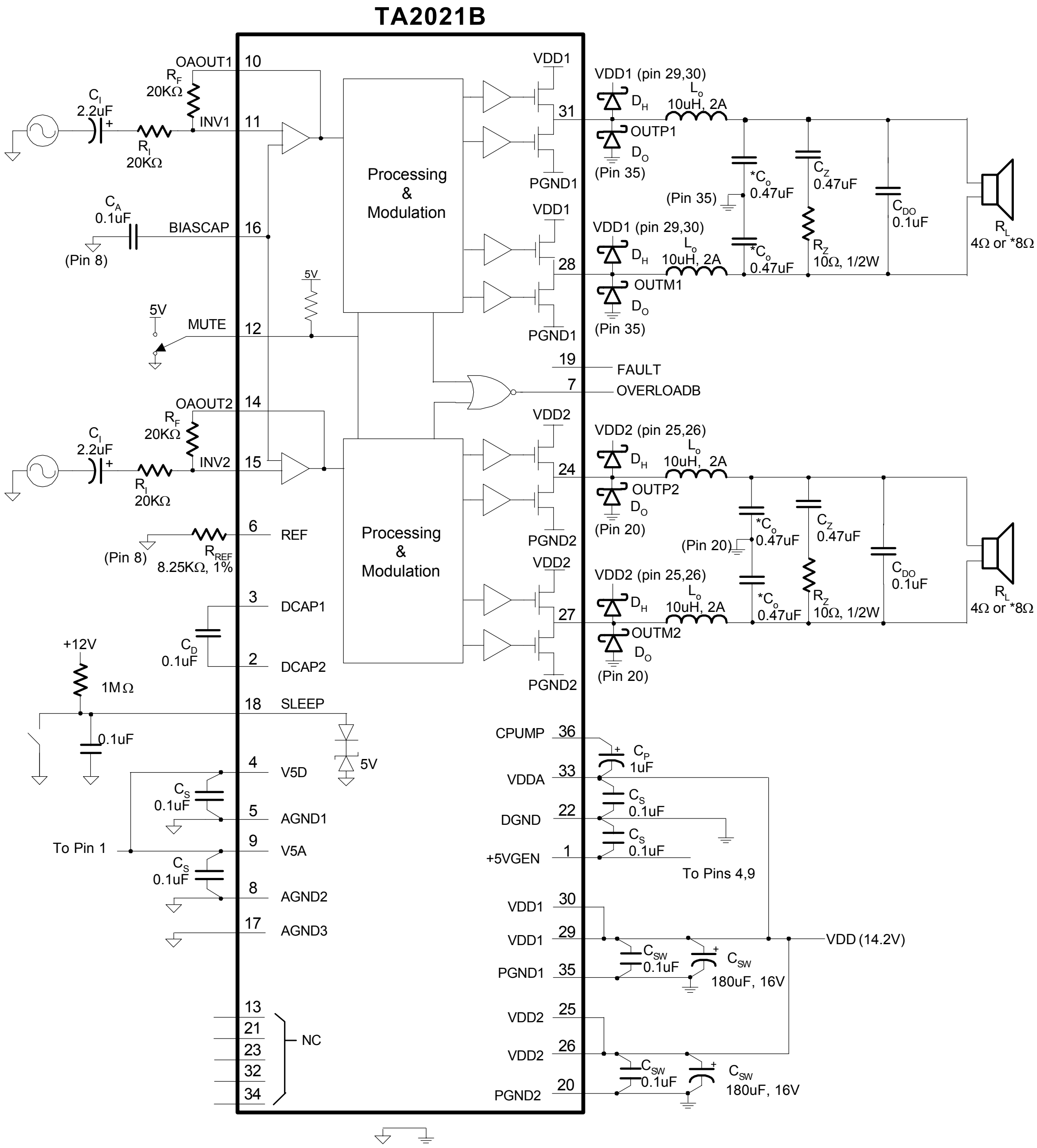
Pin	Function	Description
2, 3	DCAP2, DCAP1	Charge pump switching pins. DCAP1 (pin 3) is a free running 300kHz square wave between VDDA and DGND (12Vpp nominal). DCAP2 (pin 2) is level shifted 10 volts above DCAP1 (pin 3) with the same amplitude (12Vpp nominal), frequency, and phase as DCAP1.
4, 9	V5D, V5A	Digital 5VDC, Analog 5VDC
5, 8, 17	AGND1, AGND2, AGND3	Analog Ground
6	REF	Internal reference voltage; approximately 1.0 VDC.
7	OVERLOADB	A logic low output indicates the input signal has overloaded the amplifier.
10, 14	OAOUT1, OAOUT2	Input stage output pins.
11, 15	INV1, INV2	Single-ended inputs. Inputs are a “virtual” ground of an inverting op-amp with approximately 2.4VDC bias.
12	MUTE	When set to logic high, both amplifiers are muted and in idle mode. When low (grounded), both amplifiers are fully operational. If left floating, the device stays in the mute mode. This pin should be tied to GND if not used.
16	BIASCAP	Input stage bias voltage (approximately 2.4VDC).
18	SLEEP	When set to logic high, device goes into low power mode. If not used, this pin should be grounded
19	FAULT	A logic high output indicates thermal overload, or an output is shorted to ground, or another output.
20, 35	PGND2, PGND1	Power Grounds (high current)
22	DGND	Digital Ground
24, 27; 31, 28	OUTP2 & OUTM2; OUTP1 & OUTM1	Bridged outputs
25, 26, 29, 30	VDD2, VDD2 VDD1, VDD1	Supply pins for high current H-bridges.
13, 21, 23, 32, 34	NC	Not connected. Not bonded internally.
33	VDDA	Supply pin for analog section.
36	CPUMP	Charge pump output (nominally 10V above VDDA)
1	5VGEN	Regulated 5VDC source used to supply power to the input section (pins 4 and 9).

TA2021B Pinout

36-pin Slug-Up SOP Package
(Top View)



Application / Test Circuit



Note: Analog and Digital/Power Grounds must be connected locally at the TA2021

Analog Ground

Digital/Power Ground

All Diodes Motorola MBRS130T3

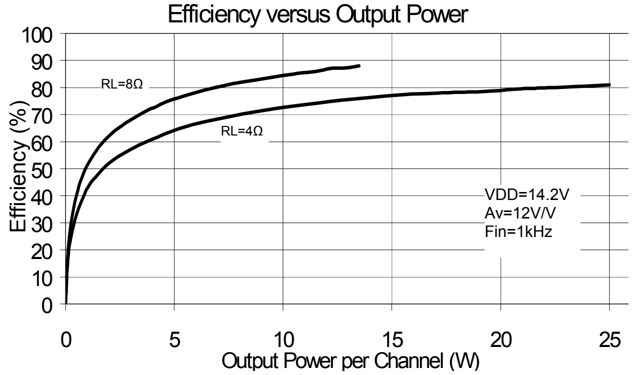
* Use C_o = 0.22μF and Cz = 0.22μF for 8 Ohm loads

External Components Description (Refer to the Application/Test Circuit)

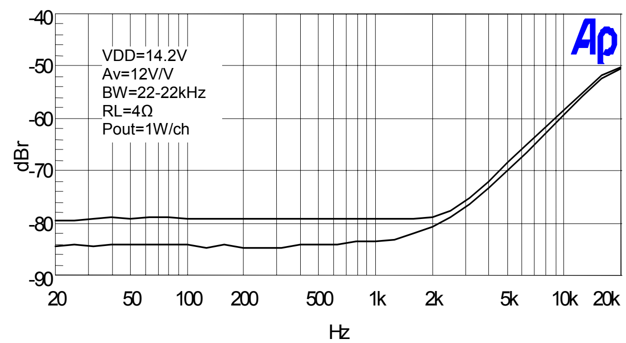
Components	Description
R_I	Inverting Input Resistance to provide AC gain in conjunction with R_F. This input is biased at the BIASCAP voltage (approximately 2.4VDC).
R_F	Feedback resistor to set AC gain in conjunction with R_I; $A_V = 12(R_F / R_I)$. Please refer to the Amplifier Gain paragraph in the Application Information section.
C_I	AC input coupling capacitor which, in conjunction with R_I, forms a highpass filter at $f_C = 1/(2\pi R_I C_I)$
R_{REF}	Bias resistor. Locate close to pin 6 and ground at pin 8.
C_A	BIASCAP decoupling capacitor. Should be located close to pin 16.
C_D	Charge pump input capacitor. This capacitor should be connected directly between pins 2 and 3 and located physically close to the TA2028.
C_P	Charge pump output capacitor that enables efficient high side gate drive for the internal H-bridges. To maximize performance, this capacitor should be connected directly between pin 36 (CPUMP) and pin 34 (VDDA). Please observe the polarity shown in the Application/ Test Circuit.
C_S	Supply decoupling for the low current power supply pins. For optimum performance, these components should be located close to the pin and returned to their respective ground as shown in the Application/Test Circuit.
C_{SW}	Supply decoupling for the high current, high frequency H-Bridge supply pins. These components must be located as close to the device as possible to minimize supply overshoot and maximize device reliability. Both the high frequency bypassing (0.1uF) and bulk capacitor (180uF) should have good high frequency performance including low ESR and low ESL. Panasonic HFQ or FC capacitors are ideal for the bulk capacitor.
C_Z	Zobel Capacitor.
R_Z	Zobel resistor, which in conjunction with C_Z, terminates the output filter at high frequencies. The combination of R_Z and C_Z minimizes peaking of the output filter under both no load conditions or with real world loads, including loudspeakers which usually exhibit a rising impedance with frequency.
D_O	Schottky diodes that minimize undershoots of the outputs with respect to power ground during switching transitions. For maximum effectiveness, these diodes must be located close to the output pins and returned to their respective PGND. Please see Application/Test Circuit for ground return pin.
D_H	Schottky diodes that minimize overshoots of the outputs with respect to V_{DD} during switching transitions (required for applications where V_{DD} >13.5V). For maximum effectiveness, these diodes must be located close to the output pins and returned to their respective V_{DD} pins. Please see Application/Test Circuit for V_{DD} return pin.
L_O	Output inductor, which in conjunction with C_O, demodulates (filters) the switching waveform into an audio signal. Forms a second order filter with a cutoff frequency of $f_C = 1/(2\pi\sqrt{L_O C_O})$ and a quality factor of $Q = R_L C_O / \sqrt{L_O C_O}$.
C_O	Output capacitor.
C_{DO}	Differential Output Capacitor.

Typical Performance

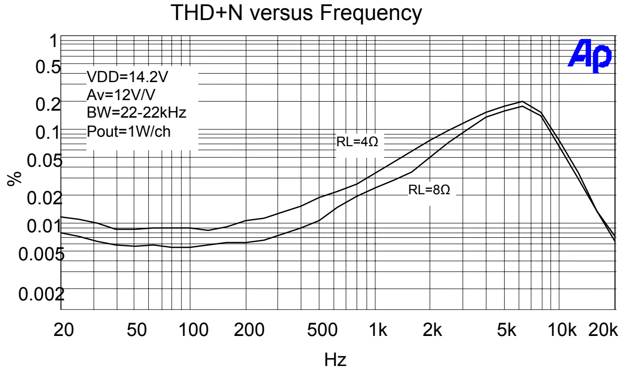
Efficiency versus Output Power



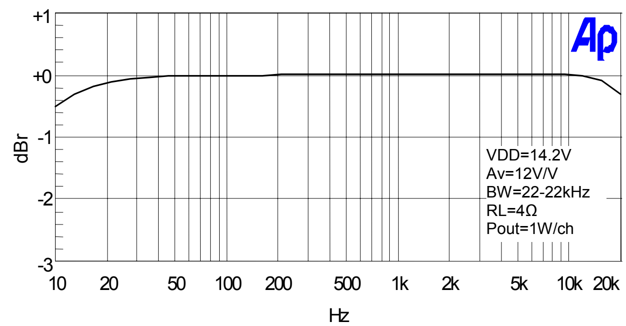
Channel Separation versus Frequency



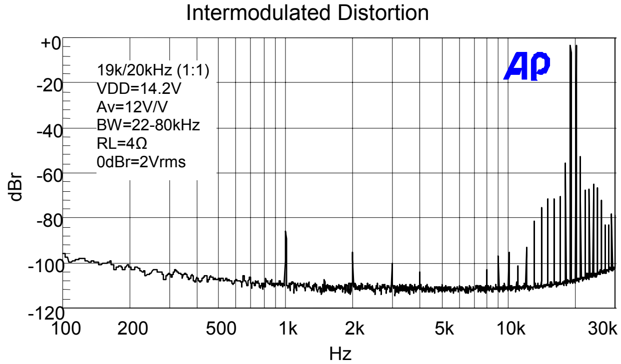
THD+N versus Frequency



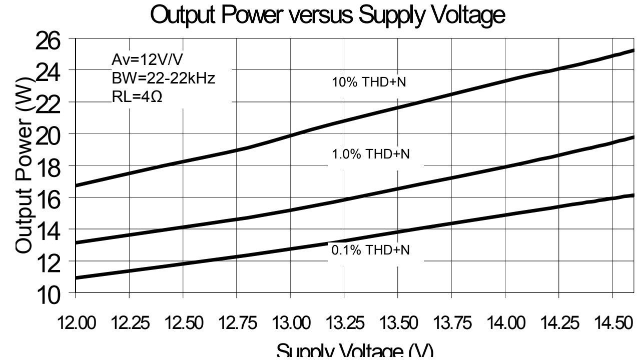
Frequency Response



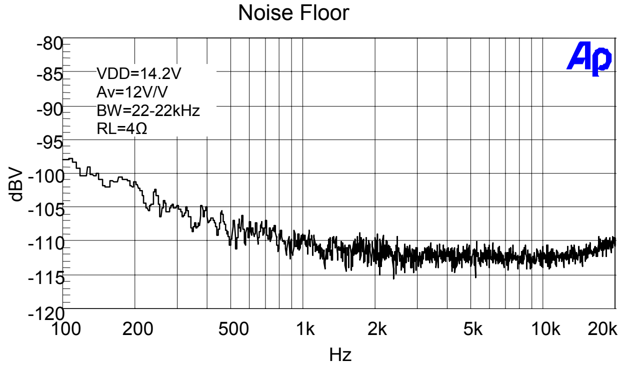
Intermodulated Distortion



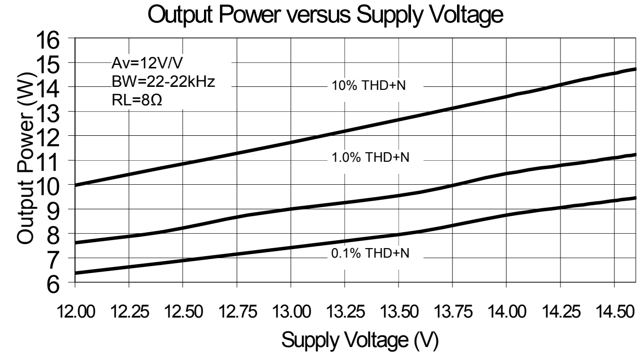
Output Power versus Supply Voltage



Noise Floor



Output Power versus Supply Voltage



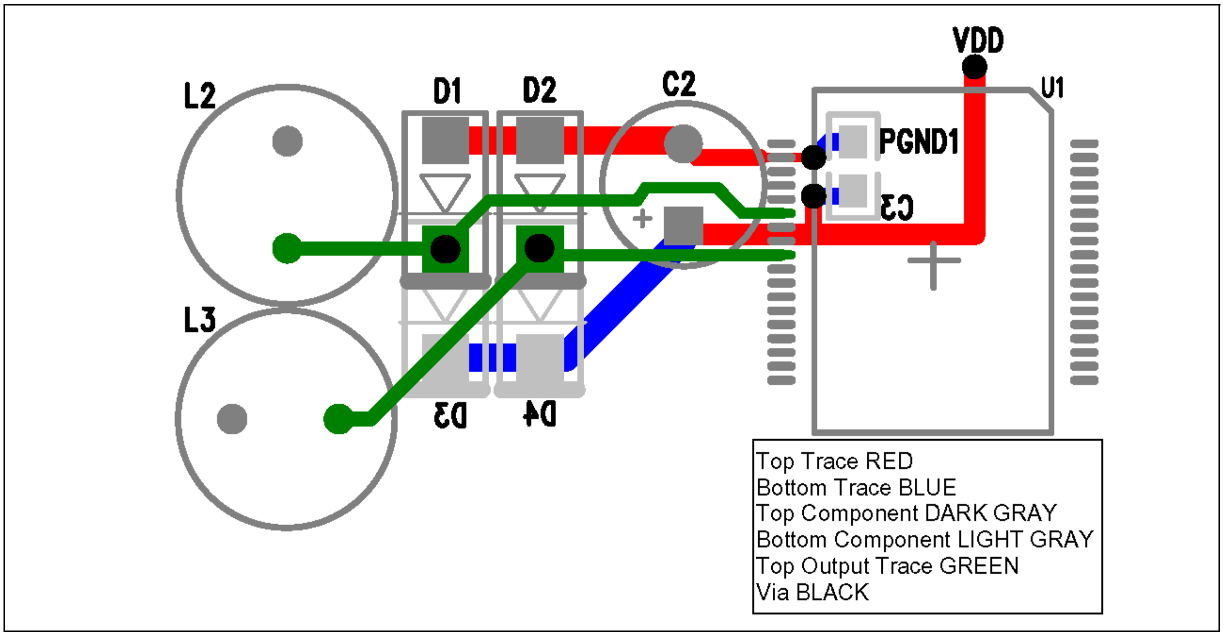
Application Information

Circuit Board Layout

The TA2021B is a power amplifier which operates at relatively high switching frequencies. The outputs of the amplifier switch between VDD and PGND at frequencies as high as 1MHz while driving high currents. This high-frequency digital signal is passed through an LC low-pass filter to recover the amplified audio signal. Because the TA2021B drives the inductive LC output filters and speaker load, the amplifier outputs can be pulled above VDD and below PGND by the stored energy in the output inductance. To avoid subjecting the TA2021B to potentially damaging voltage stress, it is critical to have a good printed circuit board layout to minimize parasitic effects caused by excessive trace inductance/capacitance. It is recommended that Tripath's layout and application circuit be used as closely as possible for all applications and only be deviated from after careful analysis of the effects of any changes.

Output Stage layout Considerations and Component Selection Criteria

Proper PCB layout and component selection is a major step in designing a reliable TA2021B power amplifier. The supply pins require proper decoupling with correctly chosen components to achieve optimal reliability. The output pins need proper protection to keep the outputs from going below ground and above VDD.



The above layout shows component placement and routing for channel 1 (the same design criteria applies to channel 2). This shows that C3, a 0.1uF surface mount 0805 capacitor, should be the first component placed and must decouple VDD1 (pins 29 and 30) directly to PGND1 (pin35). C2, a low ESR, electrolytic capacitor, should also decouple VDD1 directly to PGND1. Both C2 and C3 may decouple VDD1 to a ground plane, but it is critical that the return path to the PGND1 pin of the TA2021B, whether it is a ground plane or a trace, be a short and direct low impedance path. Effectively decoupling VDD will shunt any power supply trace length inductance.

The diodes and inductors shown are for channel 1's outputs. D1, D3, and L2 connect to the OUTP1 pin and D2, D4, and L3 connect to the OUTM1 pin of the TA2021B. Each output must have Schottky or Ultra Fast Recovery diodes placed near the TA2021B, preferably immediately after the decoupling capacitors and use short returns to PGND1. These low side diodes, D1 and D2, will prevent the outputs from going below ground. To be optimally effective they must have a short and direct return path to its proper ground pin (PGND1) of the TA2021B. This can be achieved with a ground plane or a trace. Additionally, each channel must use Schottky or Ultra Fast Recovery diodes with short returns to VDD if the supply voltage exceeds 13.5V. These high side diodes, D3 and D4, will prevent the outputs from going above VDD. To be optimally effective they must have a short and direct return path to its proper VDD pin (VDD1) of the TA2021B. This can be achieved with a ground plane or a trace.

The output inductors, L2 and L3, should be placed close to the TA2021B without compromising the locations of the closely placed supply decoupling capacitors and output diodes. The purpose of placing the output inductors close to the TA2021B output pins is to reduce the trace length of the switching outputs. This will aid in reducing radiated emissions.

Please see the External Component Description section on page 6 for more details on the above-mentioned components. The Application/ Test Circuit refers to the low side diodes as D_O, The high side diodes as D_H, and both supply decoupling capacitors as C_{SW}.

TA2021B Amplifier Gain

The gain of the TA2021B is set by the ratio of two external resistors, R_I and R_F, and is given by the following formula:

$$\frac{V_O}{V_I} = -12\frac{R_F}{R_I}$$

where V_I is the input signal level and V_O is the differential output signal level across the speaker. Please note that OUTP1 and OUTP2 are 180° out of phase with their corresponding input signals.

20 watts of RMS output power results from an 8.944 Vrms signal across a four-ohm speaker load. If $R_F = R_I$, then 20 Watts will be achieved with 0.745 Vrms of input signal.

$$8.944\,V_{RMS} = \sqrt{(R_L * P_O)} = \sqrt{(4\Omega * 20W)}$$

Protection Circuits

The TA2021B is guarded against over-temperature and over-current conditions. When the device goes into an over-temperature or over-current state, the FAULT pin goes to a logic HIGH state indicating a fault condition. When this occurs, the amplifier is muted, all outputs are TRI-STATED, and will float to 1/2 of VDD.

Over-temperature Protection

An over-temperature fault occurs if the junction temperature of the part exceeds approximately 155°C. The thermal hysteresis of the part is approximately 45°C, therefore the fault will automatically clear when the junction temperature drops below 110°C.

Over-current Protection

An over-current fault occurs if more than approximately 7 amps of current flows from any of the amplifier output pins. This can occur if the speaker wires are shorted together or if one side of the speaker is shorted to ground. An over-current fault sets an internal latch that can only be cleared if the MUTE pin is toggled or if the part is powered down. Alternately, if the MUTE pin is connected to the FAULT pin, the HIGH output of the FAULT pin will toggle the MUTE pin and automatically reset the fault condition.

Overload (Output Active Low)

The OVERLOADB pin is a 5V logic active-low output. When low, it indicates that the level of the input signal has overloaded the amplifier resulting in increased distortion at the output. The OVERLOADB signal can be used to control a distortion indicator light or LED through a simple buffer circuit.

Sleep Pin (Input Active High)

The SLEEP pin is a 5V logic input that, when pulled high (>3.5V), puts the part into a low quiescent current mode. This pin is internally clamped by a zener diode to approximately 6V thus allowing the pin to be pulled up through a large valued resistor (1MΩ recommended, 100KΩ minimum) to VDD. To disable SLEEP mode, the sleep pin should be grounded.

Fault Pin (Output Active High)

The FAULT pin is a 5V logic output that indicates various fault conditions within the device. These conditions include: low supply voltage, low charge pump voltage, low 5V regulator voltage, over current at any output, and junction temperature greater than approximately 155°C. The FAULT output is capable of directly driving an LED through a series 2KΩ resistor. If the FAULT pin is connected directly to the MUTE input an automatic reset will occur in the event of an over-current condition.

Performance Measurements of the TA2021B

The TA2021B operates by generating a high frequency switching signal based on the audio input. This signal is sent through an external low-pass filter that recovers an amplified version of the audio input. The frequency of the switching pattern is spread spectrum in nature and typically varies between 100kHz and 1MHz (which is well above the 20Hz – 20kHz audio band). The pattern itself does not alter or distort the audio input signal, but it does introduce some inaudible components.

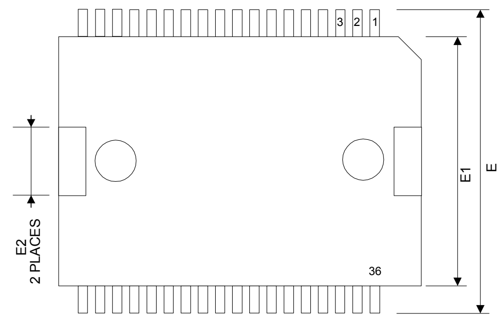
The measurements of certain performance parameters, particularly noise related specifications such as THD+N, are significantly affected by the design of the low-pass filter used on the output as well as the bandwidth setting of the measurement instrument used. Unless the filter has a very sharp roll-off just beyond the audio band or the bandwidth of the measurement instrument is limited, some of the inaudible noise components introduced by the TA2021B amplifier switching pattern will degrade the measurement.

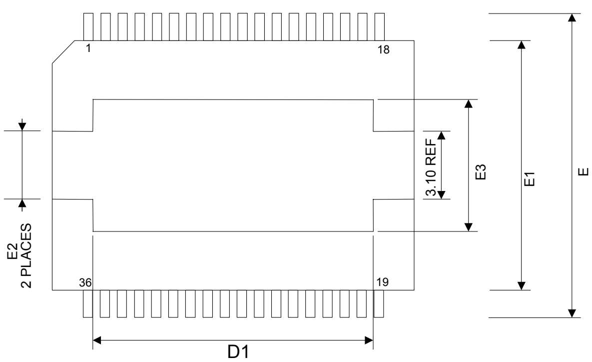
One feature of the TA2021B is that it does not require large multi-pole filters to achieve excellent performance in listening tests, usually a more critical factor than performance measurements. Though using a multi-pole filter may remove high-frequency noise and improve THD+N type measurements (when they are made with wide-bandwidth measuring equipment), these same filters degrade frequency response. The TA2021B Evaluation Board uses the Application/Test Circuit of this data sheet, which has a simple two-pole output filter and excellent performance in listening tests. Measurements in this data sheet were taken using this same circuit with a limited bandwidth setting in the measurement instrument.

Package Information

36-pin PSOP Package

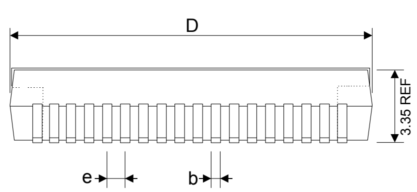
Package Dimensions for SLUG-UP



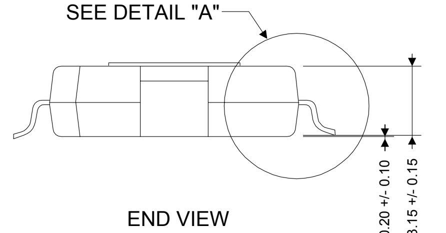


TOP VIEW

BOTTOM VIEW



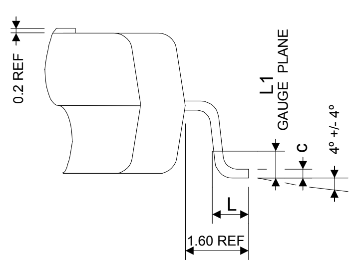
SIDE VIEW



END VIEW

Dimension	Min.	Nom.	Max.
b	0.22	---	0.38
c	0.23	---	0.32
D	15.8	15.9	16
D1	9.4	---	9.8
E	13.9	14.2	14.5
E1	10.9	11.0	11.1
E2	2.9	---	3.2
E3	5.8	---	6.2
e	0.65 BSC.		
L1	0.35 BSC.		
L	0.8	---	1.1

Note: All dimensions are in millimeters.



DETAIL "A"

Preliminary Information

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