

TOSHIBA

TA75458P/S/F/FB

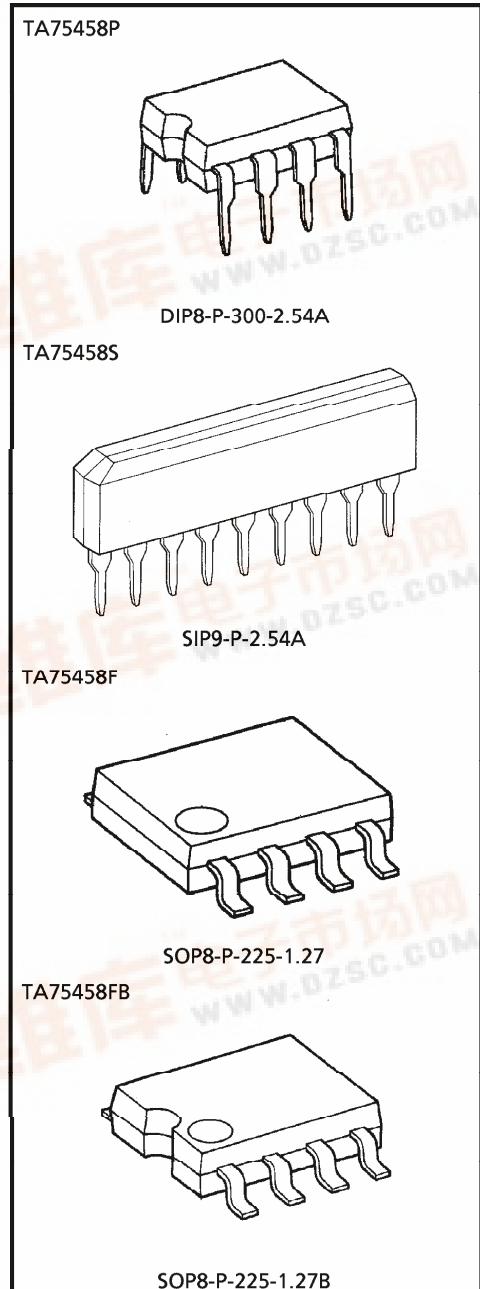
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA75458P, TA75458S, TA75458F, TA75458FB

DUAL OPERATIONAL AMPLIFIER

FEATURES

- Pair of Internally Compensated High Performance Amplifier
- No Frequency Compensation Required
- No Latch-up
- Short Circuit Protection
- Side Common Mode and Differential Voltage Range
- Low Power Consumption



Weight	
DIP8-P-300-2.54A	: 0.5g (Typ.)
SIP9-P-2.54A	: 0.9g (Typ.)
SOP8-P-225-1.27	: 0.1g (Typ.)
SOP8-P-225-1.27B	: 0.1g (Typ.)

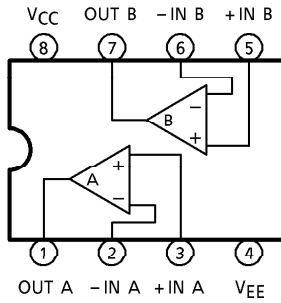
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● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

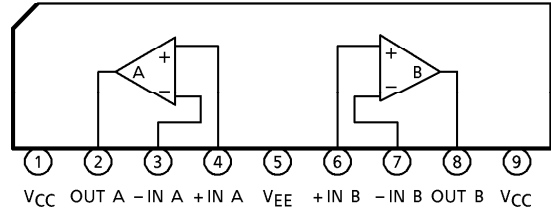


PIN CONNECTION (TOP VIEW)

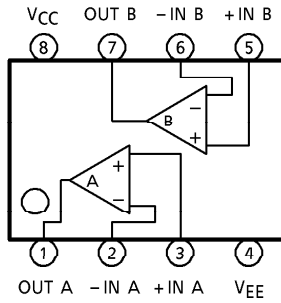
TA75458P



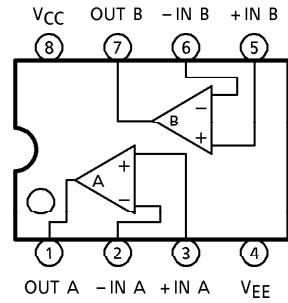
TA75458S



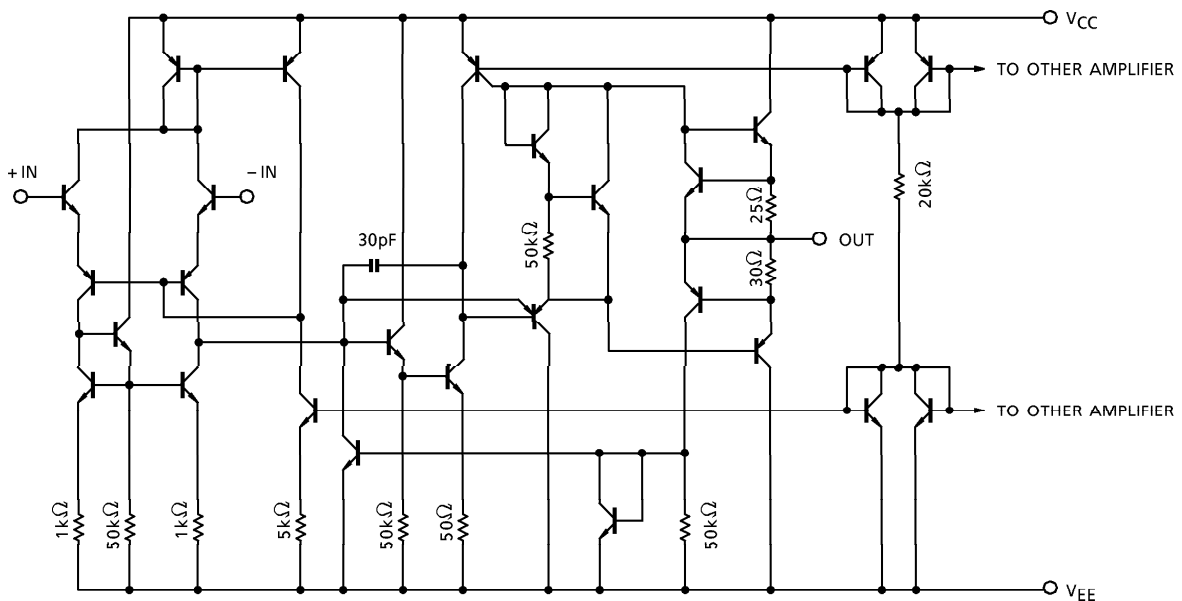
TA75458F



TA75458FB



EQUIVALENT CIRCUIT



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- The information contained herein is subject to change without notice.

MAXIMUM RATINGS (Ta = 25°C)

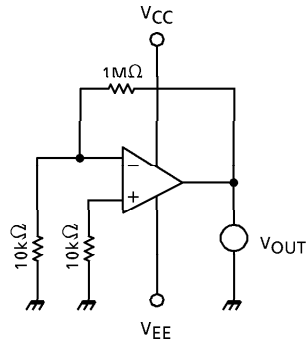
CHARACTERISTIC	SYMBOL	TA75458P	TA75458S	TA75458F TA75458FB	UNIT
Supply Voltage	V _{CC} , V _{EE}	+ 18, - 18	+ 18, - 18	+ 18, - 18	V
Differential Input Voltage	DV _{IN}	± 30	± 30	± 30	V
Input Voltage	V _{IN}	V _{CC} ~V _{EE}	V _{CC} ~V _{EE}	V _{CC} ~V _{EE}	V
Power Dissipation	P _D	500	400	240	mW
Operating Temperature	T _{opr}	- 40~85	- 40~85	- 30~75	°C
Ambient Temperature	T _{stg}	- 55~125	- 55~125	- 55~125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15V, V_{EE} = - 15V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage		V _{IO}	1	R _g ≤ 10kΩ	—	1	5	mV
Input Offset Current		I _{IO}	2		—	20	200	nA
Input Bias Current		I _I	2		—	80	500	nA
Common Mode Input Voltage		CMV _{IN}	3		± 12	± 13	—	V
Maximum Output Voltage		V _{OM}	4	R _L = 10kΩ	± 12	± 14	—	V
		V _{OMR}	4	R _L = 2kΩ	± 10	± 13	—	
Source Current		I _{source}	4		—	20	—	mA
Sink Current		I _{sink}	4		—	20	—	mA
Differential Input Impedance	Parallel Input Resistance	Z _{Di}	—	f = 20Hz Open Loop	0.3	1.0	—	MΩ
	Parallel Input Capacitance	C _i	—		—	6.0	—	pF
Output Impedance		Z _o	—	f = 20Hz	—	75	—	Ω
Voltage Gain (Open Loop)		G _V	7	V _{OUT} = ± 10V, R _L = 2kΩ	86	100	—	dB
Common Mode Input Signal Rejection Ratio		CMRR	3	f = 100Hz	70	90	—	dB
Supply Voltage Rejection Ratio		SVRR	1	R _g ≤ 10kΩ	—	30	150	μV/V
Power Bandwidth		f _W	—	G _V = 1, R _L = 2kΩ V _{OUT} = 20V _{p-p}	—	14	—	kHz
Slew Rate		SR	6	G _V = 1, R _L = 2kΩ	—	0.8	—	V/μs
Unity Gain Cross Frequency		f _T	7	Open Loop	—	1.1	—	MHz
Power Dissipation		P _D	5	V _O = 0V	—	70	170	mW
Input Offset Voltage Drift		ΔV _{IO} /ΔT	1	R _g ≤ 10kΩ, Ta = - 30~75°C	—	—	50	μV/°C
Supply Current		I _{CC} , I _{EE}	5		—	2.3	5.6	mA

TEST CIRCUIT

(1) V_{IO} , $\Delta V_{IO} / \Delta T$, SVRR



$$V_{IO} = V_{OUT} / 100 \text{ (V)}$$

$$\Delta V_{IO} / \Delta T = \{V_{IO} (25^\circ\text{C}) - V_{IO} (-30^\circ\text{C})\} / 55 \text{ (V / }^\circ\text{C)}$$

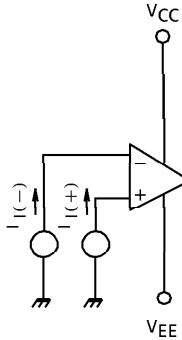
$$\Delta V_{IO} / \Delta T = \{V_{IO} (75^\circ\text{C}) - V_{IO} (25^\circ\text{C})\} / 50 \text{ (V / }^\circ\text{C)}$$

$$SVRR = (V_{IO1} - V_{IO2}) / 5 \text{ (}\mu\text{V / V)}$$

V_{IO1} : V_{CC} , AT $V_{EE} = \pm 17.5\text{V}$

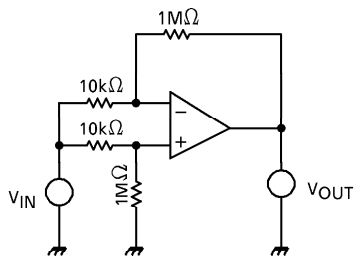
V_{IO2} : V_{CC} , At $V_{EE} = \pm 12.5\text{V}$

(2) I_I , I_{IO}



$$I_{IO} = |I_I(+)-I_I(-)|$$

(3) CMV_{IN} , CMRR

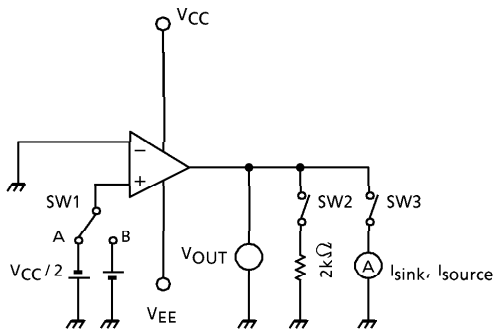


CMV_{IN} : $V_{OUT} = \pm 1\text{V (DC)}$
 $V_{IN} = \text{MEASURE}$

CMRR : RATIO OF G_{diff} vs G_{CM}

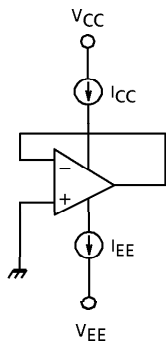
$$CMRR = 20 \log \frac{G_{diff}}{G_{CM}} \text{ (dB)}$$

(4) V_{OM} , V_{OMR} , I_{sink} , I_{source}



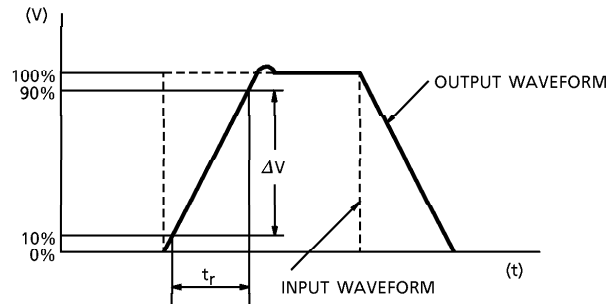
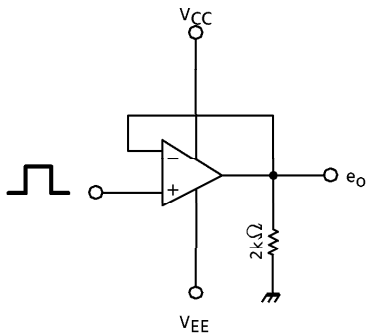
- $V_{OM} (+)$: SW1 IS SIDE B, SW2 OFF, SW3 OFF
- $V_{OM} (-)$: SW1 IS SIDE A, SW2 OFF, SW3 OFF
- $V_{OMR} (+)$: SW1 IS SIDE B, SW2 ON, SW3 OFF
- $V_{OMR} (-)$: SW1 IS SIDE A, SW2 ON, SW3 OFF
- I_{sink} : SW1 IS SIDE A, SW2 OFF, SW3 ON
- I_{source} : SW1 IS SIDE B, SW2 OFF, SW3 ON

(5) I_{CC} , I_{EE} , P_D

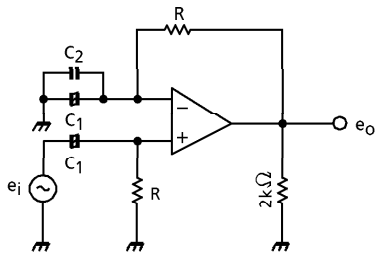


$$P_D = V_{CC} \cdot I_{CC} + V_{EE} \cdot I_{EE} \text{ (W)}$$

(6) SR



(7) G_V, f_T



G_V

$$R \geq 1 / \omega C_1$$

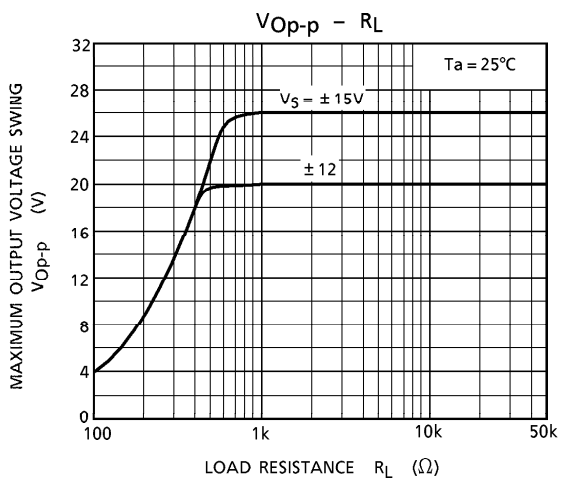
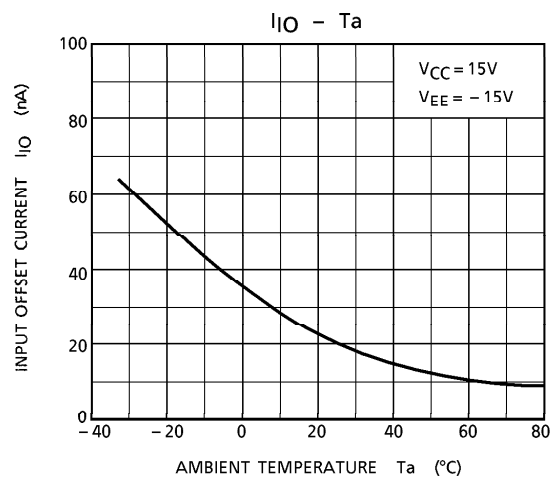
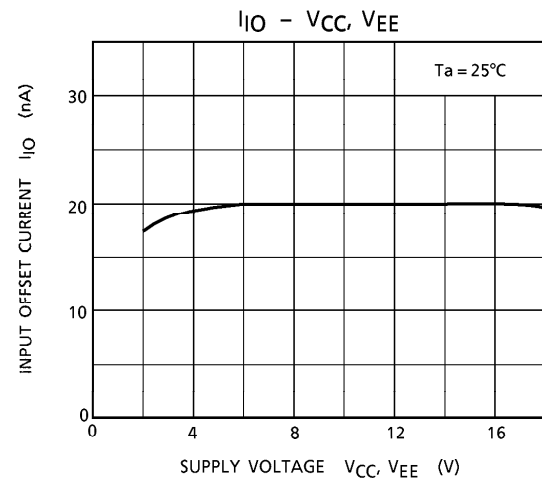
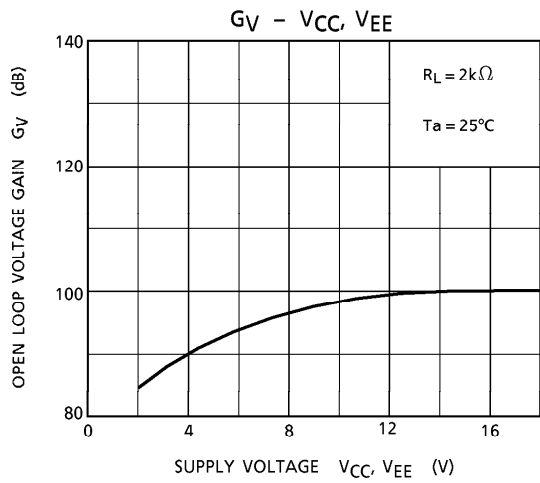
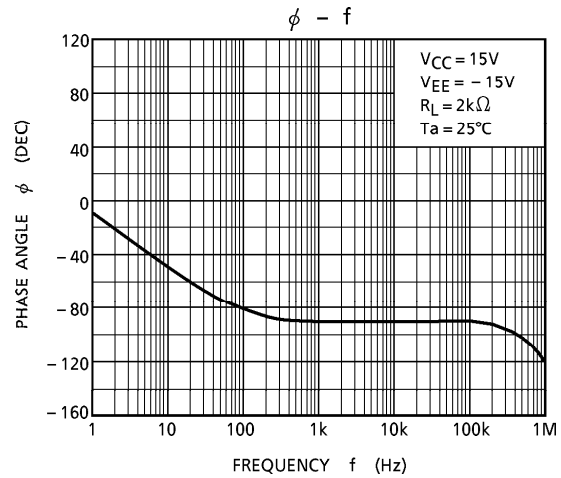
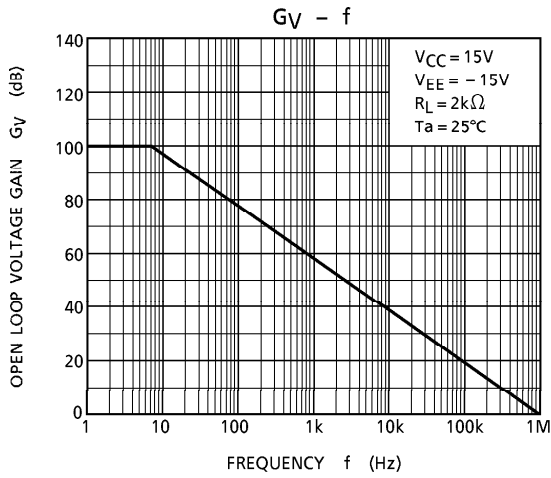
C_1 : COUPLING CONDENSER

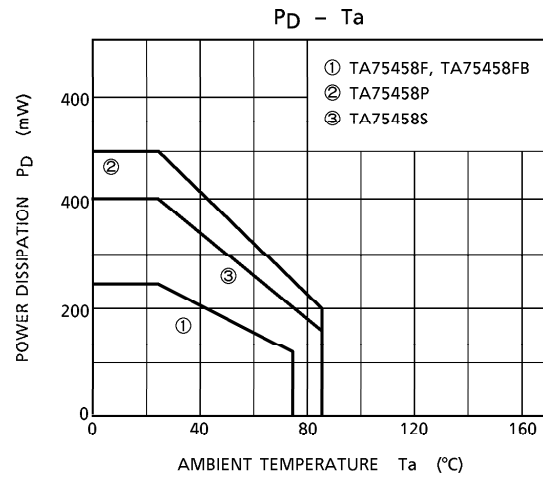
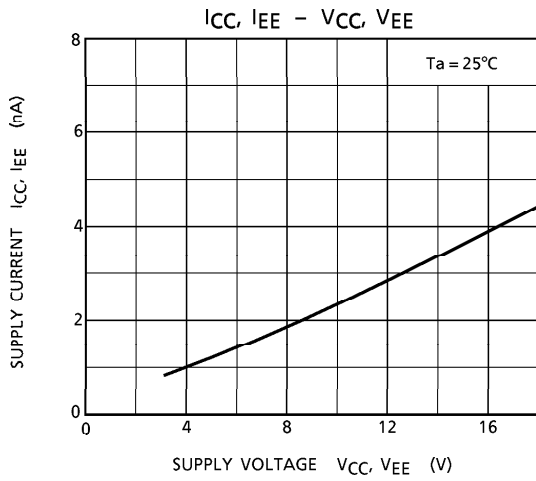
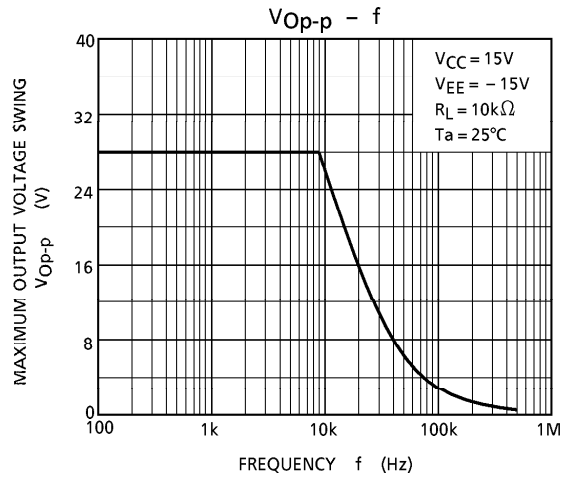
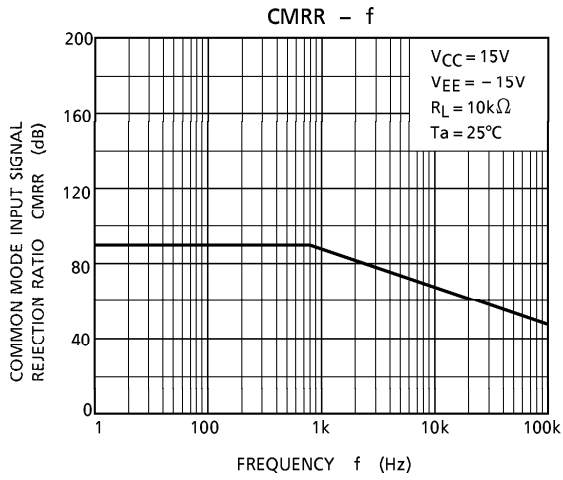
C_2 : HIGH FREQUENCY BYPASS CONDENSER
0.1 μ F

$$G_V = 20 \log e_o / e_i \text{ (dB)}$$

f_T INPUT FREQUENCY AT $e_i = e_o$

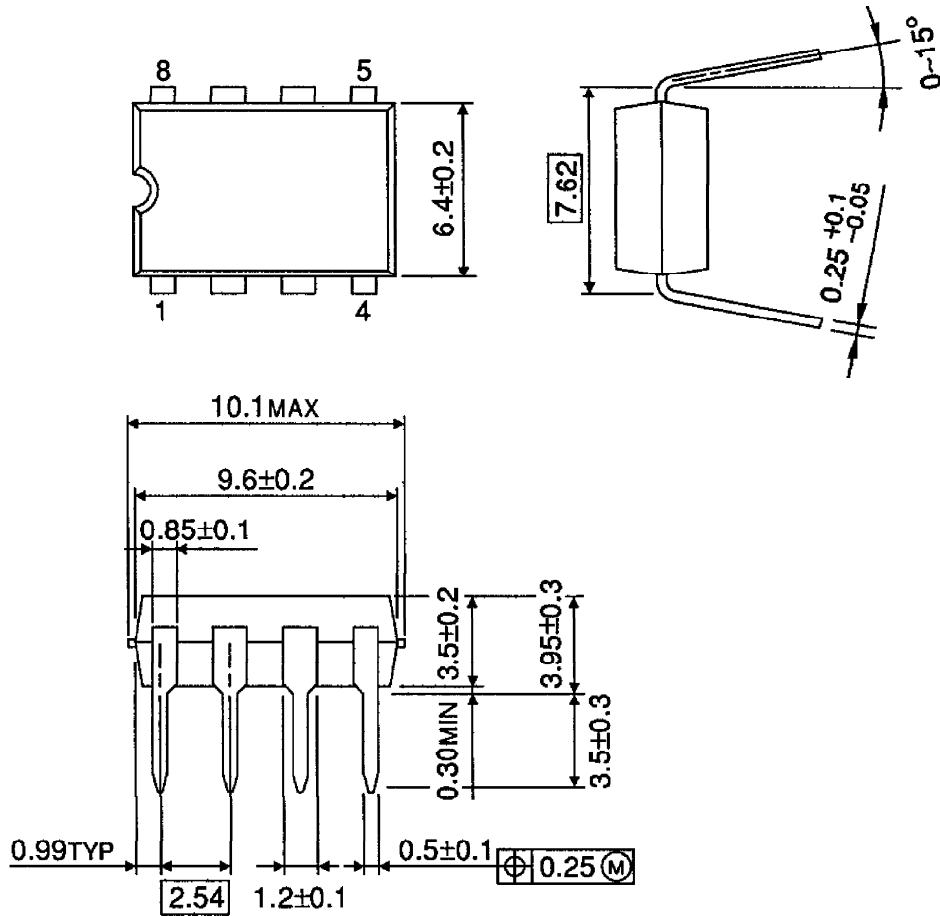
CHARACTERISTICS





OUTLINE DRAWING
DIP8-P-300-2.54A

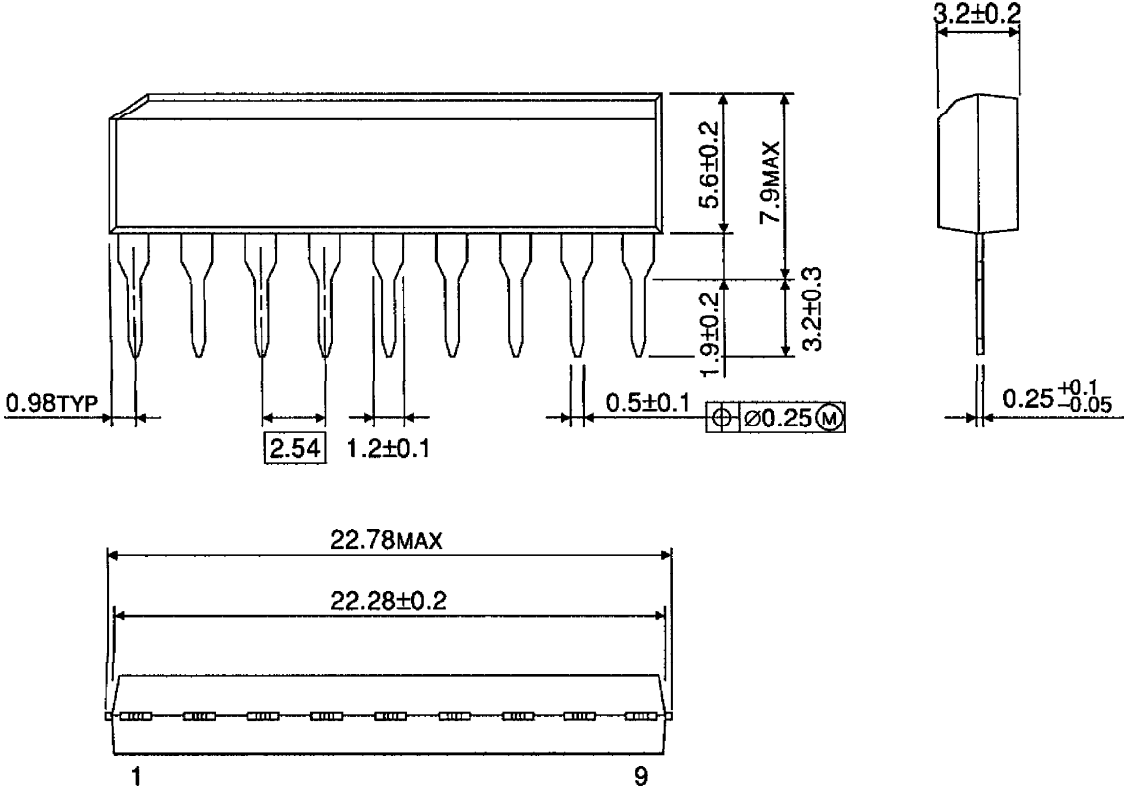
Unit : mm



Weight : 0.5g (Typ.)

OUTLINE DRAWING
SIP9-P-2.54A

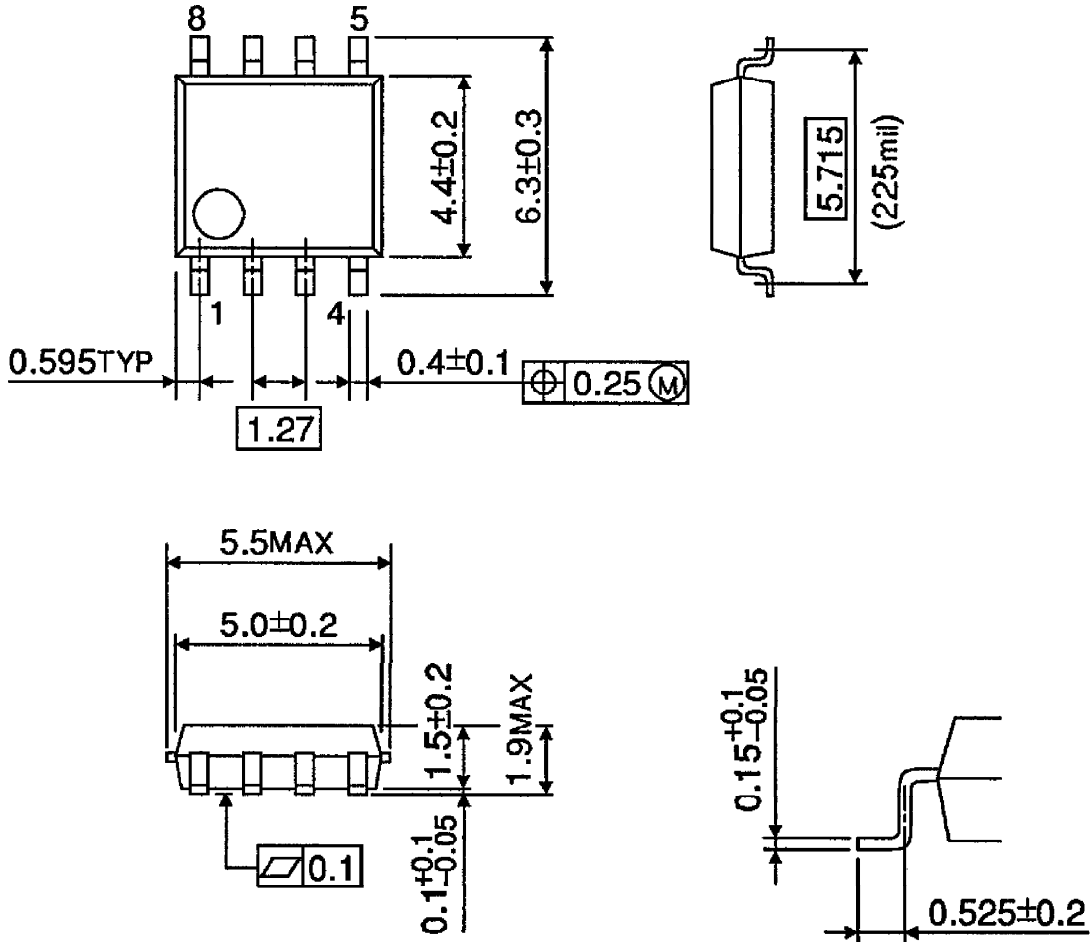
Unit : mm



Weight : 0.9g (Typ.)

OUTLINE DRAWING
SOP8-P-225-1.27

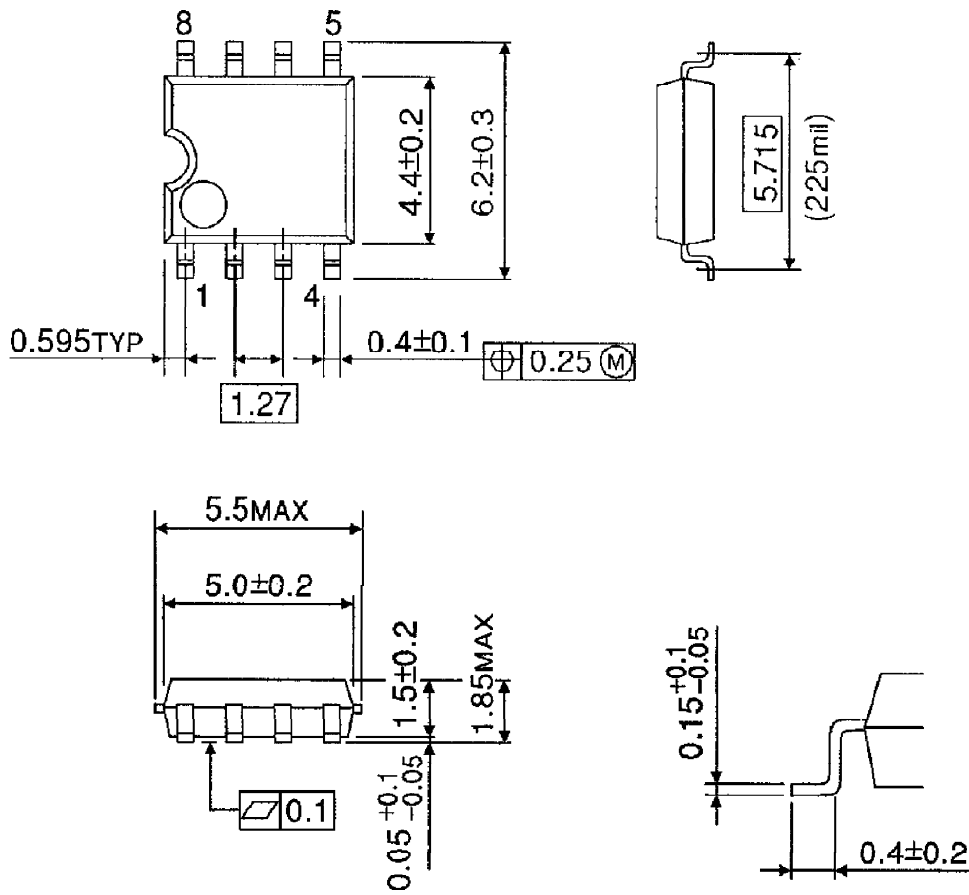
Unit : mm



Weight : 0.1g (Typ.)

OUTLINE DRAWING
SOP8-P-225-1.27B

Unit : mm



Weight : 0.1g (Typ.)