



INTEGRATED CIRCUIT

TECHNICAL DATA

TA7680AP, TA7681AP

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

TELEVISION PIF + SIF SYSTEM

TA7680AP....FOR FET TUNER

TA7681AP....FOR NPN TUNER

FUNCTIONS

PIF

- . Three Controlled IF Amplifier Stages
- . Video Demodulator Controlled by Picture Carrier
- . Black Noise and White Noise Inverter
- . Peak AGC
- . DC Amplifier for RF AGC Out

SIF

- . Three Differential IF Amplifier Stages
- . Phase Detector
- . DC Controlled Attenuator
- . Audio Amplifier Stage with NFB Terminal

FEATURES

- . PIF, SIF, ATT AUDIO DRIVER
- . 2 Chip Color TV System is Possible with TA7644BP

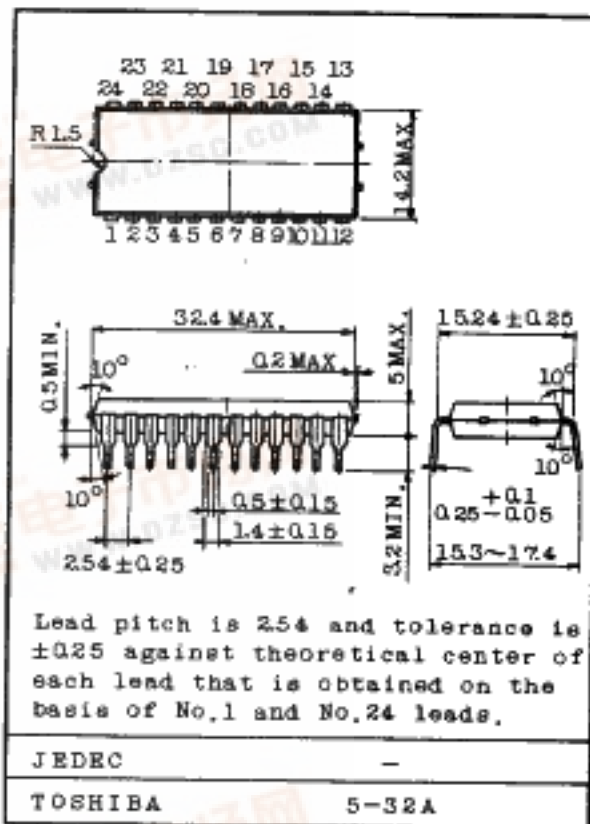
PIF

- . High Gain, Wide Band IF Amplifier
- . AGC Characteristics with Excellent Stability
- . Excellent DG/DP Characteristics
- . Excellent S/N Characteristics Due to Delayed 3 Stages AGC Action
- . Negative Video Output Signal
- . Switch Off the Video Part with VTR SW

SIF

- . Excellent Limiter Characteristics
- . Excellent Attenuator Characteristics

Unit in mm





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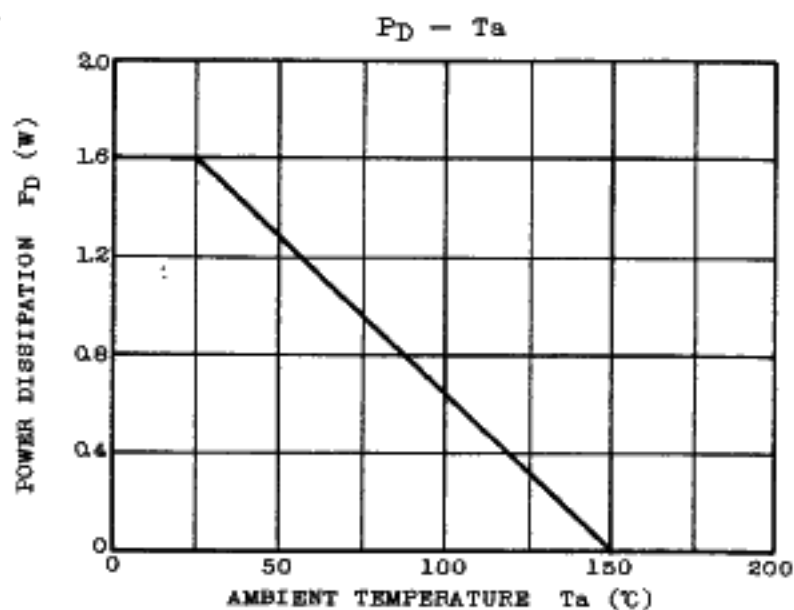
TECHNICAL DATA

TA7680AP, TA7681AP

MAXIMUM RATINGS ($T_a=25^{\circ}\text{C}$)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	15	V
Terminal 11 Open Voltage	V_{11}	15	V
Video DC Output Current	I_{15}	6	mA
Audio DC Output Current	I_3	3	mA
Terminal 2 Voltage	V_2	15	V
Power Dissipation (Note)	P_D	1.6	W
Operating Temperature	T_{opr}	-20 ~ 65	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-55 ~ 150	$^{\circ}\text{C}$

Note : Derated above $T_a=25^{\circ}\text{C}$ in the proportion of $12.8\text{mW}/^{\circ}\text{C}$.



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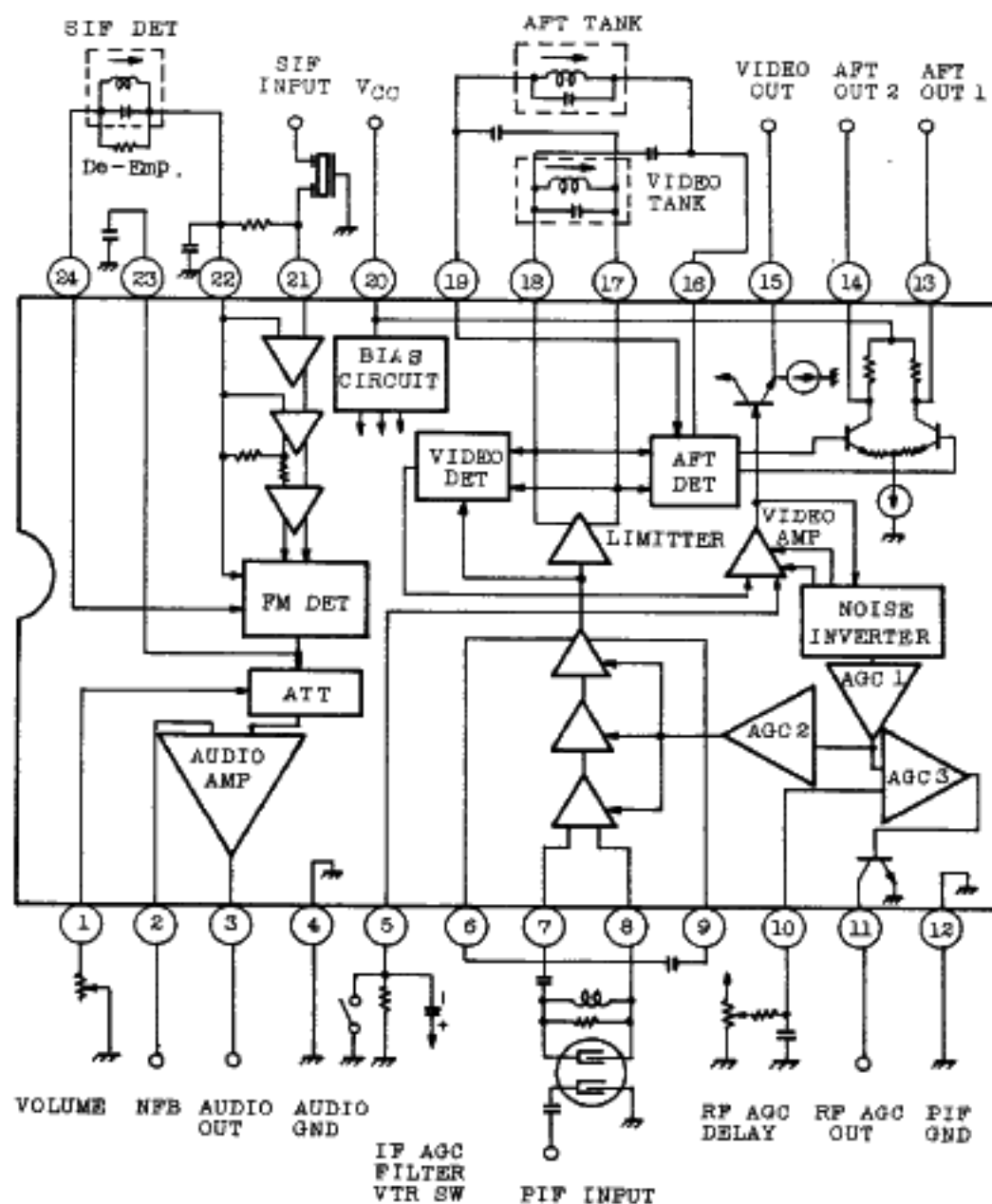


INTEGRATED CIRCUIT

TECHNICAL DATA

TA7680AP, TA7681AP

BLOCK DIAGRAM



■ 9097247 0019621 932 ■



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TECHNICAL DATA

TA7680AP, TA7681AP

ELECTRICAL CHARACTERISTICS (Ta=25°C, VCC=12V, fp=58.75MHz, fs=54.25MHz)

PIF SECTION

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Recommended Supply Voltage	VCC	-	-	10.8	12.0	13.2	V
Supply Current	ICC	1	-	50	72	95	mA
Video DC Output Voltage	V15	1	SW1:1(TA7680AP) 2(TA7681AP) SW2:2	5.2	5.5	5.8	V
AFT DC Output Voltage	V13	1	SW1:1(TA7680AP) 2(TA7681AP) SW2:2	5.3	6.8	8.3	V
	V14	1	SW1:1(TA7680AP) 2(TA7681AP) SW2:2	5.3	6.8	8.3	V
AFT DC Offset Voltage	ΔV_{13-14}	1	SW1:1(TA7680AP) 2(TA7681AP) SW2:2	-1.5	0	1.5	V
RF AGC Residual Output Voltage	V11 SAT	1	SW1:1(TA7680AP) 2(TA7681AP) SW2:2	-	-	0.5	V
RF AGC Leak Current	I11 LEAK	1	SW1:1(TA7681AP) 2(TA7680AP) SW2:1	-	-	1	μA
Video Sensitivity	v_i PIN7-8	2	(Note 1)	60	150	250	μV_{rms}
AGC Range	ΔA_{PIF}	2	(Note 2)	60	64	-	dB
Sync Tip Level Voltage	VSYNC (V15)	2	(Note 3)	2.3	2.5	2.7	V
Max. IF Input Voltage	$v_{IN MAX}$ PIF	2	(Note 4)	100	120	-	mV_{rms}
White Noise Threshold Level	VWTH (V15)	2	(Note 5)	5.8	6.2	6.6	V
White Noise Clamp Level	VWCL (V15)	2	(Note 5)	3.7	4.1	4.5	V

9097247 0019622 879



INTEGRATED CIRCUIT

TECHNICAL DATA

TA7680AP, TA7681AP

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Black Noise Threshold Level		$V_{B TH}$ (V15)	2	(Note 5)	1.4	1.6	1.8	V
Black Noise Clamp Level		$V_{B CL}$ (V15)	2	(Note 5)	2.9	3.3	3.7	V
Video Frequency Response		f_{BW}	3	(Note 6)	4.5	5.5	-	MHz
Suppression of Carrier		CL	4	(Note 7)	40	50	-	dB
Suppression of 2nd Carrier		I _{2nd}	4	(Note 8)	40	50	-	dB
920kHz Beat Level		I ₉₂₀	4	(Note 9)	33	38	-	dB
Differential Phase		DP	5	(Note 10)	-	3.5	5	deg
Differential Gain		DG	5	(Note 10)	-	7	10	%
PIF Input Impedance		R _{IN} (PIF)	6	(Note 11)	1.5	3.0	6.0	kΩ
		C _{IN} (PIF)			-	3.0	10.0	pF
AFT Sensitivity		$\Delta F/V_{13-14}$	2	(Note 12)	-	16	-	kHz/V
AFT Output Voltage	Upper	V _{13U} V _{14U}	2	(Note 13)	11.7	11.9	1.20	V
	Lower	V _{13L} V _{14L}	2	(Note 13)	1.8	2.3	2.8	V
RF AGC Max. Available Current		I _{4 MAX}	1	TA7680AP SW1:1 SW2:1	0.3	-	-	mA
				TA7681AP SW1:2 SW2:1	7.0	-	-	
RF AGC Delay Setting Range		V _{IN} DELAY		(Note 14)	5	7	9	V
AFT Band Width		ΔF_W	2	(Note 13)	1.4	-	-	MHz
Video Output Voltage		v_{OUT}	2	(Note 15)	2.25	2.5	2.75	V
SIF Output Voltage		S _{OUT}	3	(Note 16)	200	400	600	mV _{rms}

9097247 0019623 705



INTEGRATED CIRCUIT

TECHNICAL DATA

TA7680AP, TA7681AP

SIF SECTION

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Limiting Voltage		$V_{IN(LIM)}$	8	(Note 17) $R_D = \infty$	-	200	400	μV_{rms}
AM Rejection Ratio		AMR	8	SIF IN : $f = 4.5MHz$ $f_m = 400Hz$, $\Delta f = \pm 25kHz$ AM 30%, $v_{in} = 100dB_{\mu}$	40	45	-	dB
Recovered Output Voltage		V_{OD}	8	SIF IN : $f = 4.5MHz$ $f_m = 400Hz$, $\Delta f = \pm 25kHz$ $v_{in} = 80dB_{\mu}$, $R_D = 12k\Omega$	0.5	0.75	-	V_{rms}
Total Harmonic Distortion		THD _{DET}	8	SIF IN : $f = 4.5MHz$ $f_m = 400Hz$, $\Delta f = \pm 25kHz$ $v_{in} = 80dB_{\mu}$	-	1.0	-	%
Max. Audio Output Voltage		V_{OM}	8	SIF IN : $f = 4.4 \sim 4.6MHz$	4.0	-	-	V_{p-p}
SIF Input Impedance		$R_{IN(SIF)}$	7	$f = 4.5MHz$	10.0	20.0	30.0	k Ω
		$C_{IN(SIF)}$			-	3.0	-	pF
DET Output Impedance		$R_{O(DET)}$	9	(Note 18)	10.0	15.0	20.0	k Ω
DC Voltage	Terminal 21	V_{21}	1	SW ₁ :1 (TA7680AP)	3.5	4.4	5.3	V
	Terminal 23	V_{23}		2 (TA7681AP)	4.8	6.0	7.2	V
	Terminal 1	V_1		SW ₂ :2	6.0	6.7	7.4	V
Max. Attenuation		ATT MAX	10	(Note 19)	60	-	-	dB
DC Volume Gain		$G_{ATT MIN}$	10	$R_A = 0$ $G_{ATT MIN} = 20 \log \frac{v_2}{v_{23}}$	4	6	8	dB
ATT Characteristics	1	$V_1(1)$	10	*	3.4	3.8	4.2	V
	2	$V_1(2)$	10	**	4.5	4.9	5.3	V
Signal Leakage		v_{PT}	11	(Note 20)	-	1.0	3.0	mV _{rms}
AF Amp. Gain		$G_V AF$	13	(Note 21)	-	20	-	dB
AF Amp. Distortion		THD AF	12	$P_{23A} = 1V_{pp}$, 400Hz SW ₃ :ON ATT:-26dB Setting	-	1.5	-	%
AF Amp. Max. Output Voltage		$v_{OAF MAX}$	13	(Note 21) THD _{AF} 5%	1.5	2.0	-	V_{rms}
AF Output DC Voltage		V_3	1	SW ₁ :1 (TA7680AP) 2 (TA7681AP) SW ₂ :2	6.7	7.7	8.8	V

* Read the 400Hz component of V_{A1} at P₂ with $R_A = 0$. Set R_A so that $V_{A1}' = \frac{1}{2} V_{A1}$ (-6dB), then read DC voltage of terminal 1 (V_1).

** Read the 400Hz component of V_{A1} at P₂ with $R_A = 0$. Set R_A so that $V_{A1}' = 3.16 \times 10^{-3} V_{A1}$ (-50dB) then read DC voltage of terminal 1 (V_1).

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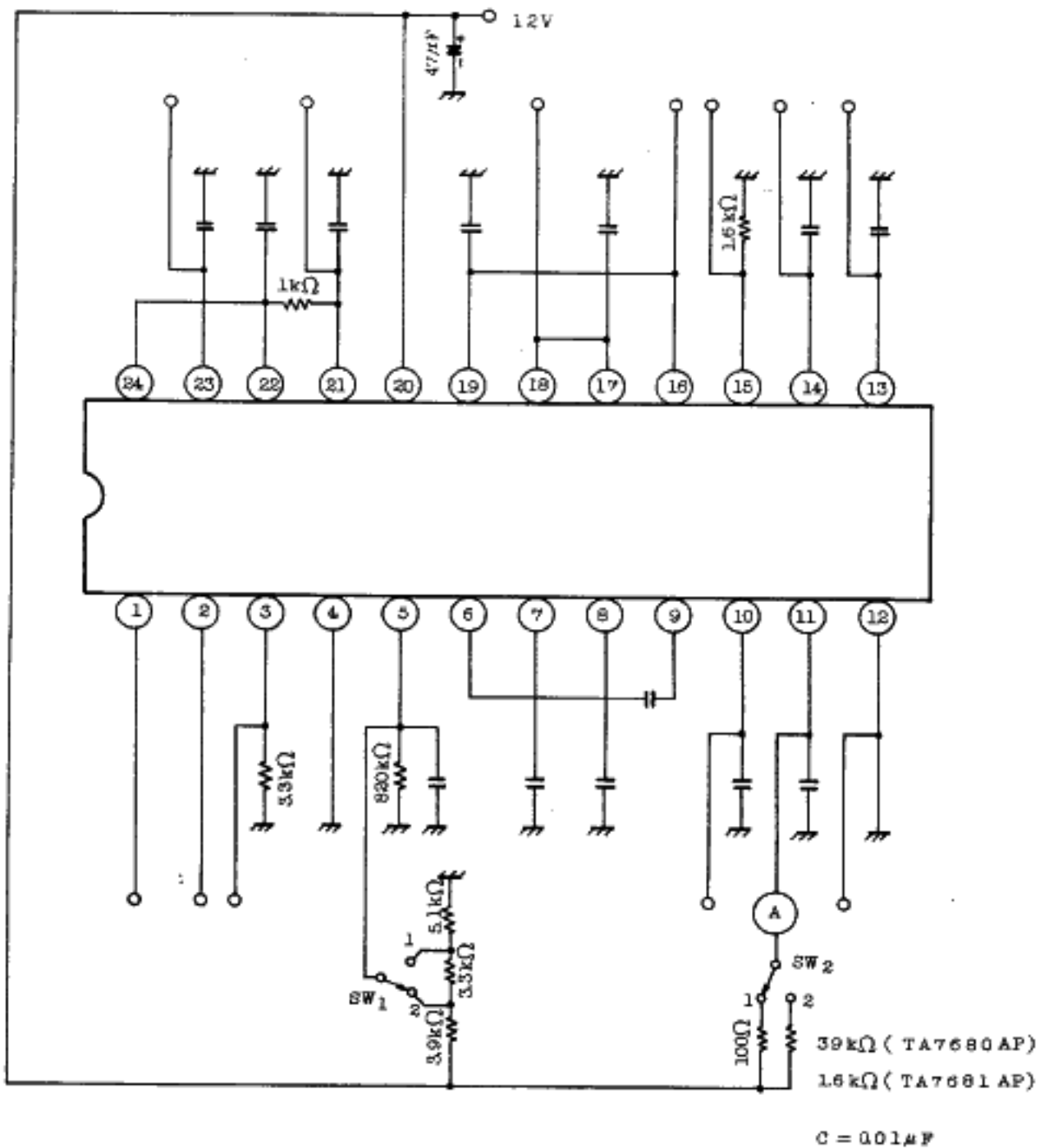
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TECHNICAL DATA

TA7680AP, TA7681AP

TEST CIRCUIT

1. DC CHARACTERISTIC



9097247 0019625 588

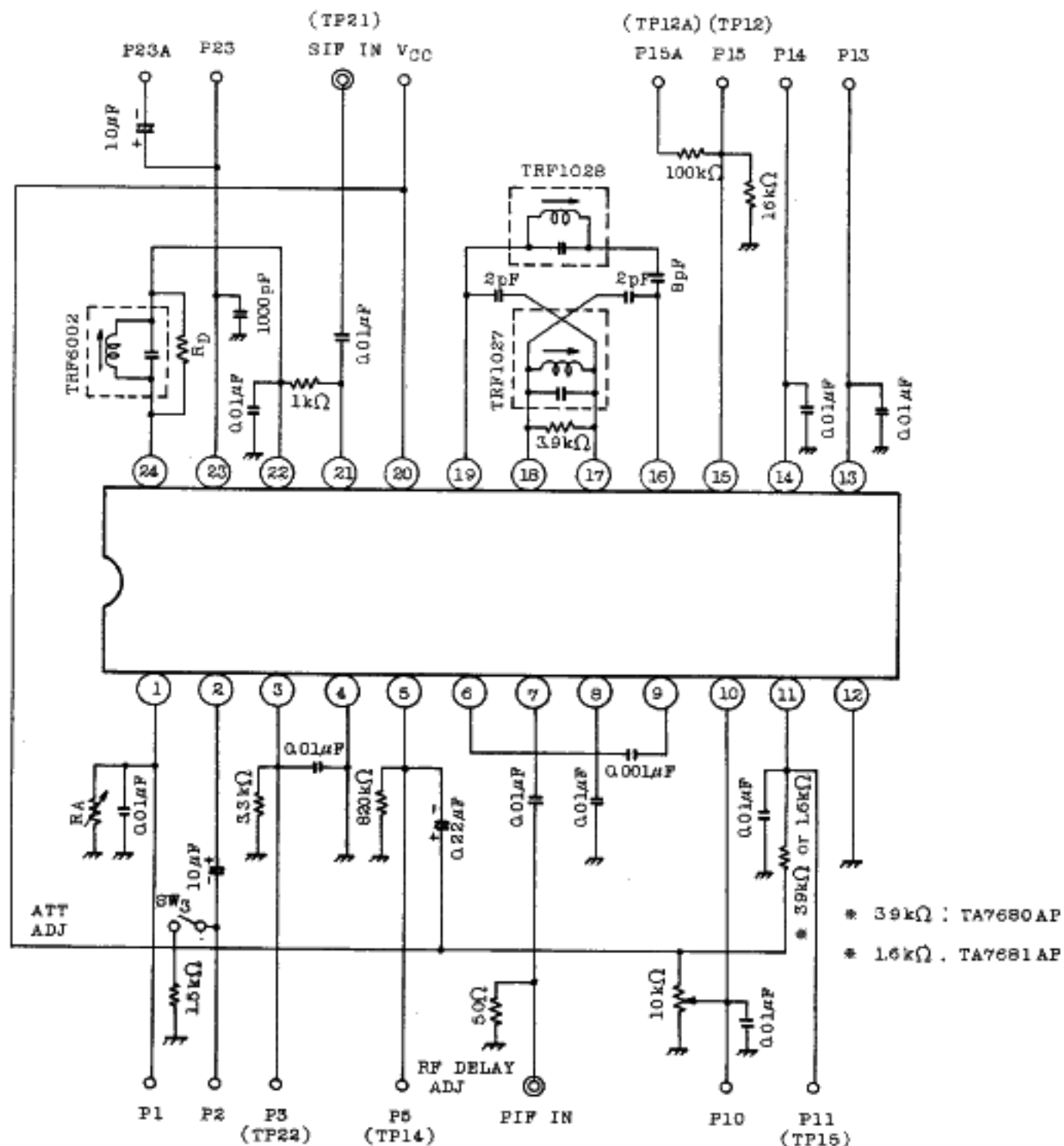


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TA7680AP, TA7681AP

2. AC CHARACTERISTIC



9097247 0019626 414

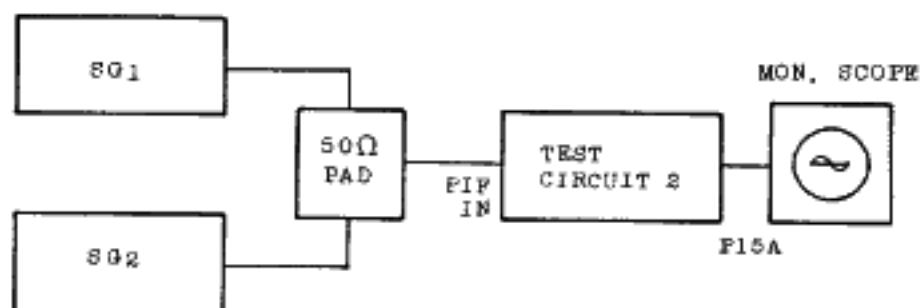


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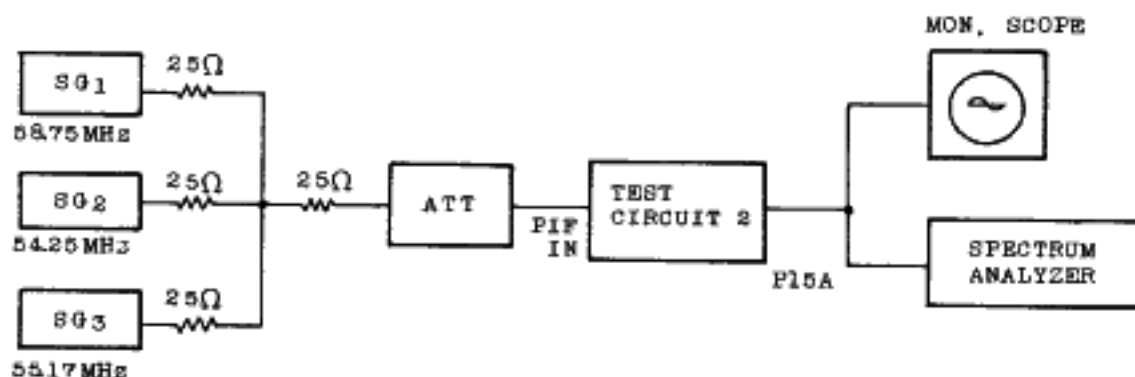
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TA7680AP, TA7681AP

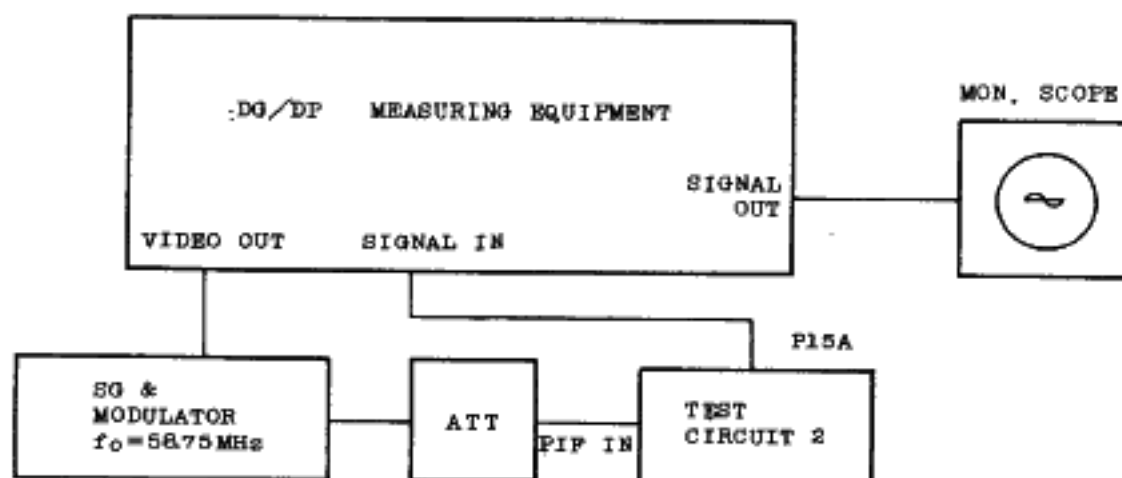
3. VIDEO FREQUENCY RESPONSE AND SIF OUTPUT VOLTAGE



4. INTER MODULATION



5. DG, DP



APL=50%

ATT : ADJUST SYNC TIP LEVEL TO DC 25V

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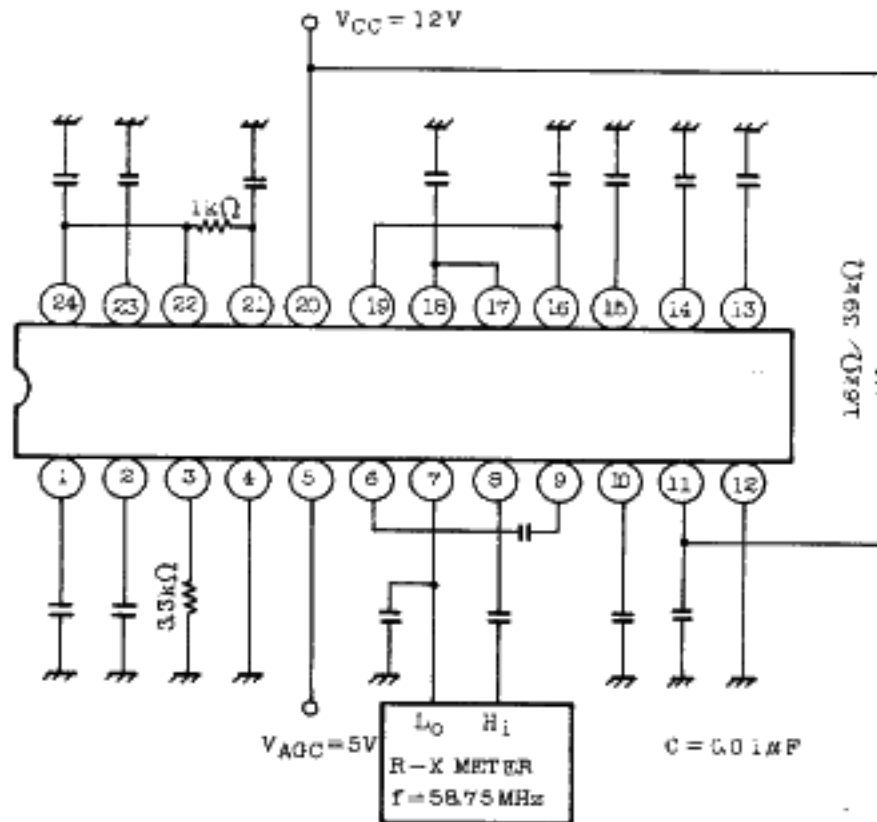


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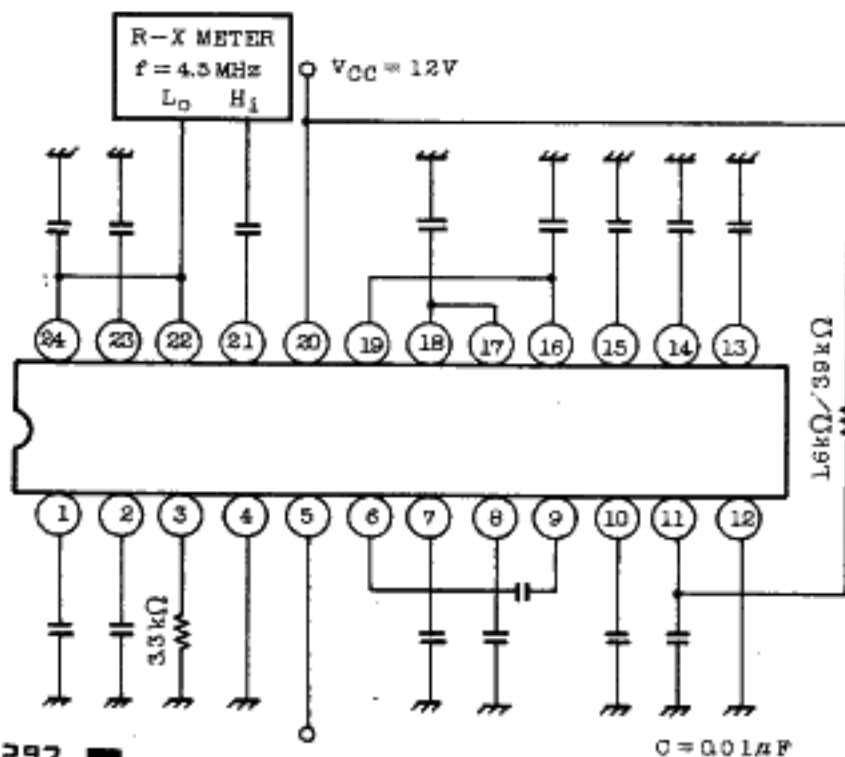
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TA7680AP, TA7681AP

6. PIF INPUT IMPEDANCE



7. SIF INPUT IMPEDANCE



9097247 0019628 297

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TOSHIBA CORPORATION

EJB-TA7680AP-10

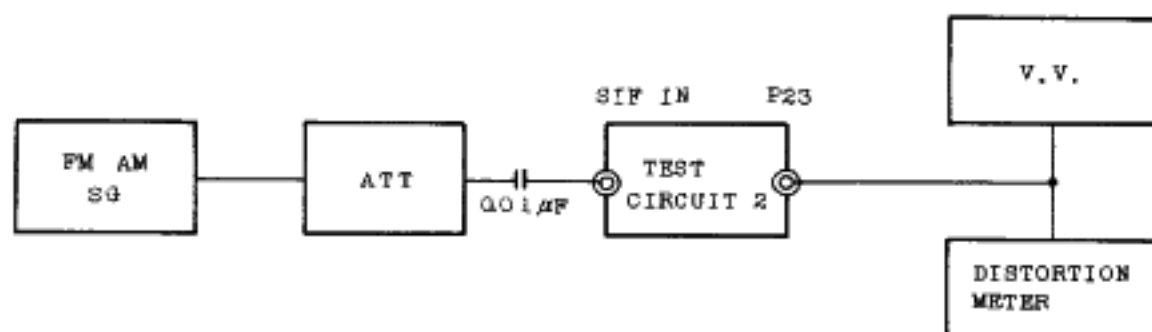


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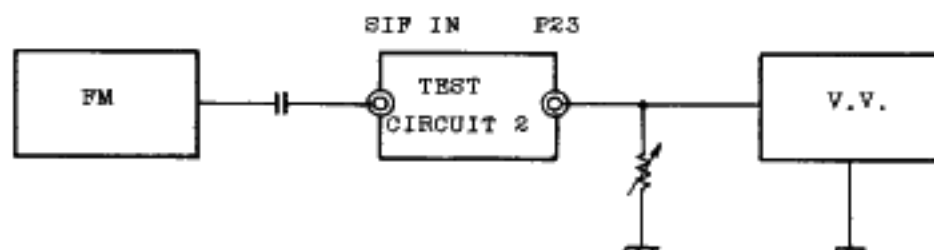
TECHNICAL DATA

TA7680AP, TA7681AP

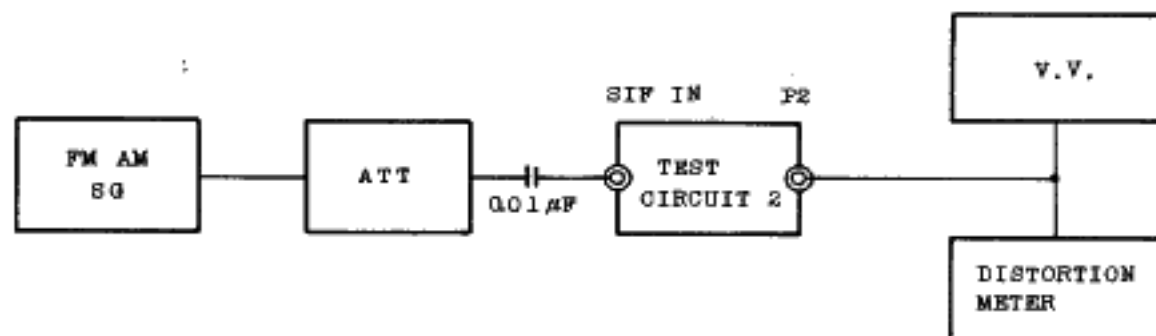
8. $V_{IN(LIM)}$, AMR, V_{OD} , THD, V_{OM}



9. AUDIO OUTPUT IMPEDANCE



10. ATT MAX., G_{ATT} MIN, $V_1(1)$, $V_1(2)$



■ 9097247 0019629 123 ■

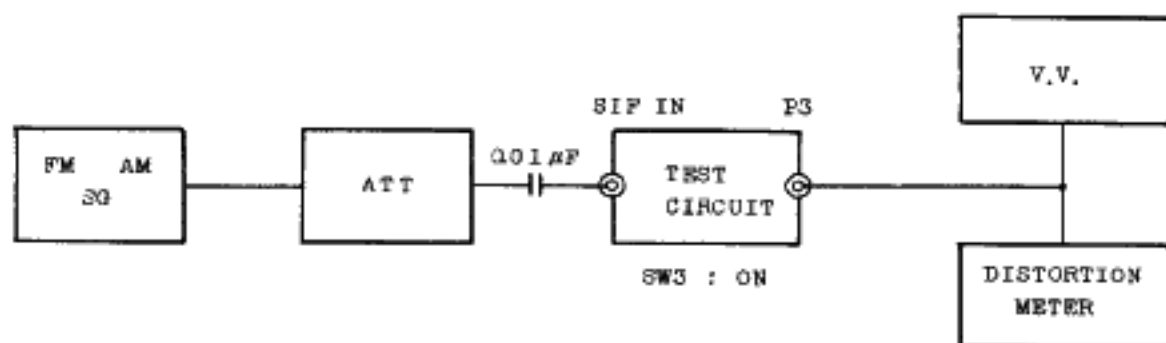


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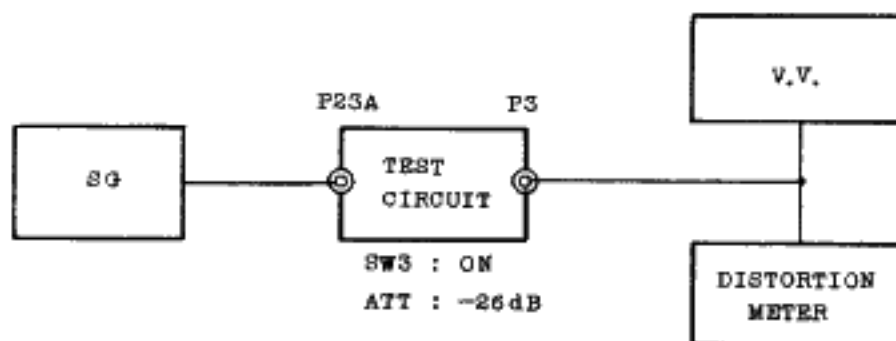
TECHNICAL DATA

TA7680AP, TA7681AP

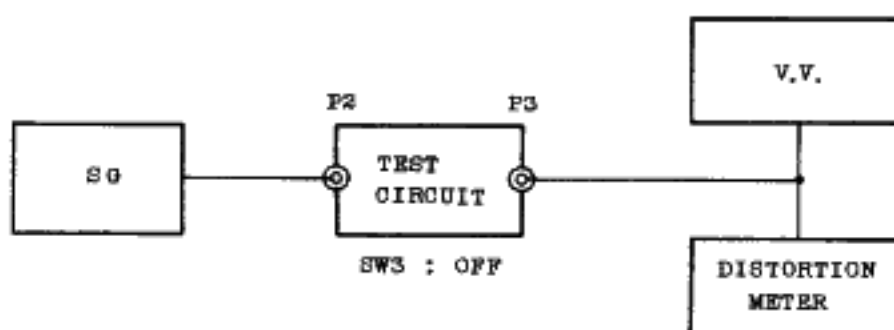
11. v_{PT}



12. THD_{AF}



13. $G_{V AF}$, $v_{OAF MAX}$:



9097247 0019630 945



INTEGRATED CIRCUIT

TECHNICAL DATA

TA7680AP, TA7681AP

TEST CONDITION

Note 1) V_{AGC} (P5 EXT. Applying Voltage)=11.5V

PIF IN ; $f=58.75\text{MHz}$ 1kHz 30% AM Modulation.

Adjust PIF Input Level v_i so that the detected output of P15A with high impedance probe will be $0.8V_{p-p}$ and measure the Input Level.

Note 2) $V_{AGC}=4V$

Measure PIF Input Level v_i' same as NOTE 1

$$\Delta A = 20 \log \frac{v_i'}{v_i} \quad [\text{dB}]$$

Note 3) PIF IN ; $f=58.75\text{MHz}$ CW 15mV_{rms}

Measure DC level of P15

Note 4) PIF IN ; $f=58.75\text{MHz}$ APL 100%, 87.5% AM modulation.

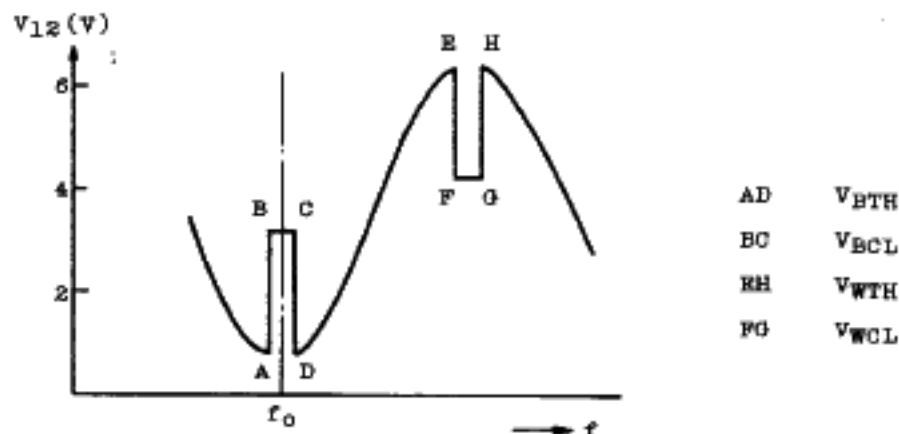
P5 : open

(1) Adjust PIF Input Level 50mV_{p-p} and measure the detected output level v_{01p-p}

(2) Then increase the Input Level so that the detected output level will be $1.1 \times v_{01p-p}$ and measure the Input Level.

Note 5) $V_{AGC}=8V$

PIF IN ; $f=58.75\text{MHz} \pm 10\text{MHz}$ variable or sweep 15mV_{rms} measure DC level of P15.





INTEGRATED CIRCUIT

TECHNICAL DATA

TA7680AP, TA7681AP

- Note 6) $V_{AGC}=8V$ ($GR \approx 30dB$)
SG₁ : 58.75MHz CW
SG₂ : 58.65~40MHz Variable
(1) Setting output of SG₁ so that DC level of P15 will be 4.0V
(2) Setting output of SG₂ (58.65MHz) so that AC level of P15 will be 0.5V_{p-p}
(3) Decreasing frequency of SG₂ until AC level of P15 will be 0.35V_{p-p} (-3dB of 0.5V_{p-p}) then read fSG₂=F
 $f_{BW}=58.75-F$ MHz
- Note 7) SG₁ ; 58.75MHz, 1kHz 80% AM modulation 100mV_{rms}
SG₂, SG₃ ; OFF
Setting V_{AGC} so that output AC level of P15 will be 2.7V_{p-p}
Measure CL of P15 after setting to 0% AM of SG₁
$$CL = 20 \log \frac{2.7}{v_{CR}(V_{p-p})} \quad (dB)$$
- Note 8) Measure I_{2nd} of P15 same as NOTE 7
- Note 9) $V_{AGC}=8V$
SG₁ ; 58.75MHz (P; Picture) 100mV_{rms}
SG₂ ; 54.25MHz (S; Sound) 32mV_{rms} (-10dB of SG₁)
SG₃ ; 55.17MHz (C; Chroma) 32mV_{rms} (-10dB of SG₁)
(1) Setting V_{AGC} so that the output tip level (lower) of P15 will be 3.0V DC
(2) Measure the level difference (dB) between c-level and 920kHz level
- Note 10) $V_{AGC}=8V$
PIF IN ; f=58.75MHz Video Signal (ramp) 87.5% AM 100mV_{p-p}
Setting ATT so that the sync tip level of P15 will be 2.5V DC
Measure DP and DG.
- Note 11) $V_{AGC}=5V$ f=58.75MHz
Measure R_{IN}, C_{IN}

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INTEGRATED CIRCUIT

TA7680AP, TA7681AP

TECHNICAL DATA

Note 12) AFT Sensitivity $\Delta F/\Delta(V_{13}-V_{14})$

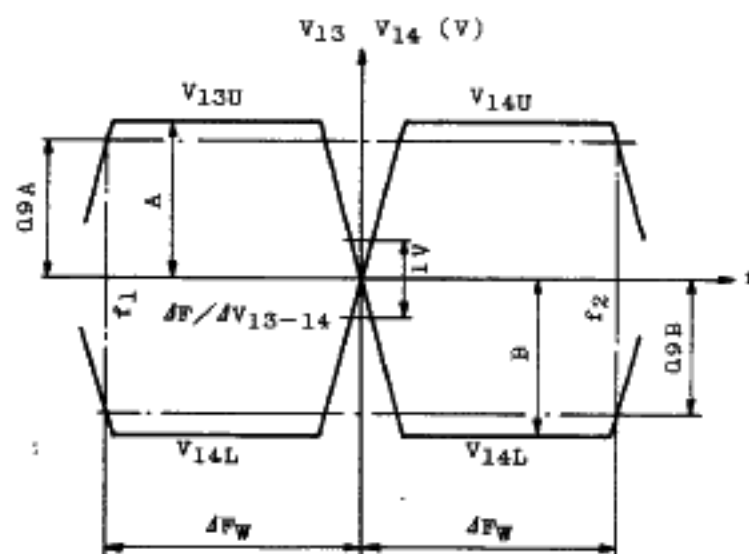
- (1) INT, AGC (P5 Open)
- (2) PIF Input ; 58.75MHz ± 1.0 MHz, CW 15mV_{rms}
- (3) Read the frequency (f_1) of PIF when $V_{13}-V_{14}=-1$ V
- (4) Read the frequency (f_2) of PIF when $V_{13}-V_{14}=1$ V

Then calculate

$$\Delta F/\Delta(V_{13}-V_{14})=|f_1-f_2|$$

Note 13) ΔF_W , V_{13U} , V_{14U} , V_{13L} , V_{14L}

- (1) INT AGC (P5 Open)
- (2) PIF IN ; 58.75MHz ± 10 MHz CW 15mV_{rms}
- (3) 8pF at Pin 16 should be shorted
- (4) Read the frequency (f_1 or f_2) when the V_5 or V_6 reduced to 90% level of A or B with varying the frequency. Then band width is the difference from center frequency (f_0).



Note 14) P5 : Open

PIF IN ; 58.75MHz CW 20mV_{rms}

- (1) Adjust the voltage of terminal 3 so that the voltage of terminal 4 will be 6.0V DC
- (2) Measure the terminal voltage 3



INTEGRATED CIRCUIT

TECHNICAL DATA

TA7680AP, TA7681AP

Note 15) P5 : Open

PIF IN ; 58.75MHz 100% APL 87.5% AM modulation signal amplitude 50mV_{p-p}
Measure detected output voltage (White peak to sync Tip)

Note 16) P5 : Open

SG₁ ; 58.75MHz CW 100mV_{rms}

SG₂ ; 54.25MHz CW 25mV_{rms}

Measure SIF (4.5MHz) output voltage at P15

Note 17) SIF IN ; f=4.5MHz FM f_{MOD}=400Hz Δf=±25kHz

(1) Adjust SIF Input Level 100mV_{p-p} and measure the detected output level v_{OS}

(2) Then decrease the Input Level so that the detected output level will be 3dB down of v_{OS} and measure the Input Level

Note 18) Output Impedance

(1) SIF IN ; f=4.5MHz, f_{MOD}=400Hz, Δf=±25kHz, 80dBμ

(2) AT P23 read the V_{O1} at R_X=∞, then read the R_X when recovered output become V_{O1}/2 with varying the R_X.

The R_X is the output impedance.

Note 19) ATT MAX.

(1) SIF IN ; f=4.5MHz, f_{MOD}=400Hz, Δf=±25kHz, 80dBμ

(2) Read the 400Hz component of V_{A1} at P2 with R_A=0, then read V_{A1}' with R_A=∞.

$$\text{ATT MAX} = 20 \log \frac{V_{A1}}{V_{A1}'}$$

Note 20) v_{PT}

(1) SIF IN ; f=4.5MHz, f_{MOD}=400Hz, Δf=±25kHz, 80dBμ

(2) Read the 400Hz component at P3

Note 21) G_V AF

(1) Apply 400Hz 0.1V_{rms} signal to P2

(2) Read the output voltage at P3



INTEGRATED CIRCUIT

TECHNICAL DATA

TA7680AP, TA7681AP

APPLICATION CIRCUIT

